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A D-BAND POWER AMPLIFIER WITH 30-GHz BANDWIDTH AND 4.5-DBM P_{sat} FOR HIGH-SPEED COMMUNICATION SYSTEM

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Abstract—This paper presents a D-band power amplifier for high-speed communication system. The capacitive effect of interconnection via on transistor performance at high frequency is analyzed and a new via structure is employed to reduce the capacitive effect. The on-chip matching technique for high frequency amplifier is analyzed and the thin-film microstrip line matching network is used, which is combined with biasing network to reduce RF signal loss and silicon cost. The amplifier is fabricated in 0.13-μm SiGe BiCMOS process. The experimental results show a 7 dB gain at 130 GHz with 3-dB bandwidth of 30-GHz. The input return loss is better than 10 dB over 23 GHz. In addition, this amplifier achieves saturated output

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power (P_{sat}) of 4.5 dBm and input 1-dB gain compression point ($P_{1\,\mathrm{dB}}$) of -4.5 dBm. The chip size of implemented power amplifier is only $0.22\,\mathrm{mm}^2$.

1. INTRODUCTION

With the development of data communication and multimedia applications, the demand of high-speed integrated circuits operating at tens of gigabits per second is rapidly growing [1–4]. Recently, some communication systems operate at 40 Gb/s have been proposed to meet the requirement of high speed communication. For a 40 Gb/s communication system, the bandwidth of whole system is needed to be larger than 25-GHz [5] and the carrier frequency has to be tens of gigahertz or even beyond hundreds of gigahertz. The III-V compound semiconductor is assumed a good candidate for high frequency operation. To date, it is used in most of the millimeter-wave circuit design. However, due to its incompatibility with commonly used low-cost CMOS intermediate frequency or base-band circuit and high fabrication cost, the III-V compound semiconductor is not the best choice for integrated system-on-chip (SoC) circuit design. In recent years, with the downscaling of device size, silicon-base transistor is capable to operate at higher and higher frequency. The demonstrated f_T and $f_{\max}$ of SiGe HBT technology is comparable with III-V compound semiconductor [6]. As demonstrated in previous publications [7–11], with good performance, compatibility with low-cost CMOS intermediate frequency or base-band circuit and also feature advanced passive components, the SiGe HBT BiCMOS technology becomes a favorable candidate for high frequency integrated circuit design.

The power amplifier is a key part in high frequency communication system. Although the available operating frequency of modern silicon-based transistor is very high, it is still a challenge to design a high frequency power amplifier with certain performance requirement [12–15]. In [16, 17], beyond 100 GHz amplifiers were realized in 65-nm CMOS technique. However, the bandwidth and linearity is not sufficient for our application. In addition, with the downscaling of transistor size, not only the cost is increased dramatically, some other limitations are also shown [18]. An amplifier was fabricated in SiGe technology, by using multistage cascode structure to achieve higher gain [19]. But by using the cascode structure, the higher supply voltage is required and then the efficiency will be deteriorated. Moreover, the linearity which is very important in our application is also affected by using the cascode structure. So it is not applicable for our design.

In order to transmit the signal efficiently, meanwhile maintain the stability of whole system, the matching network plays an important role in high frequency power amplifier design. In conventional designs, the lumped LC network is usually employed to form the matching network. However, due to the inaccuracy of modeling at high frequency and the impact of parasitic elements, the lumped LC network is not suitable for this work.

In this study, a D-band power amplifier is designed and fabricated in 0.13-μm SiGe BiCMOS process. The capacitive effect of via and its impact on transistor performance is analyzed. Then a new via structure is employed to reduce the impact of capacitive effect on transistor performance. After that, the linearity of power amplifier is analyzed and the method of optimizing the biasing condition is introduced. In addition, on-chip matching technique for high frequency amplifier is analyzed and a 2-stage thin-film microstrip line matching network which is combined with biasing network is used to achieve good return loss, wide bandwidth, compact size and good stability. Moreover, in order to achieve the maximum output power, the power matching methodology is used and the load-pull method is employed to optimal the load impedance. Finally, the broad-band design methodology is analyzed. The experimental results of the proposed power amplifier show a power gain of 7 dB at 130 GHz with the 3-dB bandwidth of 30 GHz. The saturated output power P_{sat} is 4.5 dBm and the return loss is better than 10 dB over more than 23 GHz bandwidth. The consumed silicon area of whole circuit is just 0.22 mm^2.

2. D-BAND CLASS A POWER AMPLIFIER DESIGN AND ANALYSIS

2.1. Transistor and Capacitive Effect of Via

The transistor plays the most important role in millimeter-wave circuit design. Its size and layout will obviously dominate the performance of whole circuit. In high frequency design, the main problem is the

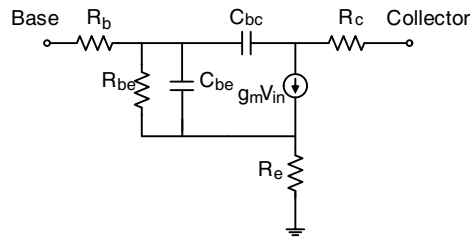

Figure 1. Small signal model of SiGe HBT transistor.

available gain of transistor is very low. The small signal model of SiGe HBT transistor is shown in Fig. 1. The maximum stable gain (MSG) of a transistor can be calculated base on the formula as follow:

$$MSG \approx \sqrt{\left(\frac{g_m}{\omega C_{bc}}\right)^2 + 1} \tag{1}$$

where g_m is the transconductance of transistor and C_{bc} is the parasitic capacitance between base and collector. From the formula (1), it can be seen that C_{bc} dramatically impacts the performance of device. In high frequency amplifier design, the signal trace is realized by the top metal layer due to its low signal loss. While the transistor is located below the bottom metal layer, so a deep via is needed to connect the device and signal trace, as shown in Fig. 2(a). With the downscaling of device size, the base and collector of transistor become very close in the layout. Then the capacitive effect between vias which are connected to base and collector cannot be negligible anymore and it will significantly increase the C_{bc}. The capacitance between vias can be estimated by the capacitance equation as follow:

$$C = \varepsilon_r \varepsilon_0 \frac{S}{d} \tag{2}$$

where ε_r is relative static permittivity, ε_0 is electric constant, S is overlap area and d is distance between the plates, as illustrated in Fig. 2. In amplifier design, the ε_r is decided by process and ε_0 is constant. Therefore, the variables we can use are — the area (S) and

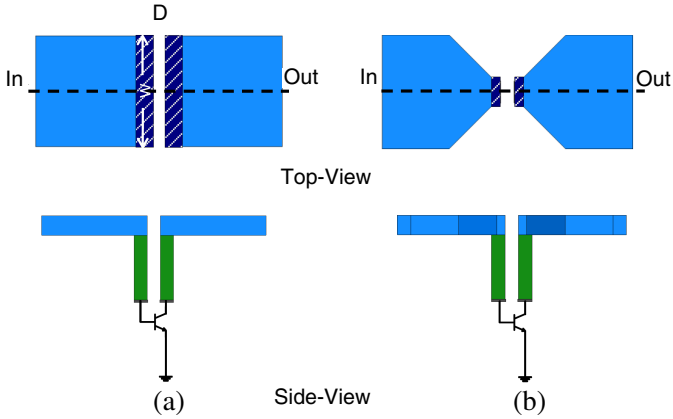

Figure 2. Structure of via which connect transistor and signal trace (a) conventional, (b) proposed.

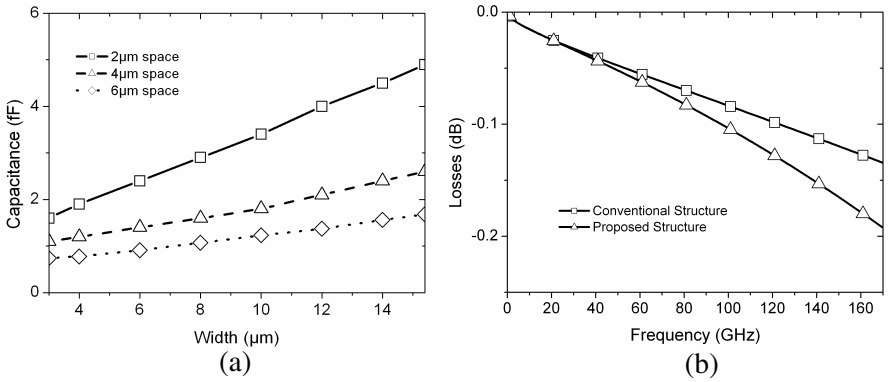

Figure 3. Capacitive effect and signal loss of via structure: (a) capacitive effect, (b) signal loss.

the distance (d). In addition, the length of via which equal to the distance between the signal trace and transistor is also decided by the process, because the signal trace is fixed at the top metal. Then only the width of via can be adjusted. The simulation results of vias at different width and distance is shown in Fig. 3(a). It can be seen that, the capacitance is dramatically increased with the increasing of width at every distance setting. Moreover with the narrow distance, the impact is more obvious. In addition, the distance between vias is also related to the process. Thus in this work, as shown in Fig. 2(b), the distance of via structure is set to 2 μm with the width of 3 μm. In this process, the intrinsic base-to-collector capacitance of the transistor is ~ 6 fF and the capacitance of other popularly used processes is on the same order. Then, by using formula (1), the maximum stable gain (MSG) of transistor is increased by 1.6 dB which is a big improvement for high frequency power amplifier design. As shown in Fig. 3(b), it should be noted that, by using the proposed via structure, the capacitive effect is depressed and the signal loss of via is just increased 0.05 dB which is acceptable for this work. By using above mentioned technique, the MSG of the transistor is maximized. Therefore by considering the losses of matching network and limitation of load impedance can be realized at high frequency, the gain of every stage can be optimized.

2.2. Linearity Consideration and Power Amplifier Topology

The linearity is a very important parameter in power amplifier design. It decides the capability of the amplifier to process the input signal.

The output 1-dB compression point ($OP_{1\,\mathrm{dB}}$) of the whole power amplifier can be obtained by using the following formula:

$$\frac{1}{OP_{1dB,all}} = \frac{1}{OP_{1dB,stage4}} + \frac{1}{OP_{1dB,stage3} * G_4} + \frac{1}{OP_{1dB,stage2} * C_3 * G_4} + \frac{1}{OP_{1dB,stage1} * G_2 * G_3 * G_4} \tag{3}$$

where $OP_{1dB,}*$ is the output 1-dB gain compression point of every stage and whole power amplifier, $G*$ is the gain of every stage. The gain of every stage is already optimized in Section 2. A. Then in order to achieve a good linearity of whole power amplifier, the linearity of every stage need to be optimized, especially the rear stages. The linearity of every stage can be calculated by using the formula as follow:

$$P_{1\,\mathrm{dB}} = \frac{I_s \cdot (V_C - V_{CE})}{4} \tag{4}$$

where V_c is the supply voltage of the amplifier, V_{CE} is the voltage between collector and emitter, I_s is the maximum current before 1-dB compression point [12]. The V_{CE} and I_s depend on the bias point. Therefore, by considering the limitation of application and process, the bias point can be calculated to achieve the optimal linearity. In this work, the bias condition of every stage is set to same level, due to the requirement of application and corresponding to the optimal linearity, the bias current I_b is set to 20 µA. In addition, as the application requirement of this work, the higher output power is demanded. So, the supply voltage of whole system is set to a higher level and then the efficiency will be a little degraded. In high frequency amplifier design, in order to achieve higher gain, the cascode structure is often used. However, the cascode structure requires higher supply voltage and then the efficiency will be deteriorated. Moreover, the performance of linearity which is very important in our application will also be affected by using cascode structure [19]. Therefore, the cascode structure is not suitable for this power amplifier design. As a tradeoff between gain, output power and efficiency, the common-emitter structure becomes the practical solution for this power amplifier design. The schematic of the proposed 4-stage common-emitter power amplifier is shown in Fig. 4.

2.3. High Frequency Amplifier Matching Methodology

In high frequency power amplifier design, the matching network is very important, due to it obviously impacts the performance of whole system, such as gain, return loss, stability, output power, efficiency

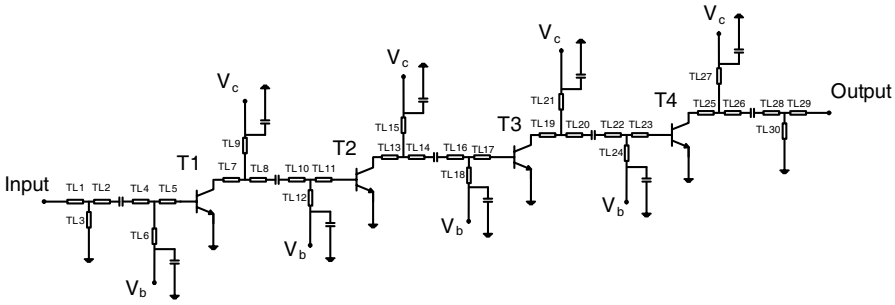

Figure 4. Schematic of proposed 4-stage common-emitter power amplifier.

and so on [20, 27]. Lumped element based matching network has been demonstrated up to 100 GHz recently [19]. However, at these high frequency designs, the accurate modeling of lumped elements such as capacitor, inductor and transformer is very difficult to be obtained. So the performance of matching network will depends on the accuracy of modeling. With simple structure and applicability of system integration, the thin-film microstrip line is suitable to form the matching network in high frequency amplifier design. The main drawback of thin-film matching network is its relatively large size (on the order of $\sim \lambda$). But, with the increasing of operating frequency, the λ becomes small. In our design the $1/4\lambda$ is $\sim 290\,\mu$m, so it becomes the suitable choice for this high frequency amplifier design. The structure of thin-film microstrip line is shown in Fig. 5. In this SiGe HBT technology, there are 5 normal metal layers and 2 top metal layers. The total dielectric thickness from metal 1 to top metal 2 is 10 µm and the conductor thickness of top metal 2 is 3 µm. So the signal line was realized by the thickest metal layer-top metal 2, since it gives minimum RF signal loss. The ground plane is realized by metal 1 with 0.5 µm thickness and the space between signal line and ground plane is 10-µm. The characteristic impedance of this thin-film transmission line can be expressed as follow:

$$Z_0 = \frac{1}{V_p Cap} \tag{5}$$

where Cap is the capacitance per unit length and the V_p is the phase velocity which can be calculated by $V_p = c/\sqrt{\varepsilon_f}$, where c is the speed of light and ε_f is the effective relative dielectric constant. The ε_f is related to the relative dielectric constant of the dielectric substrate and also takes the effect of the external electromagnetic fields into account [21]. After optimized through simulation, the width of signal

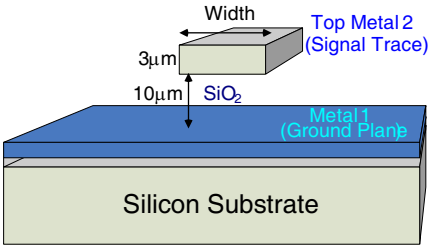

Figure 5. Thin-film microstrip line.

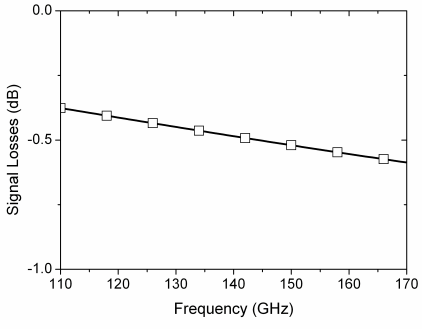

Figure 6. RF signal loss of 100-μm thin-film microstrip line.

line is set to 15 μm ($Z_0 = 50\,\Omega$). The simulated signal loss of this thin-film microstrip line with 100-μm length at different operating frequency is plotted in Fig. 6. From this figure, the RF signal loss is 0.4 dB to 0.6 dB over 110 GHz to 170 GHz. So it is suitable for using as signal trace and matching network. In order to achieve enough power gain and maximum output power at same time, the different matching strategies are used in input and output matching network design [28–30]. The conjugate matching method is adopted in input matching network design to achieve the maximum power gain, while the power matching method is adopted in output matching network design to obtain the maximum output power.

2.3.1. Input Matching Network

As mentioned above, the conjugate matching method is used in input matching network design to achieve maximum power gain, as shown in Fig. 7. The input matching is composed of several thin-film microstrip lines and one capacitor. Firstly, the input impedance of transistor Z_{trans} is transformed by the thin-film transmission line L_1. Then the admittance Y_3 is given by $Y_3 = Y_1 + Y_2$. Finally, the impedance Z_a is obtained from Y_3 which transformed by L_3.

Because our design is applied to a wideband high speed system, two-stage matching network is employed to form a wideband matching network. The microstrip lines L_4, L_5 and L_6 works similar to L_1, L_2 and L_3. The capacitor C_1 inserted between two matching network stages acts as not only impedance transforming, also DC signal blocking. The impedance of transistor Z_{trans} is then transformed to

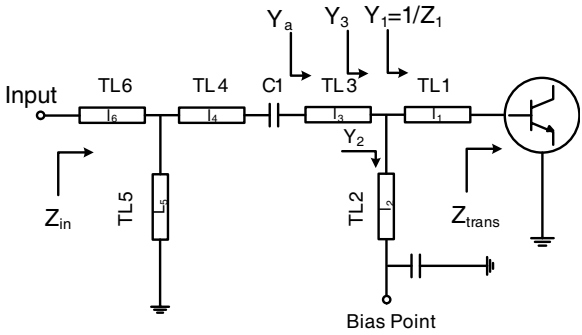

Figure 7. Input matching network.

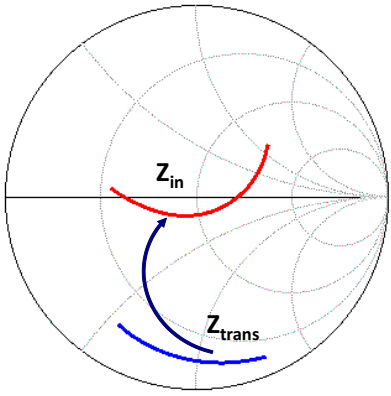

Figure 8. Smith chart representation of input impedance before/after matching network from 110 to 170 GHz.

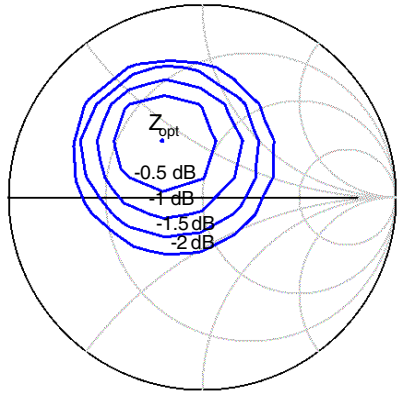

Figure 9. Output power courter under different load impedance by using load-pull method.

Z_{in} at the input point by the matching network. The smith chart presentation of Z_{trans} and Z_{in} from 110 GHz to 170 GHz are plotted in Fig. 8. Beside the function of impedance transform, the shunt thin-film microstrip line stub L_5 also works as the ESD protection circuit. The shunt stub L_3 has another function of circuit biasing. Then the biasing network is combined with matching network to eliminate the addition biasing network, which leads to less parasitic and gives a small signal loss [22, 31–34]. Also silicon area is utilized efficiently.

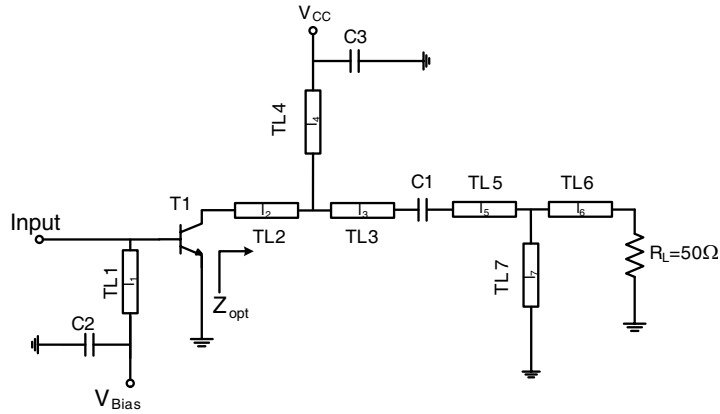

Figure 10. Output matching network.

2.3.2. Output Matching Network

The output matching is another critical consideration in power amplifier design, since it is required to deliver maximum power to the load. Therefore, the power matching method is used instead of conjugate matching method. Because of the nonlinear behavior under larger-signal operation, the load-pull method [24] is employed to determine the optimal load impedance. By using load-pull simulation, it gives an insight into how the output power change with the load impedance varies is obtained.

Figure 9 presents the output power contours under different load impedance by using the load-pull simulation. Then as a compromise between power gain and output power, the optimal load impedance is achieved as $27.9 + \mathrm{j}19.2\,\Omega$. The schematic of output matching network which is used to transfer the load impedance ($50\,\Omega$) to optimal load impedance is shown in Fig. 10. Beside the function of impedance transform, the shunt stab L_4 and L_7 in output matching network also act as bias network and ESD protect circuit, like their counterpart in input matching network to less parasitic and save silicon area.

2.4. Broad-band Design Methodology

Because the application of our design is high-speed communication system, the bandwidth of the amplifier is required to be very wide. The bandwidth of proposed amplifier depends on the inter-stage matching network [25]. As above mentioned, the L-C matching network is used for inter-stage matching, as shown in Fig. 11. Therefore, the

quality factor Q of inter-stage matching network will determine the bandwidth of whole amplifier and its impact is presented in Fig. 12. The bandwidth of the matching network can be calculated as follow:

$$BW = \frac{f_c}{Q} \tag{6}$$

where f_c is the center frequency. In this design, the required bandwidth is 30-GHz and the center frequency is 130-GHz. Therefore to satisfy the requirement, the Q must be smaller than 4.3.

The Q of matching network can be extracted by:

$$Q = \frac{imag(Z_m)}{real(Z_m)} \tag{7}$$

where Z_m is the input impedance of matching network. So the value of Q depends on the length and width of thin-film transmission line. On the other hand, if the Q is set very low, the peak gain of the amplifier

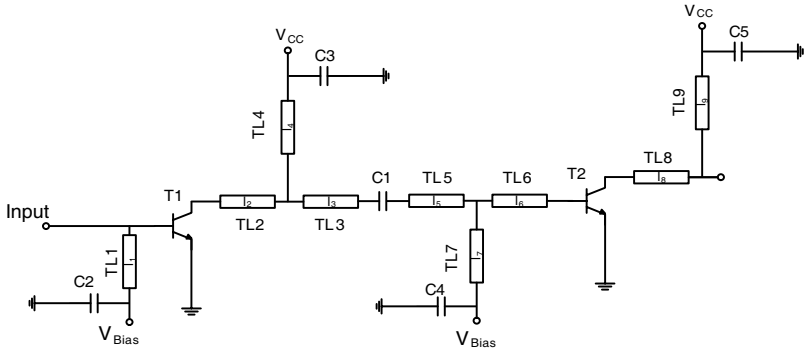

Figure 11. Inter-stage matching network.

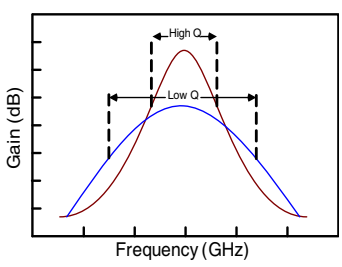

Figure 12. Impact of Q on bandwidth.

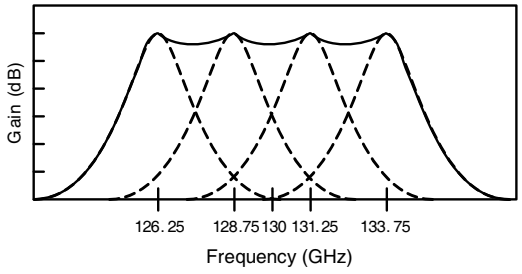

Figure 13. Frequency response of wideband power amplifier.

is also very low. Then, as a compromise of gain and bandwidth, in our design, the width of series transmission line is set to 15 μm and the width of shunt stab is set to 6 μm. Then the Q of matching network is 3.2 at 130 GHz. In addition, in order to enhance the performance of bandwidth, the peak frequency of every stage is set to different with 2.5 GHz spacing. Then the combined whole system is a very wide bandwidth power amplifier, as shown in Fig. 13. However, by using this method, the total gain of the whole amplifier will also be degraded. Then there is a trade-off between gain and bandwidth, which is decided by the application requirements [35, 36].

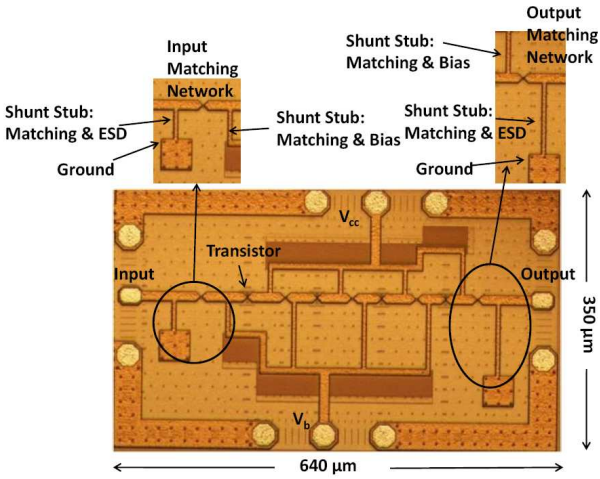

Figure 14. Chip micrograph of proposed amplifier.

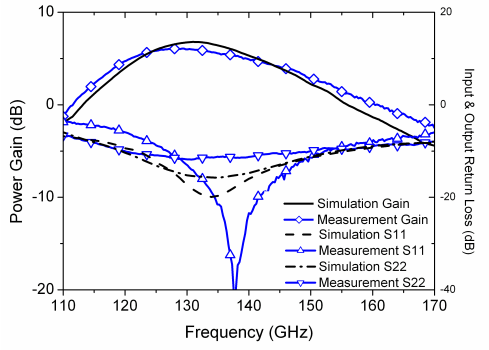

Figure 15. Simulated and measured gain and input/output return loss.

3. EXPERIMENTAL RESULTS AND DISCUSSION

The power amplifier is fabricated in 0.13 µm SiGe BiCMOS process with f_T of 180 GHz and $f_{\max}$ of 270 GHz. The measurement equipments are calibrated by using line-reflect-reflect-match (LRRM) calibration with a ceramic standard substrate. The chip photomicrograph of the fabricated power amplifier is shown in Fig. 14. The silicon area of this amplifier is only 0.22 mm^2.

The simulation and measurement results of power gain S_{21} and return loss S_{11}/S_{22} are shown in Fig. 15. The amplifier has a measured gain of 7 dB at 130 GHz and 6.1 dB at 135 GHz with a 3-dB bandwidth over 30 GHz from 117 to 148 GHz which can be used for 40 Gb/s transmission system [5]. The circuit draws 53 mA current from a supply of 1.5 V. When the supply voltage is set to 2.5 V, the gain of 6.5 dB can be achieved at 135 GHz, but the efficiency will be degraded. The input return loss is better than 10 dB over more than 23 GHz. From these figures, it is noted that by using the thin-film microstrip line to form the matching network, the return loss is good enough over very wide bandwidth and suitable for wideband application. Fig. 16 shows measured large signal characteristics of proposed amplifier. The measurement is performed at 135 GHz. The results show the input $P_{1\,\mathrm{dB}}$ of -4.5 dBm and the saturated output power (P_{sat}) of 4.5 dBm reaching maximum PAE of 4.1%. Finally, Table 1 summarizes the main performance of proposed amplifier and comparison with recently published high frequency amplifiers in silicon-based technology. Compared with other published high frequency amplifiers, the amplifier in this work achieved wider bandwidth and better linearity meanwhile other key parameters are also competitive.

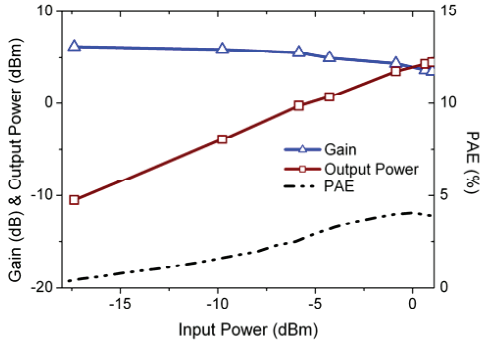

Figure 16. Measured output power and gain VS input power at 135 GHz.

Table 1. Performance summary of proposed power amplifier and comparison with recently published high frequency amplifier.

Reference	[16]	[17]	[19]	[23]	[26]	**This Work**
Process	65 nm CMOS	65 nm CMOS	0.13 μm SiGe	90 nm CMOS	90 nm CMOS	**0.13 μm SiGe**
Topology	4 CS	3 CS +3 CG	3 CC + 2 CE	3 CS	4 CS	**4 CE**
Frwquency (GHz)	100	140	170	104	77	**117-148**
Input P_{1dB} (dBm)	−6	−12	−12	NA	−2.8	**−4.5**
P_{sat} (dBm)	10	> −1.8	0	NA	6.3	**4.5**
Gain (dB)	13	8	15	9.3	8.5	**7**
Bandwidth (GHz)	20	10	14	2	17.5	**30**
Fractional BW (%)	20	7	8	2	23	**23**
PAE_{MAX} (%)	7.3	NA	NA	NA	2※	**4.1**
P_{DC} (mW)	86	63	135	22	142	**80**
Area (mm^2)	0.78×0.42	0.2×0.3*	0.48×0.2*	0.64×0.38*	1.5×0.65	**0.35×0.64**

*Estimate from the micrograph (not including pads)

※Estimate from the power transfer curve

CS: Common-Source, CG: Common-Gate, CE: Common-Emitter, CC: Cascode

4. CONCLUSION

In this study, a D-band power amplifier has been designed and fabricated in 0.13-μm SiGe BiCMOS process. In order to meet the requirement of bandwidth, gain and linearity, 4-stage common-emitter configuration is used and a new via structure is employed to reduce the capacitive effect. Then the linearity of power amplifier is analyzed and the proposed amplifier is optimized for higher output power. In addition, thin-film microstrip line is employed to form the matching network which combined with the biasing network to reduce the RF signal loss and silicon cost. From the experimental results, the designed amplifier shows good linearity, wide bandwidth, and other good performances, which are competitive with recently published high frequency amplifiers. Such crucial characteristics demonstrate the proposed power amplifier is suitable for high frequency high speed communication application.

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