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ANN-BASED PAD MODELING TECHNIQUE FOR MOSFET DEVICES

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Abstract—In this paper, an approach for the pad modeling of the test structure for Metal Oxide Semiconductor Field Effect Transistor (MOSFET) up to 40 GHz is presented. The approach is based on a combination of the conventional equivalent circuit model and artificial neural network (ANN). The pad capacitances and series resistors are directly obtained from EM (electromagnetic) simulation of the S parameters with different size of pad and operating frequency. The parasitic elements in the test structure can be modeled by using a sub artificial neural network (SANN). So the pad capacitances and series resistors can be regarded as functions of the dimensions of the pad structure and operating frequencies by using SANN. Good agreement between the ANN-based modeling and EM simulation results has been demonstrated. In order to remove the impact of the parasitic elements, the de-embedding procedure for MOSFET device using ANN-based pad model is also demonstrated.

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1. INTRODUCTION

With fast growth in the radio-frequency (RF) wireless communications market, the demand for high performance but low cost RF solutions is rising. This advanced performance of MOSFET is attractive for HF circuit design in view of a system-on-a-chip realization, where digital, mixed-signal baseband, and RF transceiver blocks would be integrated on a single chip. Design RF circuits which include MOSFETs requires accurate models to describe the RF behavior of MOSFET used in the circuit. However, the MOSFET is so small that it is impossible to measure its RF behavior by placing the coplanar probes directly on the devices. A test structure with probe pads and device under test (DUT) is needed for RF measurement. Usually we measure S parameter of the test structure to obtain the RF parameters of DUT. However, the existence of probe pads significantly affects the S parameter measurement of the DUT. The pad is sensitive to the substrate effects due to its large metal plate area and limits the performance of the devices or circuits using pads [1–3, 21–23].

In order to remove the parasitic impact of the pad, pad de-embedding is needed. Three ways are followed for pad de-embedding: One is obtaining the S parameter of pad by utilizing EM simulation. Another one is measuring the S parameter of the dummy device which excludes the DUT in the test structure [4–6]. The third one is a combination of the artificial neural network technique and the equivalent circuit model which based on the physical structure [1]. Artificial neural network which is used for building complex and nonlinear relationship between a set of input and output data has widely used in RF and microwave design recently [7–10]. The third method can solve the problem of quick and accurate modeling of pad. But in Ref. [1], low loss substrate is considered and it is not applicable to silicon substrate that is used in MOSFET devices. Comparing with low loss substrate, the equivalent circuit and the pad modeling for silicon substrate are more complicated. The introduction of resistors in the equivalent circuit model will make the parameter extraction more time-consuming. Furthermore, the series resistors are frequency-dependency that we must take frequency as a input parameter in the ANN model. As a result, the process of setting up ANN model for pad is more complicated than low loss substrate. The aim of this paper is to model the pad modeling of high loss substrate.

In this paper, an approach for the pad modeling of the test structure for RF MOSFET up to 40 GHz is presented. The approach is based on a combination of the conventional equivalent circuit model and artificial neural network (ANN). Each parasitic element of pad

in the equivalent circuit model can be regarded as a SANN. The pad capacitances and series resistors are directly obtained from EM (electromagnetic) simulation of the S parameters with different size of pad and operating frequency. Good agreement between the ANN-based modeling and EM simulation results has been obtained.

The organization of this paper is as follows: Section 2 describes the equivalent circuit model of the pad. Section 3 introduces the artificial neural network. The ANN-based modeling technique is described in Section 4. The de-embedding procedure for MOSFET devices is demonstrated in Section 5. The conclusion is shown in Section 6.

2. EQUIVALENT CIRCUIT MODEL OF PAD

A typical pad profile on silicon substrate and its corresponding equivalent circuit model are shown in Figures 1(a) and (b), respectively [11]. Where C_{pg} and C_{pd} represent the pad capacitance of the gate and drain between the signal pad and the ground pad respectively. C_{pgd} represents the coupling capacitance between the gate and drain pad. R_{pg} and R_{pd} represent the substrate loss resistance of the gate pad, the drain pad, respectively. All the parasitic elements can be determined as follows [12]:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_{pg} + Y_{pgd} & -Y_{pgd} \\ -Y_{pgd} & Y_{pd} + Y_{pgd} \end{bmatrix} \tag{1}$$

where Y is the matrix obtained from the conversion of S parameter that is measured from pad structure. Provided that $(\omega R_{pg} C_{pg})^2 + 1 \approx 1$, then we can get

$$\begin{aligned} Y_{pg} &= Y_{11} + Y_{12} = \frac{1}{R_{pg} + \frac{1}{j\omega C_{pg}}} = \frac{j\omega C_{pg} + R_{pg}(\omega C_{pg})^2}{(\omega R_{pg} C_{pg})^2 + 1} \\ &\approx R_{pg}(\omega C_{pg})^2 + j\omega C_{pg} \end{aligned} \tag{2}$$

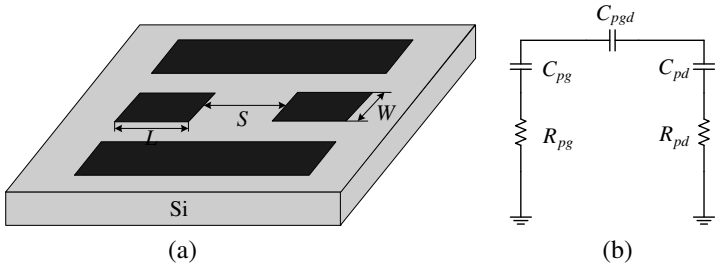

Figure 1. Pad and its equivalent circuit model. (a) Pad structure. (b) Equivalent circuit model.

$$Y_{pd} = Y_{22} + Y_{21} = \frac{1}{R_{pd} + \frac{1}{j\omega C_{pd}}} = \frac{j\omega C_{pd} + R_{pd}(\omega C_{pd})^2}{(\omega R_{pd} C_{pd})^2 + 1}$$

$$\approx R_{pd}(\omega C_{pd})^2 + j\omega C_{pd} \quad (3)$$

$$Y_{pgd} = -Y_{12} = j\omega C_{pgd} \quad (4)$$

From the above expression (2)–(4), we can get

$$C_{pg} = \frac{\mathrm{Im}(Y_{pg})}{2\pi f} = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{2\pi f} \quad (5)$$

$$C_{pd} = \frac{\mathrm{Im}(Y_{pd})}{2\pi f} = \frac{\mathrm{Im}(Y_{22} + Y_{21})}{2\pi f} \quad (6)$$

$$R_{pg} = \mathrm{Re}\left(\frac{1}{Y_{pg}}\right) = \mathrm{Re}\left(\frac{1}{Y_{11} + Y_{12}}\right) \quad (7)$$

$$R_{pd} = \mathrm{Re}\left(\frac{1}{Y_{pd}}\right) = \mathrm{Re}\left(\frac{1}{Y_{22} + Y_{21}}\right) \quad (8)$$

$$C_{pgd} = \frac{\mathrm{Im}(Y_{pgd})}{2\pi f} = \frac{-\mathrm{Im}(Y_{12})}{2\pi f} \quad (9)$$

where f is the frequency. For the symmetrical structure, we can get $R_{pg} = R_{pd}$ and $C_{pg} = C_{pd}$.

3. ANN TECHNIQUE INTRODUCTION

ANN is widely used in the optimization of passive components and microwave nonlinear device modeling [13–20, 24, 25]. The most commonly used and simplest network architecture called Multilayer Perceptron Neural Network (MLPNN). A MLPNN consists of three layers: an input layer, an output layer and an intermediate or hidden layer. The neurons in the input layer only act as buffer for distributing the input signals to neurons in hidden layer. Each neuron in hidden layer sums up its input signals after weighting them. Depending on the complexity of the input response and desired output, the number of hidden layers and neurons at each layer can vary. Training a network consists of adjusting its weights using learning algorithms. It is a very powerful approach for building complex and nonlinear relationship between a set of input and output data. For this reason, artificial neural networks recently gained attention as a fast and flexible tool to microwave modeling and design.

The neural network architecture used in this paper is the MLPNN. In theory, these networks can perform any complex nonlinear mapping. A typical MLPNN consists of an input layer, a hidden layer and an output layer is shown in Figure 2.

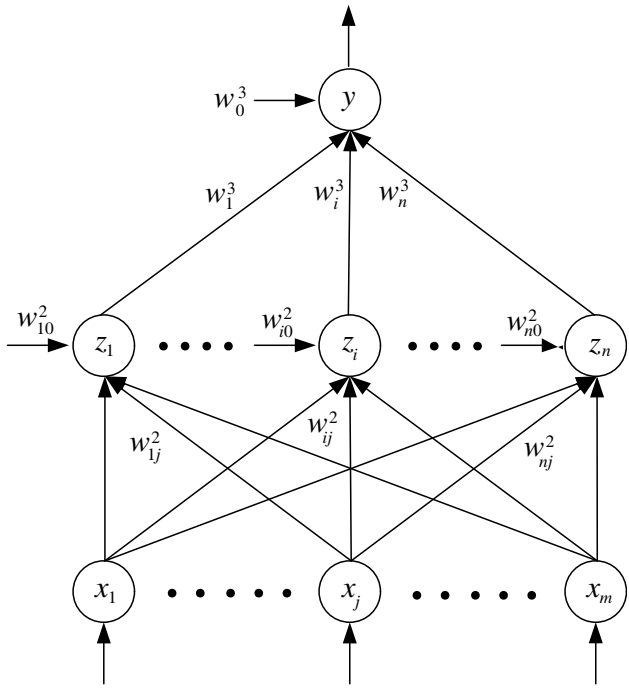

Figure 2. Three-layer MLPNN structure.

For given input x, the output of three-layer MLPNN can be computed by:

$$y = w_0^3 + \sum_{i=1}^{n} w_i^3 \sigma(Z_i) = w_0^3 + \sum_{i=1}^{n} w_i^3 \sigma\left(w_{i0}^2 + \sum_{j=1}^{m} w_{ij}^2 x_j\right) \tag{10}$$

where w_{ij}^l represents the weight of the link between the jth neuron of the $(l-1)$th layer and the ith neuron of the lth layer, w_0^3 and w_{i0}^2 represent the bias of each neuron of output and hidden layers, $\sigma(\cdot)$ is an activation function. The most commonly used hidden layer activation function is the sigmoid function given by

$$\sigma(x) = \frac{1}{1+e^{-x}} \tag{11}$$

The ANN model is then trained to learn the relationship between input and output by using training data which is a sample of input-output data. The purpose of training is to determine the ANN model parameters, i.e., neural network weights w_{ij}^l, such that the ANN model

predicted output best matches that of the training data. The testing data (new sample of input-output data) is used to test the accuracy of the ANN model.

4. ANN-BASED PAD MODELING TECHNIQUE

ANN-based microwave device modeling technique combines the conventional equivalent circuit and the artificial neural network modeling technique. Each intrinsic nonlinear circuit element can be modeled by using a SANN.

The pad capacitances and series resistors are determined by different size of pad and operating frequency. So the pad capacitances and series resistors can be regarded as functions of the dimensions of the pad structure and operating frequencies by using SANN. The input parameters values of ANN are shown in Table 1.

The pad capacitances and series resistors can be described by using SANN as follows:

$$C_{pg} = f_{\text{ANN}}^{C_{pg}}(W, L, S, Freq) \tag{12}$$

$$C_{pd} = f_{\text{ANN}}^{C_{pd}}(W, L, S, Freq) \tag{13}$$

Table 1. Variable pad input parameters values.

Parameter	Notation	Values
Width	W	30–100 μm
Length	L	30–100 μm
Slot	S	30–300 μm
Frequency	$Freq$	0–40 GHz

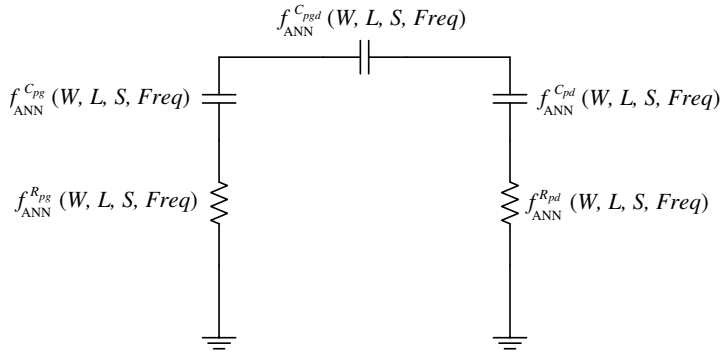

Figure 3. ANN-based equivalent circuit model of pad.

$$R_{pg} = f_{\text{ANN}}^{R_{pg}}(W, L, S, Freq) \tag{14}$$

$$R_{pd} = f_{\text{ANN}}^{R_{pd}}(W, L, S, Freq) \tag{15}$$

$$C_{pgd} = f_{\text{ANN}}^{C_{pgd}}(W, L, S, Freq) \tag{16}$$

where f_{ANN} represents ANN of each element of the pad. It can be found that the pad capacitances and series resistors are functions of W, L, S, $Freq$. The corresponding ANN-based equivalent circuit model of pad is shown in Figure 3.

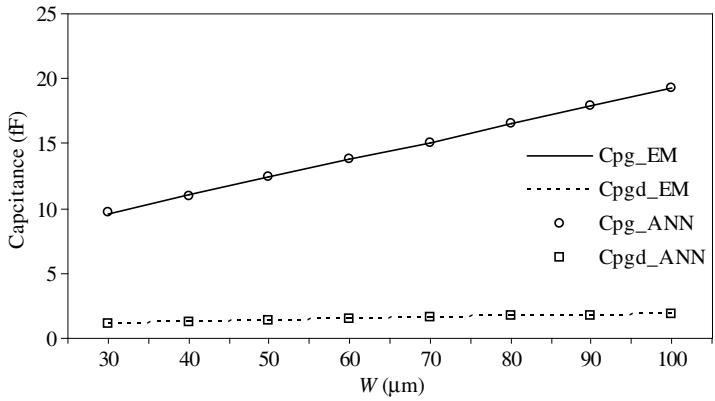

Figure 4. Pad capacitances versus its width ($L = 60\,\mu\text{m}$, $S = 180\,\mu\text{m}$ and $Freq = 10\,\text{GHz}$).

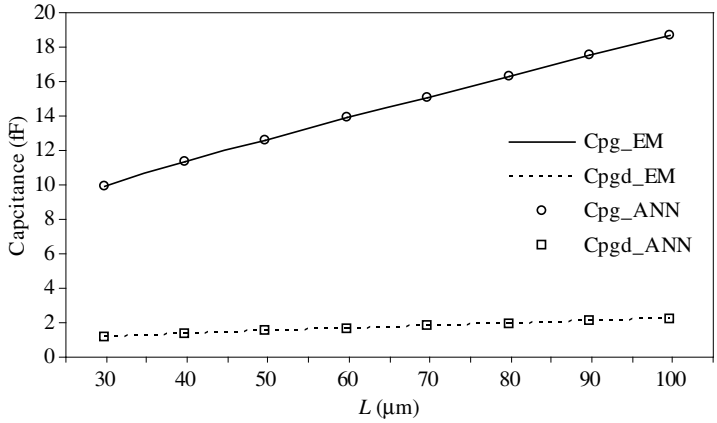

Figure 5. Pad capacitances versus its length ($W = 60\,\mu\text{m}$, $S = 180\,\mu\text{m}$ and $Freq = 10\,\text{GHz}$).

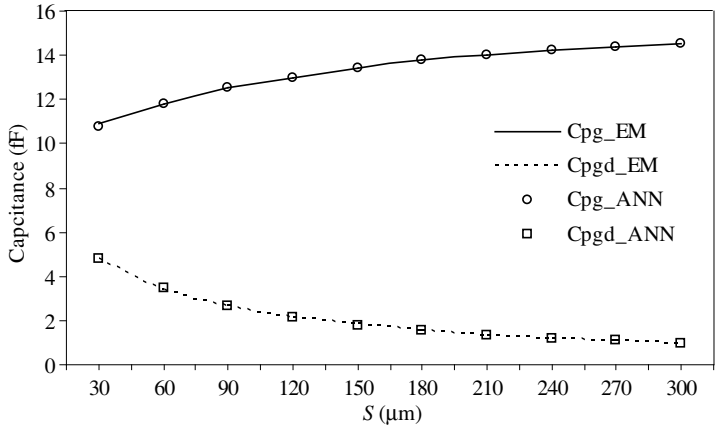

Figure 6. Pad capacitances versus its slot ($W = 60\,\mu m$, $L = 60\,\mu m$ and $Freq = 10\,GHz$).

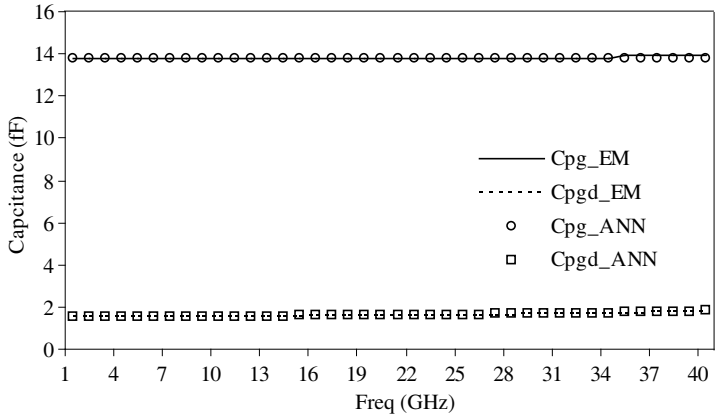

Figure 7. Pad capacitances versus its frequency ($W = 60\,\mu m$, $L = 60\,\mu m$ and $S = 180\,\mu m$).

The training data is obtained from Agilent ADS over a frequency range of 0 to 40 GHz by different pad dimensions. The training is conducted by using Quasi-Newton method until the difference between the training data and the output from the ANN model has reached less than 1%. 16 neurons are used in the hidden layer.

Figures 4–11 show the pad capacitances and series resistors versus with width W, length L, slot S and frequency $Freq$, respectively. Because the pad structure is symmetrical, the characteristic of C_{pg} and R_{pg} is identical with that of C_{pd} and R_{pd}.

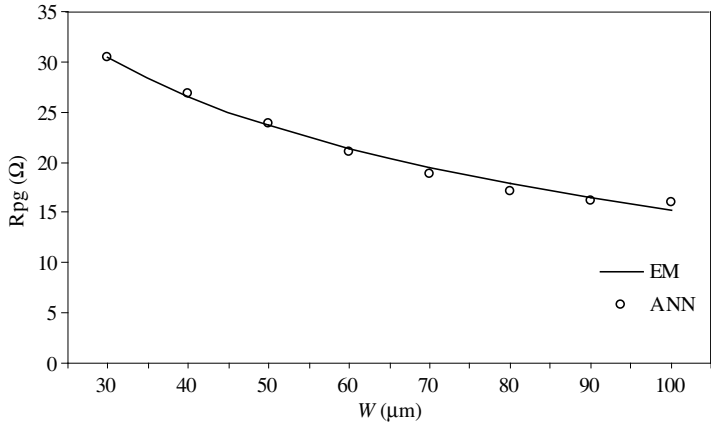

Figure 8. Series resistors versus its width ($L = 60\,\mu m$, $S = 180\,\mu m$ and $Freq = 10\,GHz$).

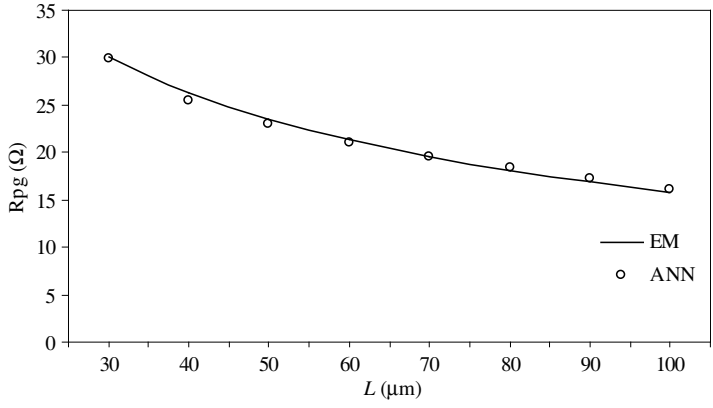

Figure 9. Series resistors versus its length ($W = 60\,\mu m$, $S = 180\,\mu m$ and $Freq = 10\,GHz$).

From Figures 4–11, we can see the comparison between the data obtained from the ANN model and the EM simulated data for the pad. When different size of device or circuit is considered, its pad performance can be obtained from the ANN model efficiently instead of EM simulation.

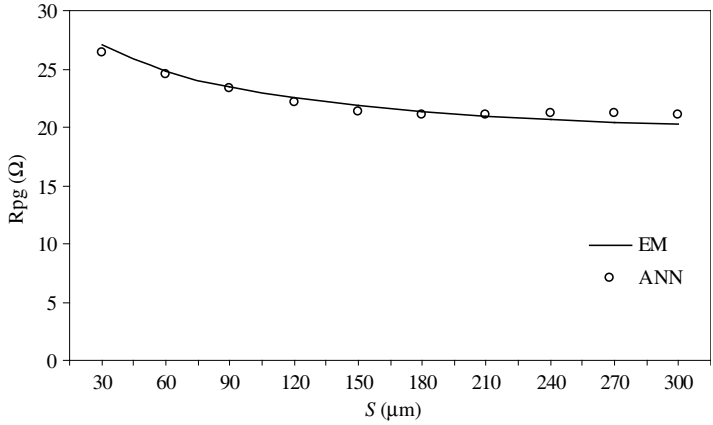

Figure 10. Series resistors versus its slot ($W = 60\,\mu\text{m}$, $L = 60\,\mu\text{m}$ and $Freq = 10\,\text{GHz}$).

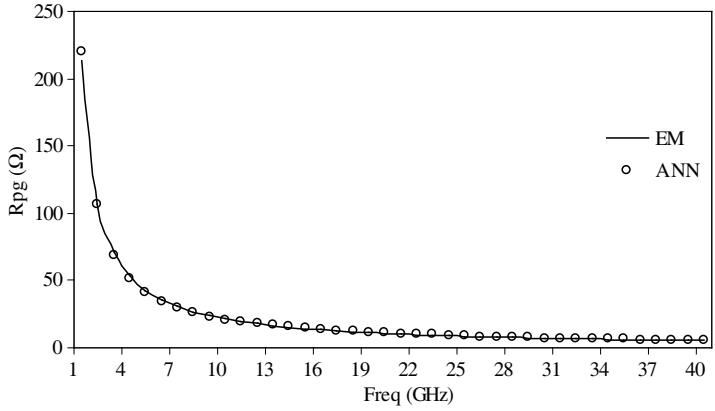

Figure 11. Series resistors versus its frequency ($W = 60\,\mu\text{m}$, $L = 60\,\mu\text{m}$ and $S = 180\,\mu\text{m}$).

5. PAD DE-EMBEDDING TECHNIQUE FOR MOSFET

Now we consider the pad presented by SANN and DUT together as shown in Figure 12.

In this paper, MOSFET devices are fabricated by using $0.18\,\mu\text{m}$ RF CMOS technology. The test structure dimension is $250 \times 350\,\mu\text{m}^2$, with pad dimension $W \times L \times S = 50 \times 50 \times 150\,\mu\text{m}^3$.

A measurement result from a calibrated probe is the response of the device under test including parasitics associated with probe pads.

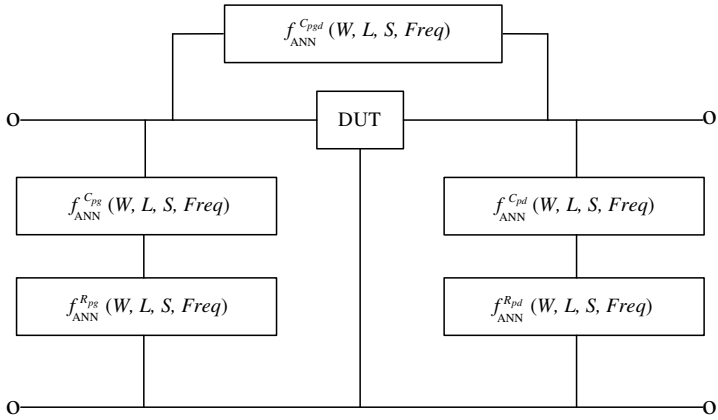

Figure 12. ANN-based pad and DUT network model.

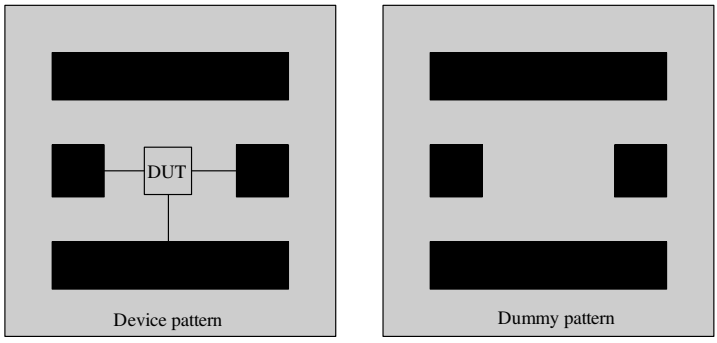

Figure 13. Device and dummy layout.

Pad capacitances can not be removed by using calibration method. In order to get the DUT response from measurement, the pad parasitics must be removed. So the dummy devices are introduced. Layout patterns, one including the DUT while the other (dummy) excluding it, are fabricated on the same wafer as shown in Figure 13. Here, we examine both pad de-embedding and probe pad layout techniques since they are closely related. Proper probe layout rules in addition to technology design rules must be followed.

The pad de-embedding procedure can be summarized as follows [6]:

1) Calibrate the network analyzer up to the tips of the probe by using either on-wafer or off-wafer calibration standard patterns.
2) Verify the calibration on the measurement wafer. Verification of

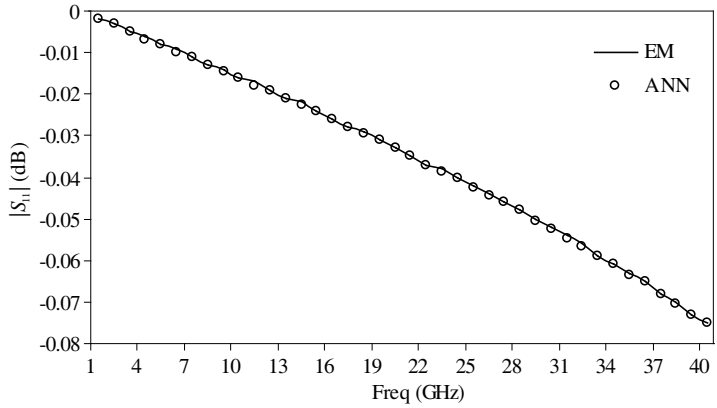

Figure 14. Comparison of S_{11} magnitude of pad between ANN-based method and EM simulated result.

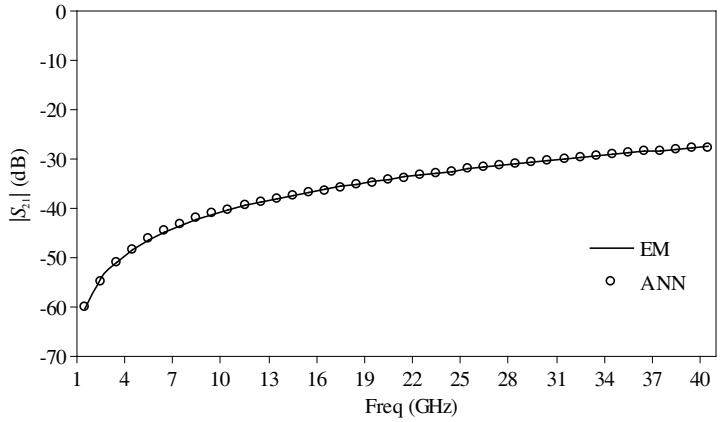

Figure 15. Comparison of S_{21} magnitude of pad between ANN-based method and EM simulated result.

the calibration can be done using high-Q inductors or capacitors. Verification will not be correct if it is done on the standard pattern where calibration is done. This is because those patterns are already used for calibration.

3) Measure the S parameters of the dummy device and convert them to Y parameters.
4) Measure the S parameters of the DUT and convert them to Y parameters.
5) Subtract the dummy Y parameters from DUT Y parameters, and convert the results back to S parameters.

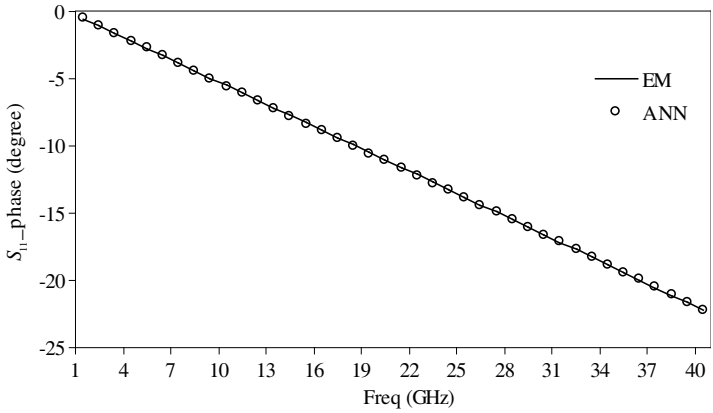

Figure 16. Comparison of S_{11} phase of pad between ANN-based method and EM simulated result.

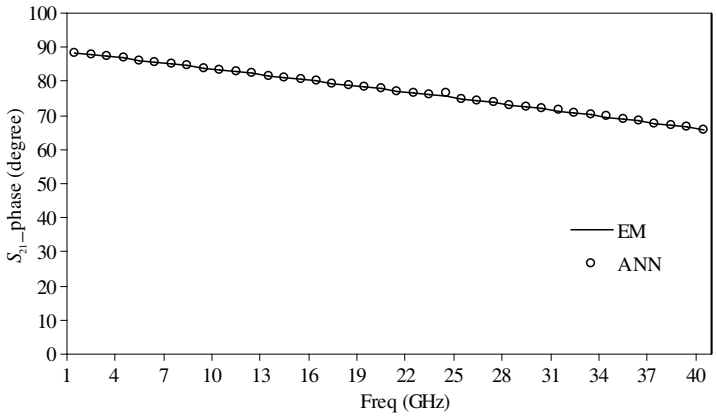

Figure 17. Comparison of S_{21} phase of pad between ANN-based method and EM simulated result.

By using ANN-based pad modeling technique, the S parameters of pad are shown in Figures 14–17 and good agreement is obtained between ANN-based model and EM simulated results.

By using ANN-based pad de-embedding technique, the parasitic effect is removed and the result is shown in Figure 18. From it we can see that the pad capacitances and series resistors affect more seriously to S_{22} and S_{12} than the magnitude of S_{11} and phase and magnitude of S_{21}.

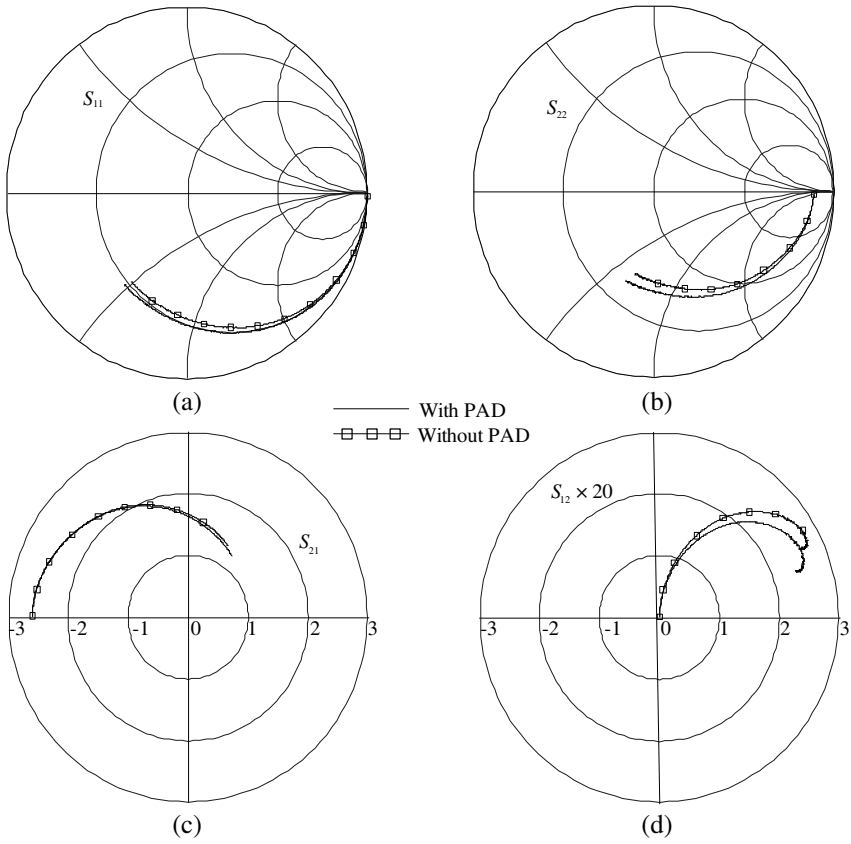

Figure 18. Comparison of MOSFET devices performance with and without pad (a) S_{11} parameter. (b) S_{22} parameter. (c) S_{21} parameter. (d) S_{12} parameter.

6. CONCLUSION

An approach of pad modeling technique based on a combination of the conventional equivalent circuit model and artificial neural network (ANN) is applied in order to investigate the pad effect to the high loss substrate on-wafer devices. Pad capacitances and series resistors for pad have been modeled by using sub artificial neural networks. Good agreement between the ANN-based modeling and EM simulated results demonstrates the validity of the pad modeling technique. Finally, the result of the pad de-embedding by using the proposed pad modeling technique is shown to demonstrate the impact of pad to MOSFET devices.

ACKNOWLEDGMENT

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