

MODELING AND LAYOUT OPTIMIZATION TECHNIQUES FOR SILICON-BASED SYMMETRICAL SPIRAL INDUCTORS

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Abstract—A scalable and highly accurate RF symmetrical inductor model (with model error of less than 5%) has been developed from more than 100 test structures, enabling device performance versus layout size trade-offs and optimization up to 10 GHz. Large conductor width designs are found to yield good performance for inductors with small inductance values. However, as inductance or frequency increases, interactions between metallization resistive and substrate losses render the use of large widths unfavorable as they consume silicon area and degrade device performance. These findings are particularly important when exploiting the cost-effective silicon-based RF technologies for applications with operating frequencies greater than 2.5 GHz.

1. INTRODUCTION

Integrated inductors are essential components in RFIC designs [1, 2]. Severe substrate and metallization losses associated with the silicon technologies prompted many researchers to devote their research efforts on the integrated spiral inductors [3–8]. To fully exploit the cost-effective silicon technologies, area-efficient inductors with optimized performance at the application frequency are required. A reliable and robust methodology that successfully optimized the physical layout of conventional spiral inductors up to 2.5 GHz has been previously proposed and published [9]. However, beyond 2.5 GHz, the inductors experience self-resonance and their inductances increase

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differently over frequency, making fair performance comparisons of identical inductance extremely difficult and complicated at high frequencies. The performances of active devices are advancing at such an amazing pace, attracting many cost-sensitive high frequency portable communication applications (> 5 GHz) to turn to silicon for solution. It is therefore critical for device and circuit design engineers to optimize the physical layout for integrated inductors and be fully aware of their design trade-offs operating at frequencies beyond 2.5 GHz.

The research outcome in [9] has established new knowledge, revealing that small inductors must be designed with large conductor width to suppress resistive loss achieving improvements in quality factor (Q -factor). As inductance increases, the conductor width has to be reduced to minimize the substrate loss which is more dominant than its resistive loss for these large inductors. With these important understandings in mind, this work attempts to develop a scalable symmetrical spiral inductor device model from a streamlined set of test structures designed based on the findings in [9], so that the physical layout of symmetrical spiral inductors can be optimized up to 10 GHz. Without these prior device knowledge, to develop a decent scalable inductor model that encompasses the full design permutations (predicting the effects of inductor's turn, core diameter and width), costly testchip and huge engineering resources would be required.

2. TEST STRUCTURE DESIGN CONSIDERATIONS AND EXPERIMENTAL SETUP

There are a few key challenges to overcome when developing an accurate and scalable inductor model. These challenges together with proposed solutions to overcome them are presented as follows:

1. Layout of the inductor's test leads must be fixed for ease of use and the input/output ports should use the highest metal layer (which is usually the thickest also) available in the processing technology. This would ensure lowest possible loss when connecting to other devices in the circuit.

2. A huge testchip with substantial number of inductors is necessary to develop a scalable device model. Hence, the inductor's layout and performance is best to be symmetrical at the input and output ports. Using symmetrical inductor, as shown in Figure 1, will result in time-efficient parameter extraction and model development processes. On the other hand, conventional spiral inductor has asymmetrical characteristics, requiring additional time to separately model the different substrate effects observed at the input and output

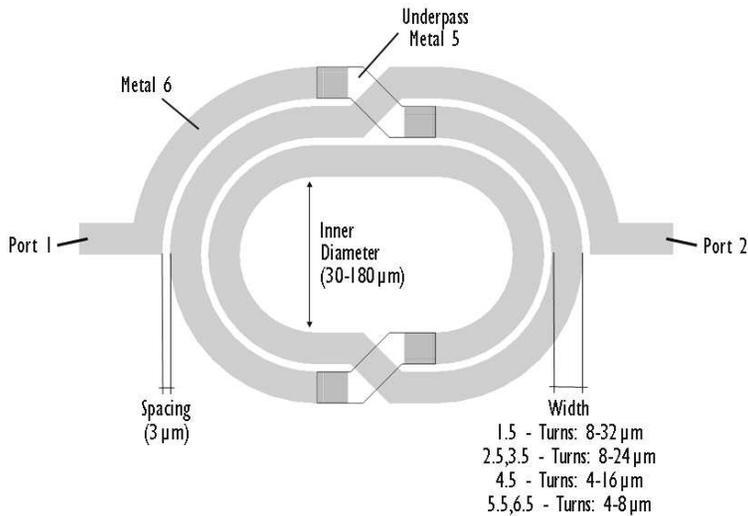
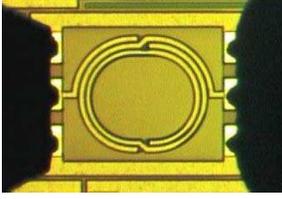


Figure 1. Physical layout scheme of symmetrical inductor for 0.18 μm RFCMOS technology.

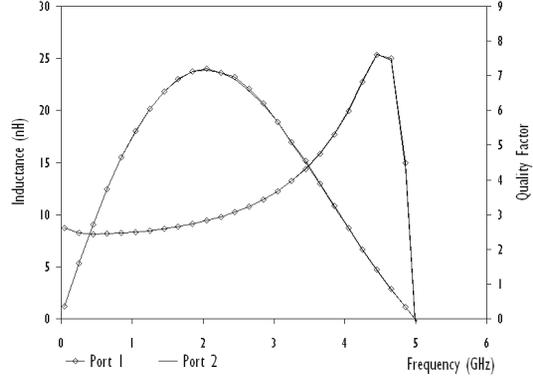
ports. Figure 2 compares the measured inductance and Q -factor for conventional and symmetrical inductors, showing asymmetrical characteristics for the conventional inductor design.

3. The inductor model must be able to generate inductors with fine inductance step variations, for example with 0.1 nH step size. This is a very important prerequisite for device performance comparison at high frequencies as well as circuit optimization. As revealed in Figure 10 of [9], varying the inductor's number of turns is not a suitable solution since the inductance steps between different turns are too large and increase at much higher rates as number of turn increases. For example, from 2 to 3-turn, L increases by 0.8 nH ; from 7 to 8-turn, L increases by 3.54 nH. To overcome this challenge, core diameter of the inductor will be varied in 1 μm steps to generate sets of inductors having fine inductance variations.

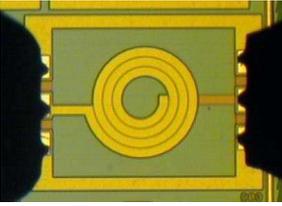
To address the stated adversaries, an extensive set of symmetrical inductor test structures has been designed. These test structures are fabricated using 0.18 μm RFCMOS processing technology. Figure 1 shows the layout of a 2.5-turn elliptically designed symmetrical inductor. Both input and output ports are designed with metal 6 (thickness of 2 μm) and metal 5 is used as underpasses to prevent shorting the coil. Such design has helped to achieve a very symmetrical layout, giving almost identical input and output port characteristics



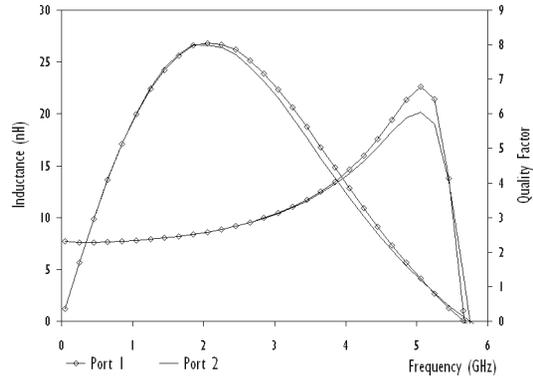
(a)



(b)



(c)



(d)

Figure 2. (a) & (b) Die photos and 2-port inductance and quality factor characteristics of symmetrical inductor and (c) & (d) conventional spiral inductor respectively.

as shown in Figure 2(b). Test element group consisting of 1.5 to 6.5-turn symmetrical inductors with core diameters ranging from 30 to 180 μm in steps of 30 μm is fabricated. The metal-to-metal spacing of the symmetrical inductors is fixed at 3 μm . Metal width, on the other hand, varies accordingly to the size of the inductors as stated in Figure 1. For example, 1.5-turn inductors are designed with widths from 8 to 32 μm and 6.5-turn inductors are designed with widths from 4 to 8 μm . From findings in [9], it would be a waste of expensive testchip resources if 6.5-turn inductors are drawn with width of 32 μm as their substrate losses will be too large, suffering self-resonance at very low frequencies and hence, completely not useful at all. Costly testchip

space is better utilized if 1.5-turn symmetrical inductors are designed with widths of $32\ \mu\text{m}$ which will reduce the peak Q -factor frequency and improves the Q -factor of these inductors at low GHz frequencies.

Agilent 8510C Vector Network Analyzer, Cascade Microtech's 300 mm probe station and Infinity probes are used to characterize these symmetrical inductors. Infinity probes are the preferred choice because they offer very low and stable contact resistance which is critical in obtaining the intrinsic performance of the inductors. Figure 2(a) depicts a die photo showing on-wafer RF measurement of a 2.5-turn symmetrical spiral inductor using infinity probes. The methodology of characterizing these symmetrical inductors and their figure of merits are identical to those adopted for conventional spiral inductors in [9]. Inductance, L and quality factor, Q of integrated inductors are determined from the de-embedded Y parameters by

$$L = \frac{\text{Imag} \left[\frac{1}{Y_{11}} \right]}{2 \times \pi \times \text{Frequency}} \quad (1)$$

$$Q = -\frac{\text{Imag} [Y_{11}]}{\text{Real} [Y_{11}]} \quad (2)$$

And series resistance, R , for spiral inductors can be expressed as follows,

$$R = \text{Real} \left[-\frac{1}{Y_{12}} \right] \quad (3)$$

L and Q are both extracted from Y_{11} and not Y_{12} parameters since it is important to include and consider the effects of the lossy silicon substrate when evaluating the overall performance of the spiral inductors. Parasitic series resistance, R is extracted from Y_{12} parameter to show the skin effects of metallization at radio frequencies, excluding substrate losses.

3. RF SUB-CIRCUIT MODEL AND EXTRACTION STRATEGY

Figure 3 illustrates the proposed scalable lumped-element RF sub-circuit model for symmetrical inductors. In the sub-circuit model, L_S and R_S account for the self-inductance and resistive loss of spiral coil respectively while L_{SK} and R_{SK} model the skin effects of the metallization at giga-hertz frequencies. C_S portrays the capacitive coupling between the input and output ports. Substrate loss of the symmetrical inductor is modeled by C_{OX} , C_{SUB} and R_{SUB} which describe the parasitic oxide capacitance between silicon substrate and

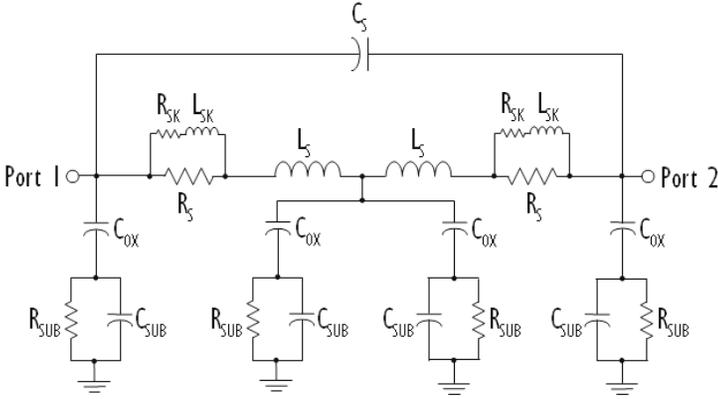


Figure 3. SPICE-compatible RF sub-circuit model for symmetrical spiral inductors.

inductor, the capacitive and resistive losses of the silicon substrate respectively. Since the layout is symmetrical, the extracted model parameters such as R_S , L_S , R_{SK} , L_{SK} , C_{OX} , R_{SUB} and C_{SUB} are identical. A double- π model instead of a simple single- π model is used for the symmetrical inductors because the total conductor lengths of these inductors are typically very long and as operating frequency increases, these metallization behave like transmission lines with distributed characteristics and hence, a simple lumped element π model is insufficient to describe its behavior [9].

Extraction strategy to obtain values of each element in the symmetrical inductor model is outlined in Figure 4. In this strategy, the open de-embedded Y -parameters for the symmetrical inductors are manipulated to derive parameters such as inductance L , Q -factor and series resistance R . Next, R_S is extracted at low frequency on the R versus frequency plot to ensure that subsequent model parameters obtained are physical and accurate. From L versus frequency plot, L_S and C_S are obtained separately focusing at the low and high frequency regions respectively. R_{SK} and L_{SK} are then acquired from Q -factor versus frequency plot, with emphasis around the peak Q -factor frequency regime to model metallization skin effects. The subsequent step for model development would be to extract the substrate loss elements from S -parameters and Y -parameters plots. All the model parameters are then further optimized to achieve better model accuracy.

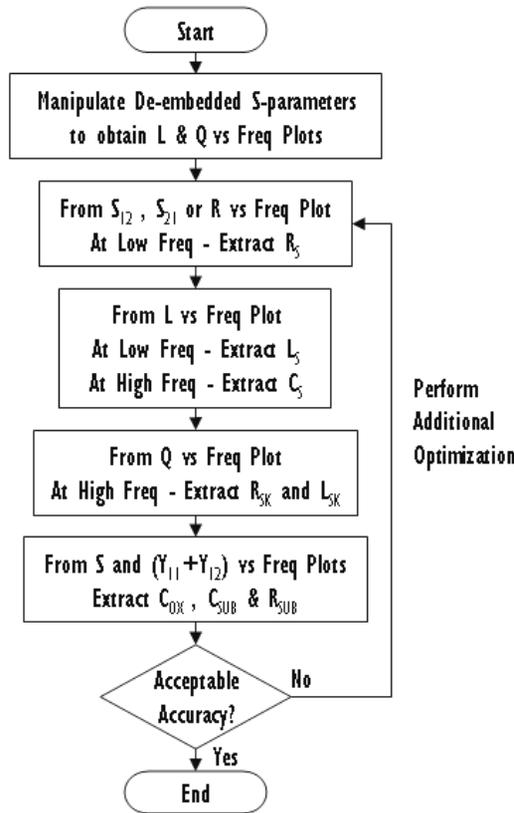


Figure 4. Model extraction strategy for symmetrical spiral inductors.

4. MODEL ACCURACY, CONTINUITY AND DESIGN TRADE-OFFS

To obtain measurement data for developing the symmetrical inductor model, a “golden wafer” is selected based on the measured resistivities of metal 5 and 6. Golden die is then chosen from this wafer as a die with typical inductance and Q -factor performance determined from full wafer map RF measurements of wide-width symmetrical inductors. For this work, automated multi-site RF measurement utilizes Cascade Microtech’s digital microscopy imaging technique to achieve consistent amount of skate for the RF probes on the test pads, correcting for the fluctuations in wafer thickness. This ensures identical probe contact resistance and therefore, variations in Q -factor are solely due to process variations in metallization thickness and its physical dimensions across

the wafer. For most silicon foundries, device modeling workflow normally takes place immediately after a technology node has been developed. Therefore, such die selection approach prior to performing device measurements for model development is critical in prolonging validity of the SPICE model as processing technology matures along with the implementation of yield enhancement techniques.

Using inductors' measurement data from a typical die and the proposed extraction strategy in Figure 4, model elements are extracted using IC-CAP, Agilent's device measurement and modeling software. After extraction, the model parameters are each put together with empirical formulae, which best emulate their behaviors, as functions of the inductors' turns, core diameter and width. As an example, Figure 5 shows how well this model can predict the measured inductance, Q -factor and series resistance for a 2.5-turn symmetrical inductor with core diameter and width of 60 and 8 μm respectively. 2.45 and 5.05 GHz have been selected to examine the accuracy as well as continuity of this scalable model. Box plots in Figure 6 have revealed outstanding predictability and accuracy for the symmetrical inductor model. For most of the useful inductors that have yet to operate beyond their self-resonant frequencies, model deviations between the measured and simulated inductance are within -1% to 3% for 2.45 and 5.05 GHz. Q -factor, on the other hand, has model deviations ranging from -3% to 5% for 2.45 and 5.05 GHz.

The symmetrical inductor model is shown to be continuous, capable of predicting inductance and Q -factor for all the test structures with various turns, core diameters and conductor widths as illustrated

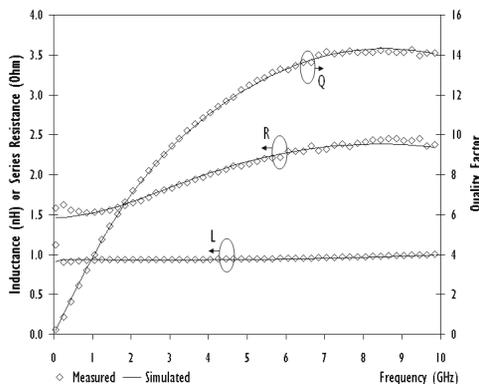


Figure 5. Simulated versus measured inductance L , Q -factor for 2.5-turn symmetrical inductor with core diameter and width of 60 and 8 μm respectively.

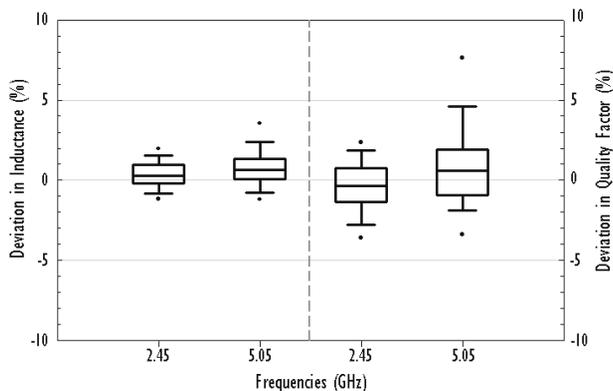


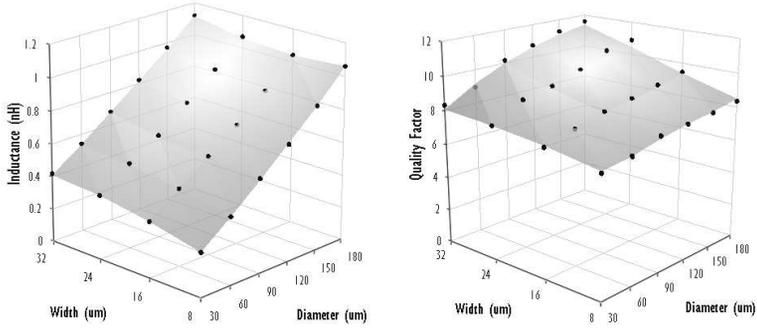
Figure 6. Box plots showing deviations between SPICE model simulated and measured inductance and Q -factor at 2.45 and 5.05 GHz for all symmetrical inductors in the test element group.

in Figure 7. These 3-dimensional plots also disclosed excellent linearity in inductance values for all the symmetrical inductors when core diameter increased from 30 to 180 μm . Therefore, designing the test structure in this manner and changing the core diameter in steps of 1 μm will ensure the establishment of inductor device library with fine inductance steps spanning a full range of application frequencies that can address the challenges set forth in Section 2.

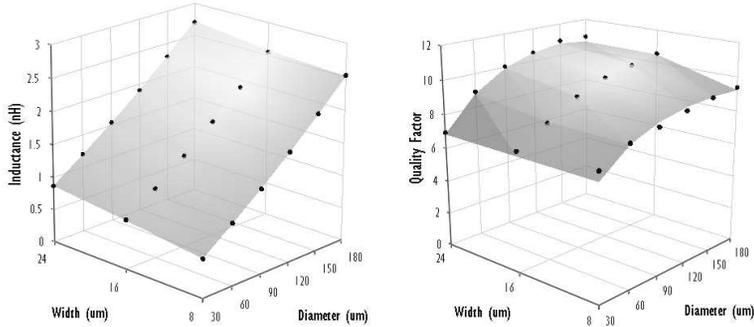
Figure 8 illustrates the inductance versus Q -factor plots for 2.5-turn symmetrical spiral inductors. On this graph, each of these plots represents a set of 2.5-turn inductors having a fixed conductor width with diameters varying from 30 to 180 μm . For instance, when diameter changes from 30 to 180 μm for the conductor width of 8 μm , inductance values from 0.6 to 2.6 nH are obtained correspondingly. Drawing iso-inductance lines across the plots in Figure 8 facilitate impartial performance evaluations on the effects of conductor width for the symmetrical inductors. For example, when a 2 nH iso-inductance line crosses the three plots, it is observed that for the widths of 8, 16 and 24 μm , in order to obtain inductors with exactly 2 nH at 2.45 GHz, the core diameters must be between 120 and 150 μm . Making use of the scalable symmetrical inductor model to perform 1 μm linear interpolation of the core diameter allows 3 inductors with widths of 8, 16 and 24 μm to have exactly 2 nH at 2.45 GHz.

Figure 9 shows the inductance and Q -factor versus frequency plots for 2 nH symmetrical spiral inductors at 2.45, 5.05 and 10.05 GHz obtained using the scalable symmetrical inductor model. These

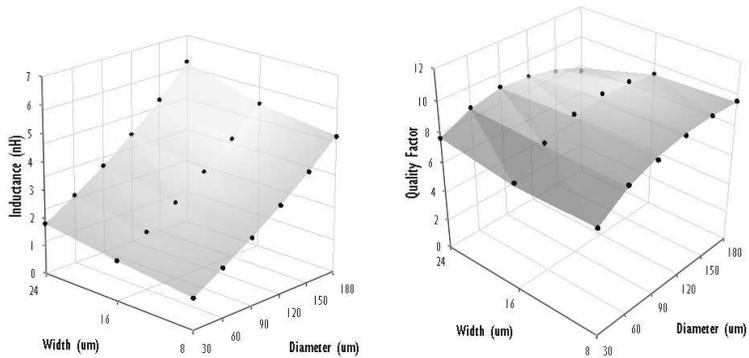
graphs have indeed revealed the fact that varying and optimizing the core diameters in $1\ \mu\text{m}$ steps has successfully allowed symmetrical inductors of different conductor widths to have identical inductance values and hence, non-biased performance comparisons at application



(a)



(b)



(c)

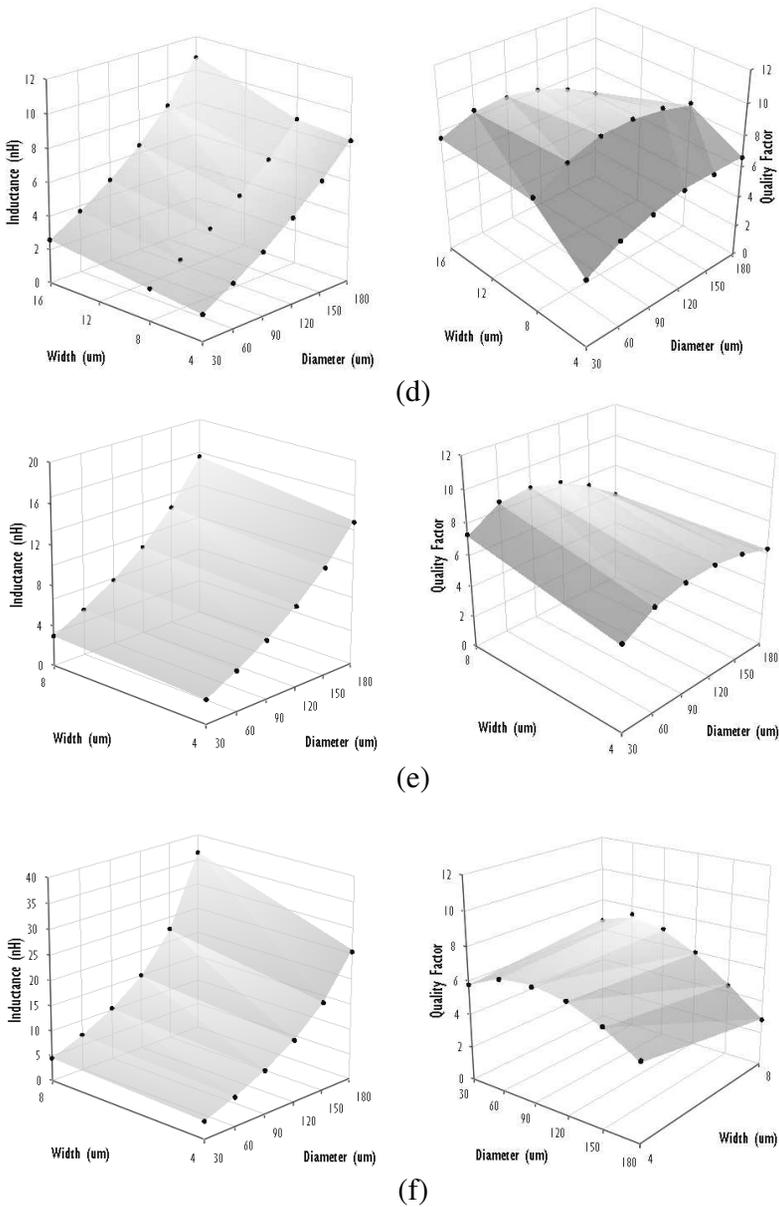


Figure 7. RF symmetrical inductor model continuity — simulated (surface) and measured (dots) inductance and Q -factor versus diameter and width at 2.45 GHz for (a) 1.5-turn, (b) 2.5-turn, (c) 3.5-turn, (d) 4.5-turn, (e) 5.5-turn and (f) 6.5-turn symmetrical inductors.

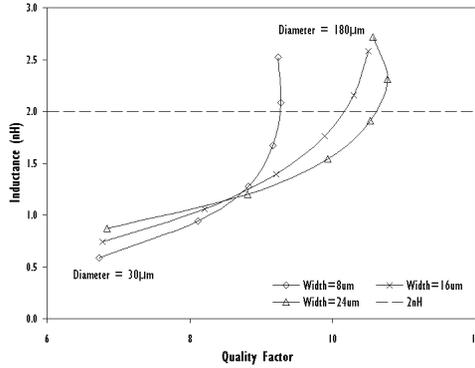


Figure 8. Inductance versus Q -factor for sets of 2.5-turn symmetrical inductors with core diameters from 30 to 180 μm and different widths at 2.45 GHz.

frequencies up to 10 GHz. As operating frequency increases, 2 nH symmetrical inductors with larger widths must be designed to have smaller low-frequency inductances (much less than 2 nH), taking into considerations self-resonance effects to ensure that these inductors would have exactly 2 nH at the frequency of interest, making fair device performance comparisons possible. Facilitated by the accurate and scalable symmetrical inductor model developed in this work, these innovative experimental comparisons are performed conveniently for the first time at frequencies more than 2.5 GHz.

Figure 9(a) concludes that at 2.45 GHz, use of 24 μm conductor width instead of 8 μm for 2 nH symmetrical inductor reduces the resistive loss at low frequencies, thereby improving Q -factor by about 15%. Although implementing such design approach trade-off substantial chip area for better device performance, optimal widths exist across each operating frequencies beyond which any further use of larger width and silicon real estate would renders this technique ineffective. To illustrate this, in Figure 9(c), at 10.05 GHz, using 8 μm conductor width instead of 16 μm for the 2 nH inductor results in higher Q -factor with more than 53% improvement. Although the inductor with 8 μm conductor width has lower Q -factor at frequencies below 3 GHz, as operating frequency increases, substrate loss which is directly proportional to conductor width becomes very dominant for the large-size inductor with width of 16 μm , thereby causing fast Q -factor roll-offs. Hence, at 10.05 GHz, Q -factor for 8 μm width inductor is observed to be the most superior.

Figure 10 consolidates and compares 1, 2 and 4 nH symmetrical

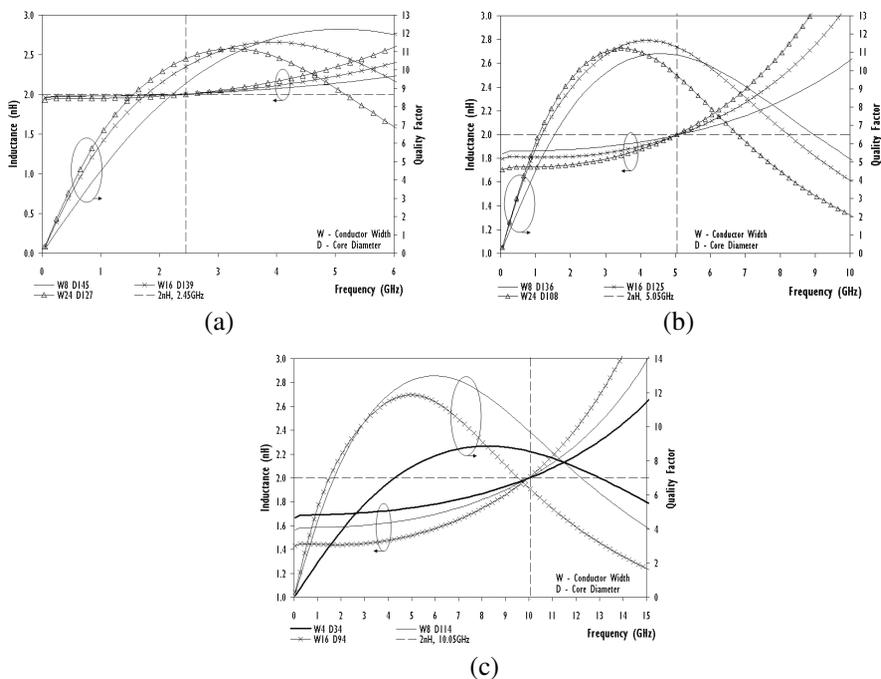


Figure 9. Inductance and Q -factor versus frequency for 2 nH symmetrical inductors at (a) 2.45, (b) 5.05 and (c) 10.05 GHz.

inductors at 2.45, 5.05 and 10.05 GHz, with identical inductance values, plots of Q -factor versus conductor width. As inductance or operating frequency increases, trade-offs between resistive and substrate loss results in the existence of optimal widths such that beyond these widths, any further use of larger conductor widths do not improve Q -factor but waste expensive silicon area. This is evident for 2 and 4 nH inductors in Figures 10(b) and (c) respectively, showing degradations in Q -factor for operating frequency of 10.05 GHz when conductor width of more than 8 μm is used. To sum up, when operating frequency increases, employing narrower conductor width and thus shorter total conductor length (narrow width conductor have larger per unit length inductance) concurrently results in smaller inductor size, lower substrate loss and better device performance all at the same time.

Figure 11 summarizes the 3 plots in Figure 10, describing the optimal widths which will give the highest Q -factor at various inductance values and operating frequencies. In general, as frequency

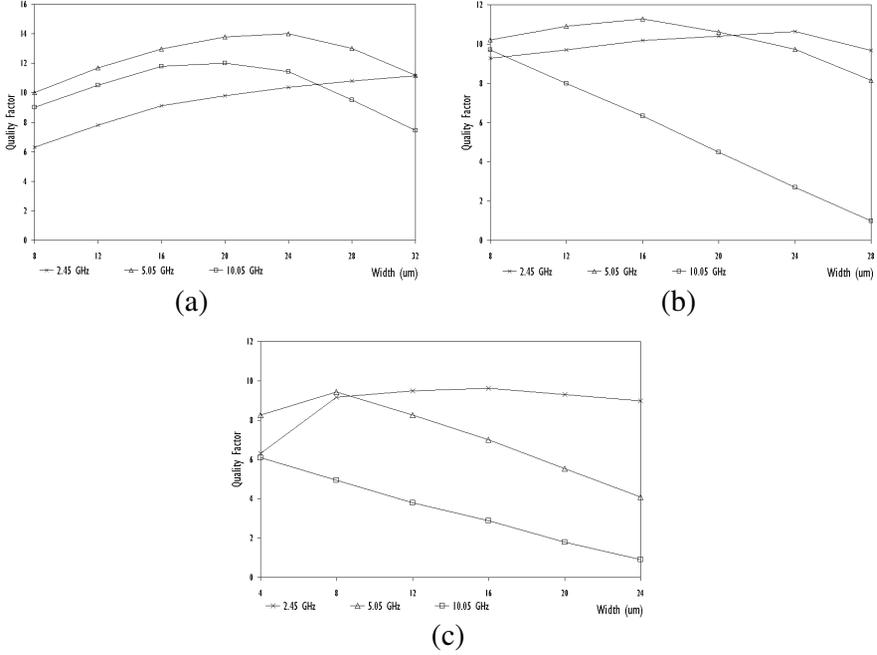


Figure 10. Q -factor versus conductor width for (a) 1 nH, (b) 2 nH and (c) 4 nH symmetrical inductor at operating frequencies of 2.45, 5.05 and 10.05 GHz.

or inductance increases, the optimal widths, whereby highest Q -factor can be attained from a given symmetrical inductor design, would be reduced. Figure 11 also compares, for the first time, at 2.45 GHz, optimal widths between conventional spiral inductors (Figure 19 of [9]) and the symmetrical spiral inductors in this work. Although the physical design optimization techniques for these 2 inductors are different, they yielded almost identical optimal width versus inductance characteristics. This provided confidence to the proposed methodology of using an accurate and scalable device model to extend the physical layout optimization of inductors beyond 2.5 GHz. It is also motivating to note that when operating frequencies increases, optimal widths for spiral inductors decreases. As silicon processing technologies advances with huge improvements made to the transistor's speed and cut-off frequency, RF circuits operating at higher frequencies will benefit from small-size, high Q -factor inductors.

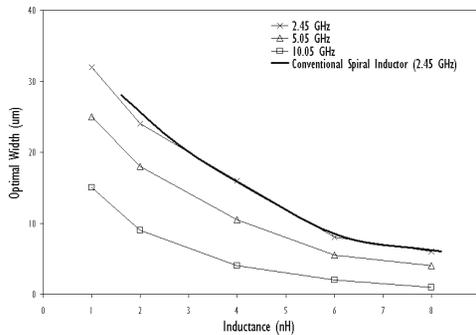


Figure 11. Optimal width for symmetrical inductor at operating frequencies of 2.45, 5.05 and 10.05 GHz and comparing conventional spiral [9] and symmetrical spiral inductor at 2.45 GHz.

5. MODEL VERIFICATION AND EVALUATION OF THIS WORK

Validity of the symmetrical inductor model has been verified using a differential amplifier which was already presented in [10] (Figures 9 and 10). This inductor model has outstanding accuracy and scalability which was demonstrated with excellent correlations between measured and simulated circuit results. Most of the research studies published in the literature utilized limited test structures to develop scalable inductor models. They also fail to ensure identical inductance values when making device performance comparisons at different application frequencies [11–14]. On the contrary, this research work has a huge test element group of 102 inductors spanning wide-ranging physical design parameters of 1.5 to 6.5-turn, widths from 4 to 32 μm and core diameters from 30 to 180 μm , to comprehensively test the proposed extraction strategy and model development methodology for the symmetrical inductors.

Table 1 consolidates a number of key research papers that were recently published in prominent technical journals to compare the contributions achieved for this work [3–7]. Notably, this research employs the most number of test structures for model development, achieving the smallest absolute model error. In contrast to the use of EM simulated inductor characteristics as measured data for developing non-SPICE compatible artificial neutral network model [8], this work has designed, fabricated and performed device characterization for a hundred inductors to develop a practical, accurate and scalable model. Being SPICE compatible, the symmetrical inductor model was

Table 1. Comparing various research works on modeling and optimizing the design of spiral.

First Author	Y. Cao	J. Chen	X. Huo	W. Gao	F. Huang	S. K. Mandal	This Research Work
Reference	[3]	[4]	[5]	[6]	[7]	[8]	
Technical Journals	IEEE JSSC	IEEE TED	IEEE TED	IEEE TMTT	IEEE JSSC	IEEE TCAD Cir & Sys	
Year of Publication	2003	2006	2006	2006	2006	2008	
Number of test structures used for model development.	11	3	7	14	5	400 (EM Simulated data)	102
How many elements are in the proposed model?	24	12+ $S \times 10$ (S = no. of Segments, a 3-turn inductor, has 62 elements, each inductor will have a different model)	20 (More elements to be added for better accuracy)	24 (All have to be extracted)	20	Unknown (Artificial Neutral Networks (ANN) models for 0.18 μ m CMOS Inductors)	21 (Only 8 elements have to be extracted)
What is the operating frequency supported by the model?	10 GHz	15 GHz (acceptable model fitting up to 10 GHz)	10 GHz	20 GHz (acceptable model fitting up to 10 GHz only)	10 – 20 GHz	Up to 2.5 GHz	10 GHz (or Self-resonant, whichever is lower)
What is the model error/deviation?	Q deviation* -10.8 – 8.7 %	Only fitting results for 3 inductors (No model Deviation)	Only fitting results for 7 Inductors (No model Deviation)	Only fitting results for 3 inductors (No model Deviation)	L : 6.6 % Q : 8.9 %	L : 15 % Q : 8 % (After testing ANN-model with another 100 EM simulated inductors)	L : -1 to 3 % Q : -3 to 5 % (For all inductors at 2.45 and 5.05 GHz)
Is the model scalable to the inductor physical design parameters?	To a certain extent, but only 11 inductors with limited turns, widths and diameters	Only 3 inductors having 2.5, 3 and 5 turns	Only 7 Inductors with different turns and substrate resistivities	Only 3 inductors results are published	Only fitting results for 5 inductors	Unknown (No data published and no inductor data to compare)	Yes (102 inductors, Scalable across different Turns, Width, Diameter)
What is the performance of the model continuity for different physical dimensions?	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown (No L and Q fitting plots against the physical dimensions of Inductors)	Excellent (Model is continuous Figure 7)
Is the model SPICE-compatible?	Yes	Yes	Yes	Yes	Yes	No (No sub-circuit models for inductors were published)	Yes
Trade-off studies between performance, layout and operating frequency at same inductance value?	No	No	No	No	No	3 nH at 2.5 GHz 4 nH at 1 GHz (ANN model was traied based on EM simulated inductor results)	Yes (Recommend the optimal widths for different inductance values up to 10 GHz Figure 11)
Has the model been verified in test circuits?	No	No	No	No	No	No	Yes

* Absolute error is calculated instead of the published root mean square error

verified with a differential amplifier and further exploited to make novel analysis in the trade-off studies between the inductor layout design and its performance up to 10 GHz.

6. CONCLUSIONS

From a streamlined set of test structures, a highly accurate and scalable RF inductor model has been developed in this work, enabling unique quantitative analysis of performance and layout by comparing inductors with identical inductance values at frequencies up to 10 GHz. Large-width designs benefit inductors with small inductance values. When inductance increases, there are optimal widths such that using much larger widths would only waste chip area and not improve Q -factor. As operating frequency increase, these optimal conductor widths will have to be reduced, achieving the benefit of having small-size symmetrical inductors with high Q -factors.

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