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CMOS Low Noise Amplifier Design for Microwave and mmWave Applications

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(*Invited Review*)

Abstract—This paper reviews recent advances in the design of low noise amplifier (LNA) in complementary metal oxide semiconductor (CMOS) technology for radio transceivers at microwave and millimeter wave (mmWave) frequencies. First, the evolution of wireless communication systems and CMOS technology are briefly revisited to highlight the requirements of an LNA design. Then, key performance parameters and device circuit models are described. Next, we discuss typical LNA topologies, followed by those important design techniques, algorithms and concepts developed specifically for CMOS LNAs. Moreover, reported CMOS LNA designs are summarized, and future design issues are identified. Finally, we conclude the paper and briefly outline our future work on CMOS LNA designs.

1. INTRODUCTION

With the rapid development of wireless communications, increasing number of subscribers demand for high data rate services with multimedia applications, such as video conferencing, online gaming and telemedography [1]. Although better paradigms of wireless networking, such as multihop cellular networks [2] could potentially increase the frequency reuse and reduce the imminence of demanding for more bandwidth, further development of wireless communications inevitably require more bandwidth to support applications with even higher data rates, e.g., at about one gigabits/s (Gbps) per data link. Fortunately, 7 GHz of contiguous microwave bandwidth has recently been opened for unlicensed use at the extremely high frequency (EHF) band in USA (57–64 GHz) and Japan (59–66 GHz) [3]. By operating at high frequencies, 60-GHz radio allows for compact phased array antennae with beam forming and space-time coding. These techniques are being adopted in wireless multiple-input multiple-output (MIMO) systems, and they support Gbps applications in point-to-point links, wireless local area networks (WLANs), wireless personal area networks (WPANs), and those wireless networks with short-range and extraordinary capability [4]. Moreover, recent measurement results show that millimeter wave (mmWave) frequencies are feasible for mobile communications [5].

Besides bandwidth, high data rate multimedia applications in wireless communications also require high level of integration and complex functionalities. As such, sufficient bandwidth is only a necessary condition to enable the continuous prosperity of wireless communications, while the most important condition is to have low-cost, compact and low-power solutions that meet the market requirements. In the past, monolithic microwave integrated circuits (MMICs) have adopted III-V semiconductor technologies due to their superior performance compared to complementary metal oxide semiconductor (CMOS). For example, III-V semiconductor technology possesses higher electron mobility, higher

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breakdown voltage and the availability of high quality-of-factor (Q) passives [3]. However, continuous scaling-down of CMOS technology enables unity-current-gain frequency (f_T) and maximum oscillation frequency (f_{MAX}) to exceed 246 GHz [6] and 500 GHz [7], respectively. Furthermore, the most attractive feature of CMOS technology is that it promises higher level of integration and thus better cost reduction [3]. Now it is possible to integrate radio-frequency (RF), intermediate-frequency (IF) and baseband digital signal processing (DSP) blocks on the same die to enable true system-on-chip (SOC) at low cost for WLAN and WPAN applications operating at tens of gigahertz frequency range [8].

The difficulty of integrating various RF components in a single chip is dependent on the wireless technology requirements. As aforementioned, 60-GHz radio is considered as the most promising wireless technology to realize Gbps data links and thus researchers strive to design and develop CMOS circuits for microwave and mmWave applications [9]. Most work in the literature focused on power amplifier (PA) [10], transmit/receive switch [11] and low noise amplifier (LNA). In this paper, we focus on the design of CMOS LNA for microwave and mmWave applications.

The rest of this paper is organized as follows. Section 2 revisits the fundamentals of an LNA, including its function, performance metrics and device circuit models. Section 3 discusses the LNA topologies and Section 4 reviews various design techniques reported for LNAs. In Section 5, we compare different techniques and suggest recommendations on LNA design for future development of wireless radio circuits. Finally, Section 6 concludes the paper with a brief snapshot of our future work on CMOS LNA designs.

2. FUNDAMENTALS OF LNAS

As shown in Figure 1, a typical RF receiver will first pass the received signal from the antenna to the bandpass filter (BPF) and then the LNA. The signal entering the LNA is usually very weak and mixed with noise. Per Frris' formula for noise figure (NF), the first few stages of the receiver will dominate its overall NF. Consequently, LNA plays an important role in amplifying the received signal while suppressing noise for the subsequent stages by a factor of the gain of the LNA. However, the noise generated by the LNA itself is injected directly into the received signal. Hence, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible, enabling the retrieval of information signal in subsequent stages in the receiver [12].

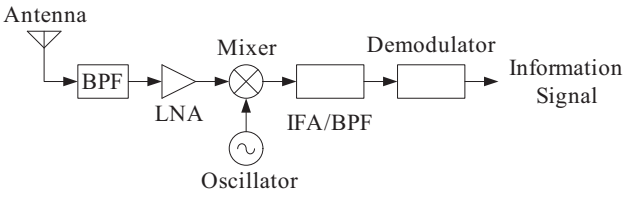

Figure 1. Block diagram of a typical RF receiver.

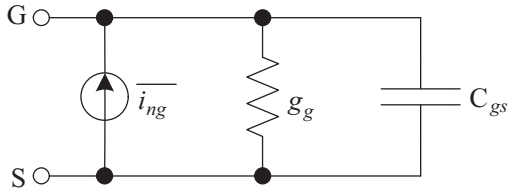

Figure 2. Gate noise model for MOSFETs.

2.1. Performance Metrics

Various performance metrics are considered in the design of an LNA, which usually include power gain (G), NF, linearity, stability, impedance matching and power dissipation (P_{diss}).

Power gain is a measure of the ability of an LNA to amplify signal power, which is measured by the ratio of output signal power to input signal power. Power gain is usually defined on a logarithmic scale in terms of decibel (dB).

NF presents a measure of the degradation in signal-to-noise-ratio (SNR) that an LNA introduces in the RF signal chain of a receiver. Particularly, NF is noise factor in decibel, which is defined as the ratio of the output noise power to the portion thereof attributable to thermal noise in the input termination at standard noise temperature T_0 (usually 290 K).

Linearity of an LNA refers to the capability of increasing the power level of input signals without otherwise altering the content of the signal. The most commonly used measures of linearity are 1-dB

compression point ($P_{1\,\mathrm{dB}}$) and input referred third order intercept point (IIP3). $P_{1\,\mathrm{dB}}$ is defined as the input power that causes a 1 dB drop in the linear gain due to device saturation. Noteworthily, IIP3 is a purely mathematical concept based on the assumption that the nonlinearity of an LNA could be modeled using a low-order polynomial. IIP3 is defined as the input power at which the amplitude of the third-order intermodulation (IM3) term is equal to the amplitude of the linear fundamental term. In addition, IIP3 probably lies beyond the damage threshold of the LNA.

Unconditional stability is critical to ensure that an LNA does not oscillate at any frequency with whatever source and load impedances. Theoretically, if both input and output impedance of an LNA have positive real part for any condition, this LNA is unconditionally stable. In the perspective of power flow, the reflected power is always less than the incident power, thus there is no extra power flowing back to the source from the LNA. Importantly, S-parameter can be used to determine the stability of an LNA. Equations (1) and (2) are widely used methods in many simulation tools to justify the stability of an LNA design. The stability factor K alone is not sufficient for the judgment and the necessary and sufficient conditions for the unconditional stable LNA are formed together with the auxiliary condition of B_1.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}|\,|S_{21}|} > 1 \tag{1}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \tag{2}$$

where $\Delta = S_{11}S_{22} + S_{12}S_{21}$, based on S-parameters.

Impedance matching refers to the requirement that an LNA should present a specific amount of impedance (e.g., 50 Ω) to the input source and the output load. In particular, if the LNA is preceded by a passive filter, such as the BPF in Figure 1, input impedance matching at the LNA is especially important because the transfer characteristics of many filters are rather sensitive to the quality of the termination [13]. Input/output impedance matching is usually measured with S_{11}/S_{22} parameters by considering an LNA as a two-port network.

Power dissipation is the amount of power drawn from the DC power supply by an LNA, and it is usually defined in dBm.

2.2. Device Models

The crucial requirement of designing a good LNA is to ensure that it adds as little noise as possible to the weak input signal, while providing enough gain for the components in the subsequent stages of a receiver to recognize the desired signal. This is true because the noise added by the LNA may overwhelm any benefits from its gain. It has to amplify a weak signal associated with random noise, which may be captured by the antenna and/or the BPF within the bandwidth of interest. Therefore, it is worth reviewing the major noise sources in a metal-oxide-semiconductor field effect transistor (MOSFET) before we discuss LNA design techniques.

Among those known noise sources, thermal noise is the well-studied one. For a given resistance R over the bandwidth Δf at a temperature T, the mean-square short-circuit noise current is calculated as

$$\overline{i_n^2} = 4kTG\Delta f, \quad \text{where } G = 1/R \tag{3}$$

As MOSFETs are essentially voltage-controlled resistors, they also exhibit thermal noise. Theoretical derivation of the drain current noise of MOSFETs can be expressed as

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \tag{4}$$

where g_{d0} is the drain-source conductance at zero Drain-Source Voltage (V_{DS}). In particular, $\gamma = 1$ when $V_{\mathrm{DS}} = 0\,\mathrm{V}$. As shown in Figure 2, the gate noise current can be expressed as

$$\overline{i_{ng}^2} = 4kT\delta g_g\Delta f \tag{5}$$

where $g_g = \omega^2 C_{gs}^2/5g_{d0}$ and δ is the gate noise coefficient, which has a value of 4/3 for long-channel devices [14].

The next type of noise is flicker noise, also known as $1/f$ noise or pink noise. It has been observed in all kinds of devices, and the fundamental physical mechanism behind is yet to find. Among all active

semiconductor devices, MOSFETs unfortunately have the highest flicker noise because of their surface conduction mechanism.

Other noise sources include: (1) short noise, which is associated with the leakage current of the drain-source diodes; (2) generation-recombination noise, which is caused by the statistical generation and recombination of charge carriers; (3) burst noise, also known as popcorn noise, consists of sudden step-like transitions between multiple discrete voltage or current levels. If it is hooked up to an audio speaker, it sounds like popcorn popping.

3. LNA TOPOLOGIES

For a MOSFET, detailed derivation shows that the source impedance that yields minimum NF is inductive in character [13]. However, as aforementioned, it remains a critical task in LNA designs to realize impedance matching at the input port by presenting a resistive impedance (e.g., $50\,\Omega$). Although one straightforward approach is using shunt-resistor like R_1 at the input port of a common-source (CS) LNA as shown in Figure 3, R_1 unfortunately adds its own thermal noise to the signal path, while attenuating the input signal ahead of the transistor, M. The combination of these two effects generally produces an unacceptably high NF.

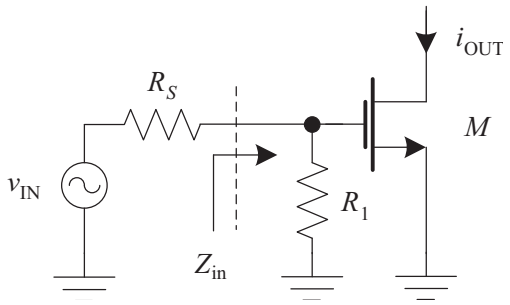

Figure 3. CS LNA topology with shunt input resistor.

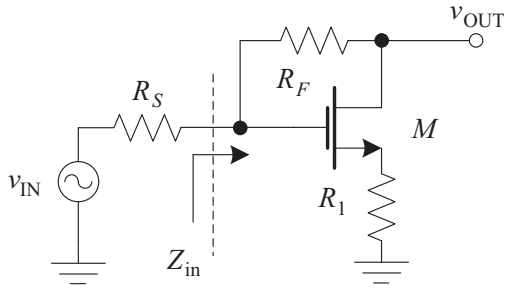

Figure 4. Shunt-series CS LNA topology.

Next, one may use the shunt-series LNA topology as shown in Figure 4. It makes use of resistive feedback in order to provide a broadband real input impedance though the resultant NF is larger than the minimum one.

3.1. Common-Gate LNA Topology

As shown in Figure 5, another method is to use a common-gate (CG) configuration. The rationale behind CG topology is that the input impedance is

$$Z_{in} = \frac{1}{sC_{gs} + g_m} \approx \frac{1}{g_m} \tag{6}$$

where g_m and C_{gs} are the transconductance and gate-source parasitic capacitance of transistor M, respectively. The resistance looking into the source terminal is resistive due to channel resistance, thus we can achieve input impedance matching by selecting proper device size and bias current.

3.2. CS LNA Topology with Inductive Degeneration

All the preceding LNA topologies discussed above suffer NF degradation due to the presence of noise resistances in the signal path. Interestingly, we are able to provide a resistive input impedance without resistors by enhancing the effect that the impedance, looking into the gate of a practical MOSFET, must possess a resistive term [13]. As such, inductive source degeneration is widely used to control over the real part of the input impedance by varying the inductance.

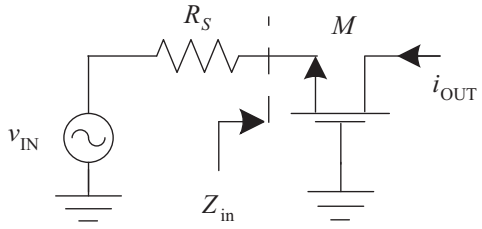

Figure 5. CG LNA topology.

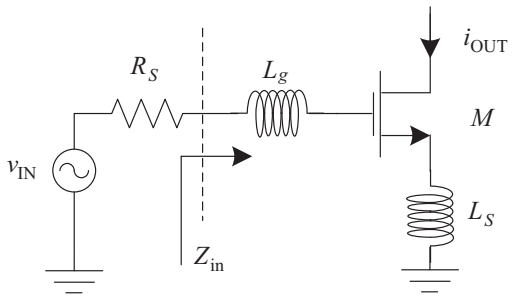

Figure 6. CS LNA topology with inductive degeneration.

Figure 6 shows the CS topology with inductive degeneration. In particular, the inductive degeneration due to L_s is ideally noiseless and the input signal is pre-amplified by the input matching series resonant network. From Figure 6, it is not difficult to show that

$$Z_{in} = s\left(L_g + L_s\right) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s \approx s\left(L_g + L_s\right) + \frac{1}{sC_{gs}} + \omega_T L_s \tag{7}$$

where $\omega_T = 2\pi f_T$ is the unity-current-gain angular frequency. Hence, we can choose appropriate value of L_s and L_g to resonate with C_{gs} at the operating frequency f with $(g_m L_s/C_{gs})$ set to R_S.

3.3. Cascode LNA Topology

CS LNA topology is popular due to its superior noise performance. However, it suffers from degraded reverse isolation and stability due to the fact that C_{gd} provides a feed-forward path between input and output. On the contrary, CG LNA topology exhibits better reverse isolation and stability, as well as to provide a wideband input match that is not sensitive to input parasitic capacitance [15]. Nevertheless, many LNA designs feature a cascode configuration as shown in Figure 7. This topology improves the isolation between input and output port, thus simplifying required matching networks. Furthermore, it also improves the gain at the expense of increased power consumption and noise. Notice that cascode LNA topology adopts current-sharing in nature, which allows for high gain without significant increase in power dissipation [16].

Other features of cascode LNA topology include high output impedance, and that the voltage gain of the overall topology is the same as the gain of the CS stage.

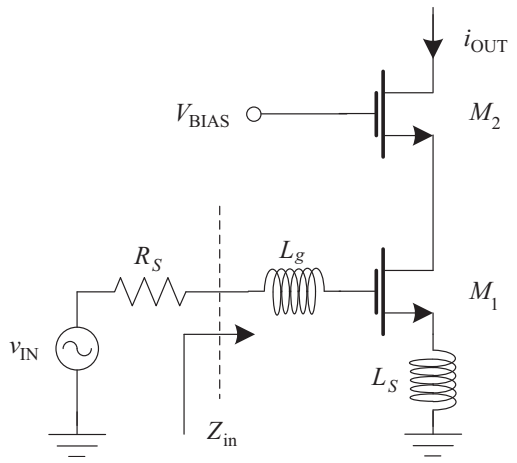

Figure 7. Cascode LNA topology.

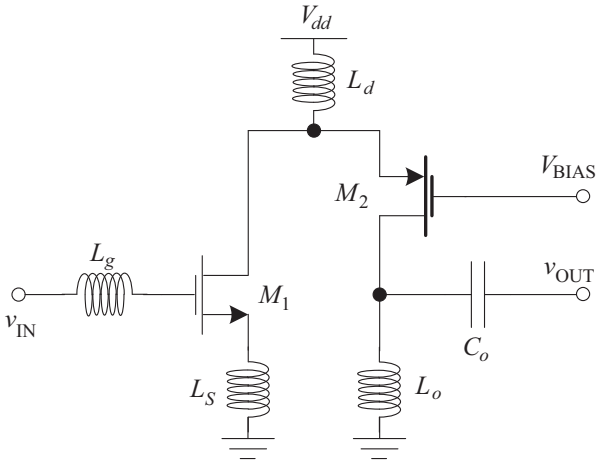

Figure 8. Folded cascode LNA topology [18].

It is worth mentioning that multicascode topology is also possible [17]. Higher order of cascode topology will provide higher gain at the expense of more parasitic capacitances.

3.4. Folded Cascode LNA Topology

Based on the cascode LNA topology, one can extend the cutoff frequency of the CS transistor, M_1, by folding the CG transistor, M_2. This leads to the folded cascode LNA topology as shown in Figure 8 [18].

Another advantage of the folded cascode LNA topology is that those parasitic capacitances at the drain node of M_1 can easily be eliminated by the resonance with the inductance L_d at the power supply pin. This is very important because the elimination/reduction of those parasitic capacitances will help to suppress the noise contribution of M_2 at the output and avoid the signal loss into the silicon substrate [19].

3.5. Differential LNA Topology

LNA designs using single-ended signaling usually result in smaller chip size than those using differential signaling. However, single-ended signaling suffers parasitic ground inductance that will usually cause considerable degradation in the performance of an LNA. On the contrary, differential signaling is able to reduce the second-order distortion and reject common-mode noise. Therefore, differential LNA topologies are nearly immune to stability problems or performance degradation caused by parasitic feedback loops. Moreover, differential LNA output is desired when connecting with Gilbert-type mixer cells.

There are two types of differential LNA topology — single-to-differential topology and fully differential topology. Figure 9 illustrates a single-to-differential LNA topology designed for a digital TV tuner.

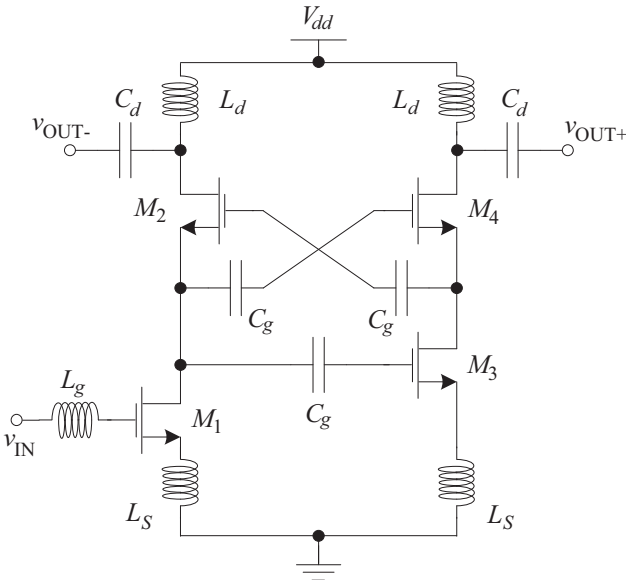

Figure 9. Single-ended input to differential output LNA topology [20].

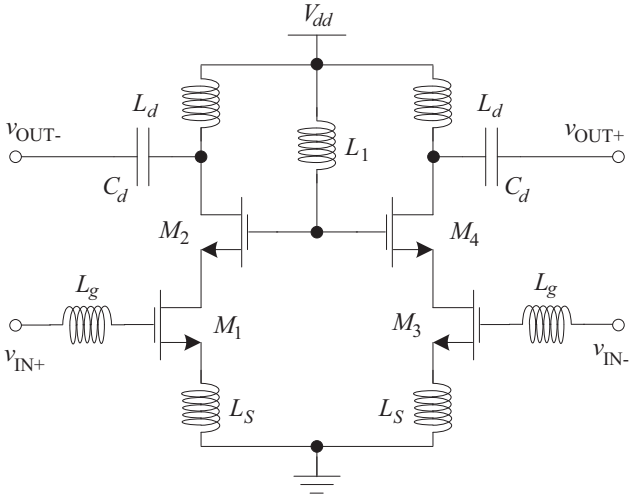

Figure 10. Fully-differential LNA topology [24].

Compared with single-to-differential LNA topology, fully differential LNA topology, shown in Figure 10, is more widely adopted due to its better stability [21].

Note that a fully-differential LNA exhibits higher noise factor than its single-ended counterpart for equal amount of power consumption [22]. Furthermore, it also costs twice the silicon area [23].

4. LNA DESIGN TECHNIQUES AND CONCEPTS

LNA designs involve the tradeoff between various performance metrics such as noise figure, gain, linearity, power dissipation and input/output impedance matching. In general, it is desired to have low noise figure, high gain, adequate linearity, low power dissipation and good impedance matching. In the following, we start the discussion of LNA designs with noise matching techniques, followed by noise reduction techniques, then impedance matching techniques, gain-enhancement techniques, power dissipation reduction techniques and wideband design techniques. Finally, we discuss LNA design techniques with process technologies.

4.1. Noise Matching Techniques

Noise matching focuses on how to present the necessary impedance such that minimum noise factor can be achieved.

4.1.1. Classical Noise Matching

Classical noise matching (CNM) technique can be used to achieve a noise factor equal to $F_{\min}$ of the transistor, which is the lowest noise factor for a given technology [25]. As shown in Figure 11(a), the key idea behind CNM is to achieve $F_{\min}$ by presenting the optimum noise impedance Z_{opt} by adding an input matching network. Figure 11(b) shows the small signal equivalent circuit of the CS sub-stage.

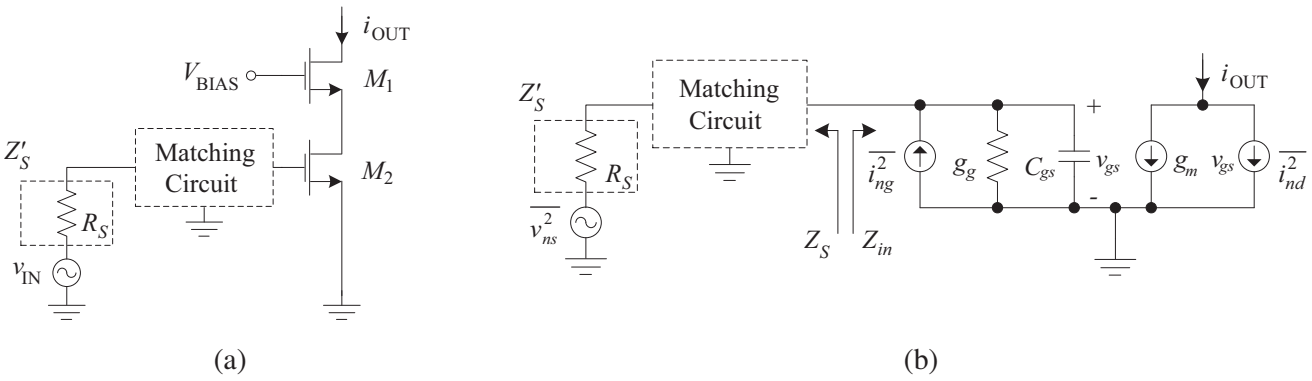

Figure 11. (a) CS LNA topology with CNM and (b) its small signal equivalent circuit.

However, a significant gain mismatch is expected in an LNA designed with CNM technique because of the inherent mismatch between Z_{opt} and Z_{in}^*, where Z_{in}^* is the complex conjugate of input impedance of the LNA [18]. Consequently, CNM technique involves a performance tradeoff between the gain and the noise factor.

4.1.2. Simultaneous Noise and Input Matching

Based on the CNM technique, one can purposely shift the optimum noise impedance Z_{opt} to the desired point by adopting feedback techniques. For example, series feedback with inductive source degeneration was applied in simultaneous noise and input matching (SNIM) technique [26], as shown in Figure 12(a). From Figure 12(b), the condition for SNIM is

$$Z_{opt} = Z_{in}^* \tag{8}$$

Notice that minor mismatch in Z_{opt} would considerably degrade the noise performance of LNA while slight mismatch in Z_{in} has a negligible effect on the gain of LNA. This relaxation on input impedance matching has been considered in SNIM, which can be implemented by adding degeneration inductance L_s. In principle, SNIM can be achieved at any value of Z_S, especially when the design allows for larger transistor size, high power dissipation and high operating frequency [18].

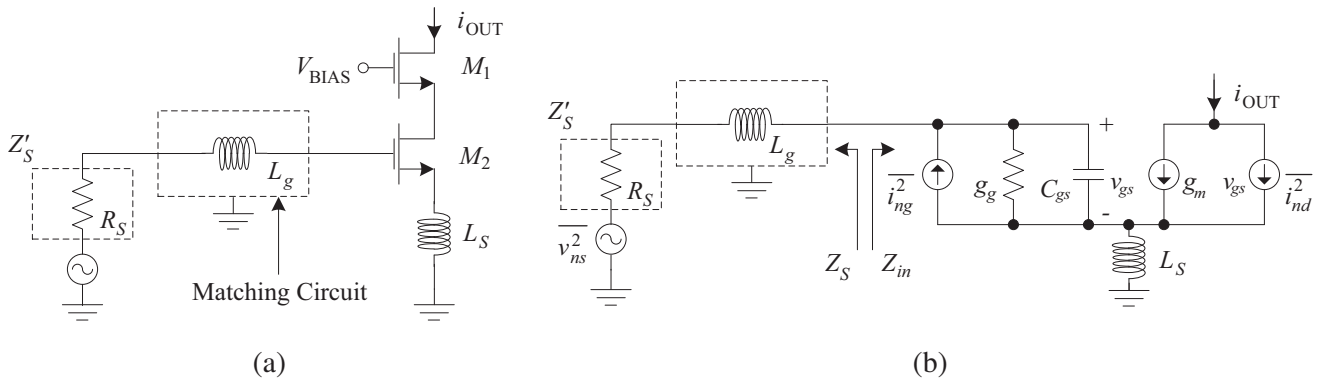

Figure 12. (a) Cascode LNA topology with SNIM and (b) its small-signal equivalent circuit.

The continued CMOS scaling down leads to ever-reducing transistor size, which poses a challenging problem for SNIM technique. With a small transistor, power constrained noise optimization (PCNO) technique can be applied and it results in an achievable minimum noise factor higher than $F_{\min}$ of the CS transistor, though input impedance matching can still be satisfied by choosing an appropriate degenerative inductance L_s [27]. PCNO technique might be considered as a compromised version of SNIM technique.

4.1.3. Power Constrained Simultaneous Noise and Input Matching

As we know, low-power implementation is an inevitable requirement for future radio transceiver design in spite of the fact that SNIM and PCNO techniques are not valid for low-power implementations. However, power constrained simultaneous noise and input matching (PCSNIM) [28] can be achieved by simply adding an capacitor, C_{ex}, between gate and source of the CG transistor, as shown in Figure 13.

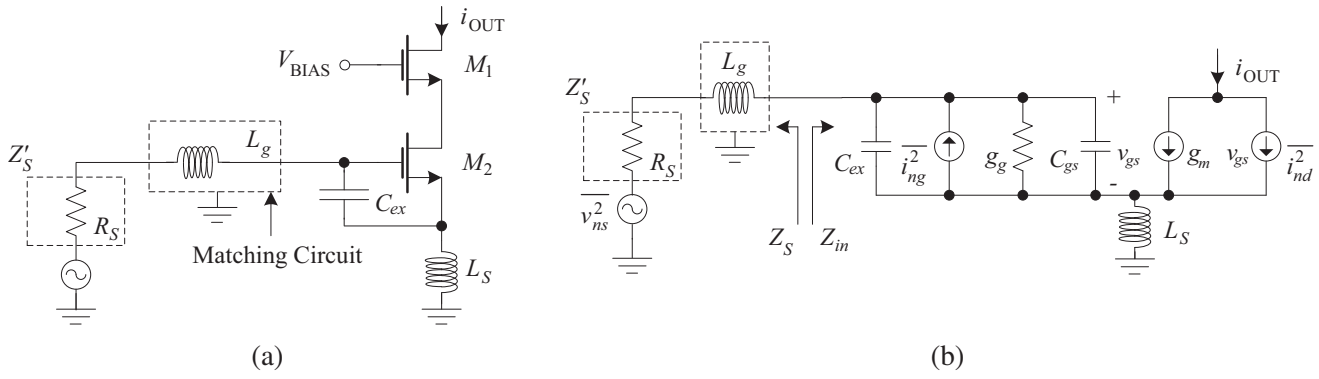

Figure 13. (a) Cascode LNA topology with PCSNIM and (b) its small-signal equivalent circuit.

Noteworthily, the addition of C_{ex} allows for simultaneous noise and input matching at any level of power dissipation provided that L_s is not very large. In particular, a tradeoff between the noise factor and the gain should be considered when selecting the values of C_{ex} and L_s. Too much L_s can lead to increased $F_{\min}$, while excessively large C_{ex} can result in reduced gain due to the degradation of the effective cutoff frequency of the composite transistor formed by M_2 and C_{ex} [18]. In addition, small transistor size and low power dissipation lead to very high noise resistance R_n that is mainly related to the transconductance g_m, leading to the major limitation of PCSNIM technique.

4.2. Noise Reduction Techniques

Noise reduction techniques attempt to bring down the lower bound of the achievable noise factor.

4.2.1. Capacitive Cross-Coupling Technique

Zhuo et al. proposed to use capacitive cross-coupling technique to improve the noise factor of a CG input stage of an LNA [29]. As shown in Figure 14, cross coupling causes the noise of transistor M_1 and M_2 to produce common-mode noise voltage at the output nodes d_1 and d_2, respectively. Rigorous small signal noise analysis shows that the noise factor is reduced to

$$F = 1 + \frac{\gamma}{2} \tag{9}$$

As we know, for a CG LNA, $F_{\min} = (1 + \gamma)$; thus, the capacitive cross-coupling technique can reduce the noise factor at the input stage.

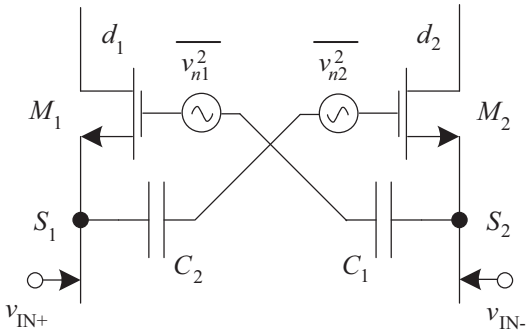

Figure 14. Capacitive cross-coupling technique [29].

Capacitive cross-coupling technique can be used together with a fully-differential topology to reduce noise factor [30, 31]. Fan et al. presented a similar design, in which capacitive cross-coupling was applied together with an additional inductor to reduce noise [32].

4.2.2. Resistive Feedthrough Technique

The CS LNA topology with inductive degeneration functions well in applications at low-gigahertz range. However, its performance degrades at higher frequencies when f becomes comparable to f_T. On the contrary, the noise and gain performance of CG LNA topology are independent of f, and this is desirable for high-frequency LNA designs. Theoretical analysis showed that the induced gate noise is essential in defining $F_{\min}$ [27]. Most analysis assumes the infinite transistor output resistance, r_{ds} and thus the noise factor of CG LNA has a lower bound of $(1+\gamma)$ for perfect input matching. Subsequently, it was noticed that finite r_{ds} of the input transistor could increase input impedance and allow us to design CG LNA with noise factor lower than the aforementioned bound [33]. Inspired by that fact, Guan and Hajimiri proposed a resistive feedthrough technique to bring the noise factor of a CG LNA to a significantly lower level [34]. The idea is to increase the transistor output resistance by adding an external resistor, R_p.

$F_{\min}$ of CG LNA with resistive feedthrough in Figure 15 is

$$F_{\min} \approx 1 + \frac{\gamma}{1 + g_{mb}/g_m}\left[\sqrt{\frac{4\delta}{5\gamma}}\frac{\omega}{\omega_T} + \frac{2}{5\,(1 + g_{mb}/g_m)}\frac{\omega^2}{\omega_T^2}\right] \tag{10}$$

At $f = 24\,\text{GHz}$, capacitive coupling and resistive loss through substrate would have considerable influence on the circuit performance. It was proposed to add a shunt inductor with a large bypass capacitor to eliminate the adverse effect by resonance [34].

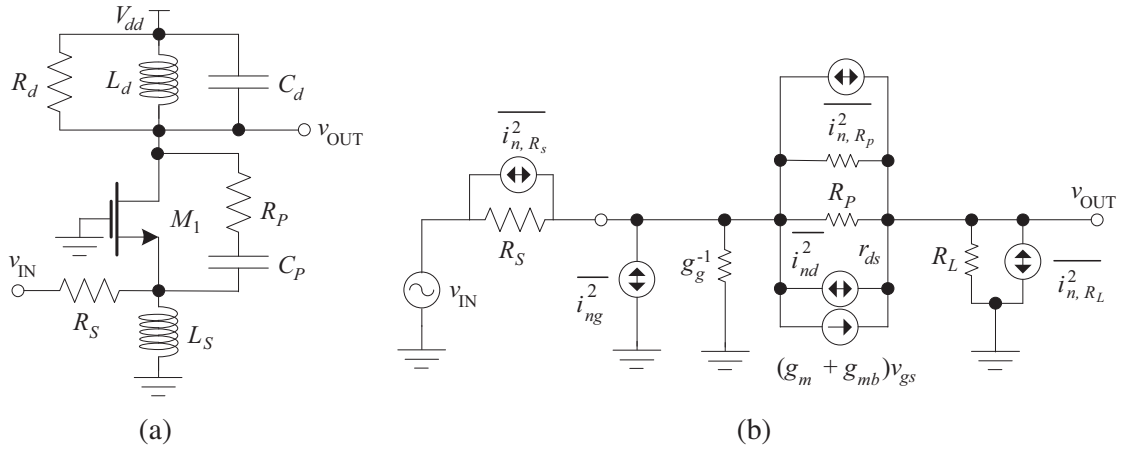

Figure 15. (a) CG LNA topology with resistive feedthrough and (b) its small signal equivalent circuits [34].

4.2.3. G_m-Boosted CG LNA

The CG LNA topology realizes resistive input impedance matching as $1/g_m$ (See Eq. (6)), and its noise factor is limited by

$$F_{\text{CG-LNA}} = 1 + \frac{\gamma}{\alpha g_m R_S} \tag{11}$$

where α and γ are empirical process-dependent and bias-dependent parameters, respectively. It is not feasible to reduce noise factor by arbitrarily increasing g_m because $g_m R_S = 1$, which is constrained by the input impedance matching condition. However, if we can tolerate some input impedance mismatch, we can increase g_m to decrease the noise factor. For example, as shown in Figure 16, Allstot et al. proposed to boost the effective transconductance G_m while keeping the intrinsic transconductance g_m [15].

By introducing an inverting amplification between the gate and source terminal of the transistor M, G_m is boosted from g_m to $(1 + A)g_m$, where A is the gain from source to gate. Then, the noise factor of the LNA is

$$F_{\text{CG-LNA},G_m\text{-Boosted}} = 1 + \frac{\gamma}{\alpha(1 + A)^2 g_m R_S} \tag{12}$$

As input matching requires that $(1 + A)g_m R_S = 1$, the noise factor is effectively reduced by a factor of $(1 + A)$. To realize the inverting gain A, one may adopt the capacitor cross-coupling technique proposed in [29]. However, the gain A is always less than unity due to the capacitor divider between C_{gs} and coupling capacitance C_C. Li et al. proposed a transformer-coupling technique to realize an greater-than-unity inverting gain A for G_m-boosted CG LNA [23].

As shown in Figure 17, a transformer T_1 is used to effectively enhance the transconductance at the source of transistor M_1. Detailed analysis on input impedance of the LNA showed that the impedance can be viewed as a parallel-resonant RLC circuit, and the inverting gain factor is $A = nk$, where n is the turns ratio, $n = \sqrt{L_S/L_P}$ and k is the coupling coefficient, $k = M/\sqrt{L_P L_S}$. L_P and L_S are the inductance of primary inductor and secondary inductor, respectively; M is the mutual inductance. The noise factor is essentially reduced to

$$F \approx 1 + \left.\frac{\gamma}{\alpha(1 + nk)}\right|_{(1+nk)g_m R_S = 1} \tag{13}$$

Assuming $k = 1$ (ideal coupling coefficient) and taking induced gate noise into account, one may derive F as

$$F = 1 + \frac{\gamma}{\alpha\,(1 + n)} + \frac{\delta\alpha}{5}\left(\frac{\omega}{\omega_T}\right)^2 (1 + n) \tag{14}$$

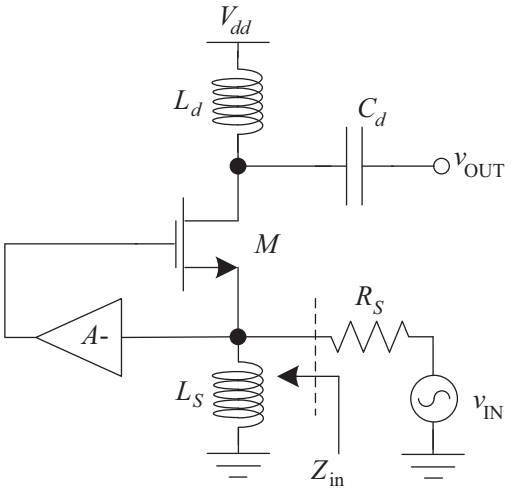

Figure 16. G_m-boosted common-gate LNA [15].

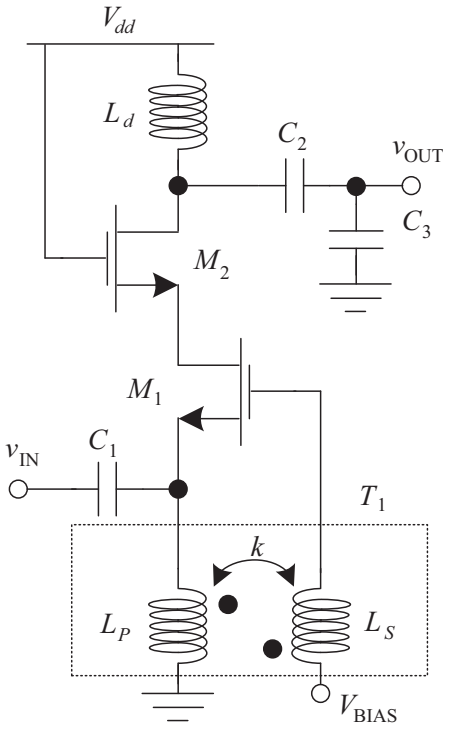

Figure 17. Transformer-coupled G_m-boosted CG LNA [23].

As can be seen from Eq. (14), g_m boosted by transform coupling has the following effects on F: (1) the channel noise is reduced by $(1 + n)$; (2) the induced gate noise is increased by the same factor. Noteworthily, practical constraints like non-idealities associated with on-chip transformer and parasitic impedance at the gate will limit the value of A between 2 and 3 [23].

4.3. Impedance Matching Techniques

Impedance matching is required in RF circuits to provide the maximum power transfer from a source to its load. For LNAs, impedance matching serves for two purposes, i.e., maximum power transfer (*power matching*) and minimum noise factor (*noise matching*) [35]. As the input signal level to an LNA is usually extremely small, any unnecessary power loss in the circuit cannot be tolerated. We have discussed the noise matching techniques above, thus we focus on power matching in this subsection.

For impedance matching, the maximum transfer of power happens when the load impedance is equal to the complex conjugate of the source impedance. Thus, the objective of any impedance matching technique to ensure the load impedance to be equal or close to the complex conjugate of the source impedance [36]. Furthermore, the perfect impedance matching happens only at one particular frequency. At all other frequencies, the matching becomes progressively worse and eventually non-existent.

Impedance matching is required at both the input and output of an LNA. In the literature, most papers focused on input impedance matching while leaving output impedance matching to the subsequent component after the LNA in the receiver chain. Furthermore, each matching element will contribute certain signal losses, directly leading to an increase in the noise figure. Thus, a simple impedance matching network will have better noise performance than its complex counterpart, although it is sometimes unavoidable to use multistage impedance transformers for specific purpose, such as broadening the input signal bandwidth.

When complex impedances are present, especially with parastitics, the two fundamental techniques in designing matching networks are *absorption* and *resonance* [36]. By *absorption*, element capacitors are placed in parallel with stray capacitances and element inductors are placed in series with stray

inductances. Then, the stray components values are subtracted from the calculated element values. By *resonance*, opposite reactance is added to resonate any stray reactance at the frequency of interest. Then, the matching network can be designed for the remaining pure resistances.

For the implementation of impedance matching for LNAs, we usually adopt two basic approaches, namely lumped element and transmission line. The former results in smaller dimensions and high Q, but being more susceptible to coupling that may cause discrepancies between design and actual performance; while the latter has mature EM environment and analytic solutions to support fast design at the expense of chip area. Furthermore, lumped R, L and C elements can be used at frequencies up to 60 GHz, if the condition that $\ell < \lambda/10$ is satisfied, where ℓ and λ are the length of the component and the wavelength, respectively. However, a proper design should consider the modeling of undesirable effects such as parasitics, spurious resonances, fringing fields, loss, and perturbations caused by a ground plane. Smaller values of R, L and C should be implemented using transmission line [35].

4.3.1. Lumped Element Approach

Impedance matching network can be done using one, two or multiple reactive lumped elements [35]. As shown in Figures 18(a) and (b), the simplest type of matching network is the L-type network, which uses two reactive elements to match any load impedance to a given source impedance. If three reactive elements are adopted, they can be arranged in T-type network or π-type network as shown in Figures 18(c) and (d), respectively.

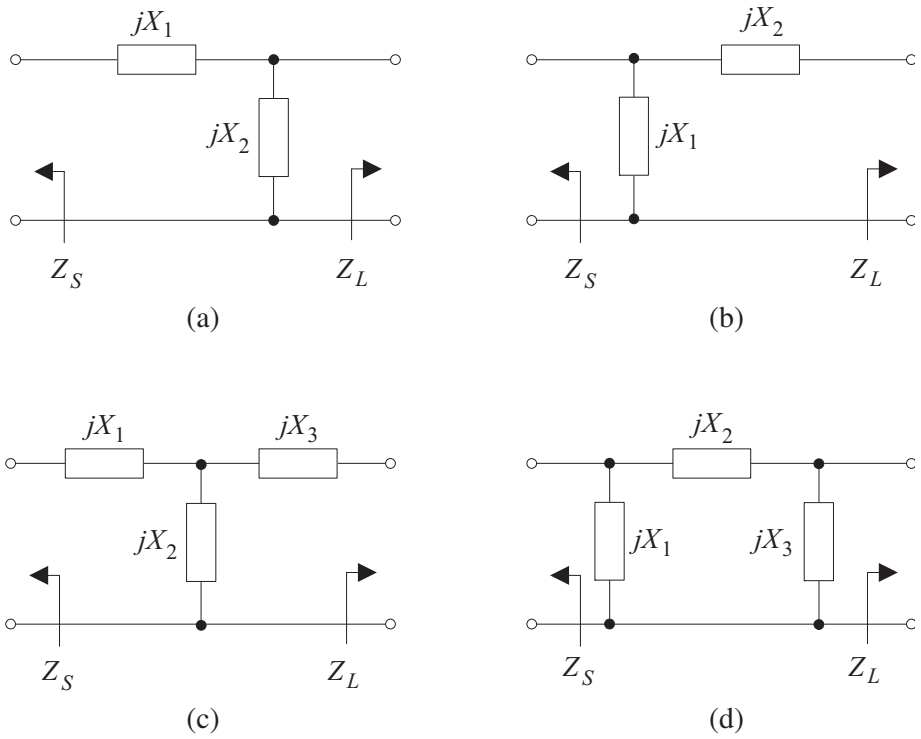

Figure 18. (a) L-type matching network A; (b) L-type matching network B; (c) T-type matching network; (d) π-type matching network.

For example, on-chip inductors usually have low Q and undesired noise contribution to LNAs. Gramegna et al. reported a single-stage cascode LNA design using on-chip inductors (with Q of 8–10) and their design achieved a NF of 1.05 dB at $f = 900$ MHz [19]. Stubbe et al. proposed to use external inductors with higher Q to reduce their noise contribution [26]. Furthermore, as per *absorption* technique, it is convenient to use those unavoidable pad, pin and electrostatic discharge (ESD) protection [37] diode capacitance as part of impedance matching network.

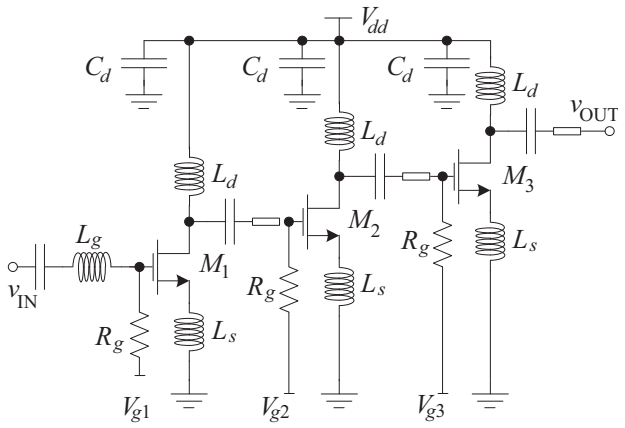

Figure 19. 3-stage CS LNA with input inductor [38].

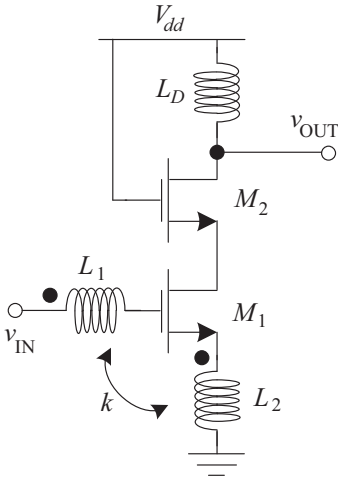

Figure 20. Transformer-based input matching LNA [48].

As shown in Figure 19, Cohen et al. proposed a CS LNA design with lumped inductors for 60-GHz applications [38], in which series coplanar inductor matching was adopted. Kunze et al. reported a similar LNA design for 60-GHz application with a compact size [39]. Their design adopted a three-stage cascode topology, and one-turn spiral inductors were used as impedance matching networks together with the parasitics of transistors.

4.3.2. Transmission Line Approach

Transmission line is usually adopted as input/output matching networks for LNA designs to achieve a wideband, flat gain [40, 41]. Loss reduction in transmission lines contributes to the reduction of noise factor of an LNA. Single-stub impedance matching is a popular technique, which uses a single open-circuited or short circuited length of transmission line connected either in parallel or in series with the transmission feed line at a certain distance from the load. This technique can be extended to double-stub impedance matching [35]. The quarter-wave transformer can be used to match a real load impedance to a transmission line. Single or multiple sections of quarter-wave transformer designs can be adopted to present optimum matching characteristics over a desired frequency band. For example, Mitomo et al. presented a three-stage cascode fully-differential LNA design for a 60-GHz receiver [42], in which the matching networks were implemented using short stubs as inductors.

Microstrip line is the most popular type of planar transmission lines, and one can easily look up its formulas on effective dielectric constant and characteristic impedance in the literature. In order to reduce the circuit size, microstrip line can be folded [43] and/or organized into hair-pin structures [44]. Razavi proposed folded microstrip technique and used it in a 60-GHz cascode LNA design [43]. The folded microstrip line was realized as a metal 8 signal line over a metal 1 ground plane with its two ends close to each other. Similarly, Kang et al. presented a 60-GHz three-stage cascode LNA design using *hair-pin type transmission line* to perform impedance matching in order to reduce chip size [44]. In addition, folded (or meandering) microstrip line technique and current-sharing technique [16] were combined together in an LNA design in [45], which was of a four-stage topology with the first three stages in CS configuration and the last stage in cascode configuration.

Coplanar waveguide is another popular type of transmission because of its easy fabrication process — both the signal line and the ground are in the same plane. Kanaya et al. studied on-chip impedance matching using CPW [46]. The CPW lines were designed using meander structures to reduce the chip size. Furthermore, the use of vertical planar waveguide (VPW) can enable us to mitigate the challenges such as design rule limitations regarding the minimum spacing between metals and the metal minimum-width, which are imposed on conventional CPW or microstrip lines. Haroun et al. proposed to use vertical planar waveguide for matching networks [47] and provided a single-stage cascode LNA design for 60-GHz applications.

4.3.3. Transformer Based Impedance Matching

Conventional source inductive degeneration method forms a feedback that leads to lower dynamic range of v_{gs}, thus reduces the overall cascode gain. Nevertheless, a transformer can be adopted to achieve the same input impedance matching [48]. As shown in Figure 20, the primary spiral L_1 of a transformer is connected at the input of the circuit in series with the gate of the CS transistor, and the secondary spiral L_2 inserted between source and ground. The overall gain is increased by 3 dB because of the opposite phase created by the transformer effect between gate and source voltages.

The coupling effect of the transformer can be used to couple the RF input signal between CG devices in cascade structures to enhance the bandwidth of a wideband mmWave LNA [49]. In addition, as shown in Figure 21, multitap transformer can be used together with switches to design *reconfigurable multimode* LNAs [50]. In addition, by choosing different combinations of switches, the effective inductance at the input matching network can be varied, and thus the operating frequency can be changed.

Transformer can be used in feedback network to achieve wideband input matching [51]. In addition, a transformer feedbacked capacitor neutralizer was proposed to boost the gain of an LNA [52]. Furthermore, transformers can be used as balun-based matching networks. A 60-GHz LNA design in single-to-differential topology was proposed in [53]. As shown in Figure 22, the design consists of two cascode stages and an output buffer. A balun-based matching network using a transformer was inserted between stage 1 and stage 2. Another transformer, with two center-tapped turns in a stacked configuration, was used as the matching network between stage 2 and output buffer. In their design,

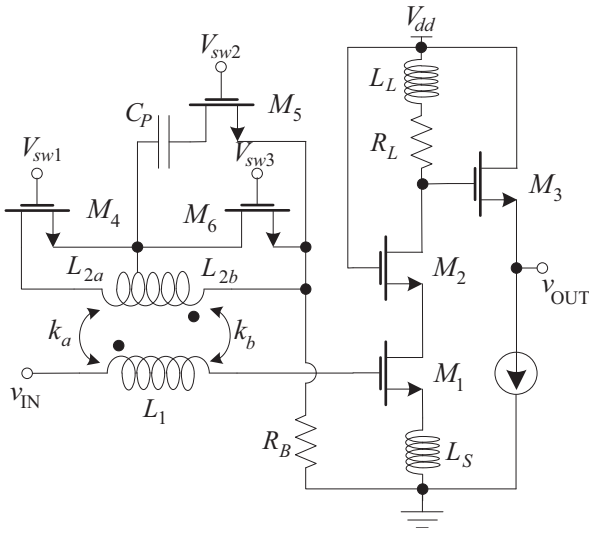

Figure 21. Transformer-based multimode LNA [50].

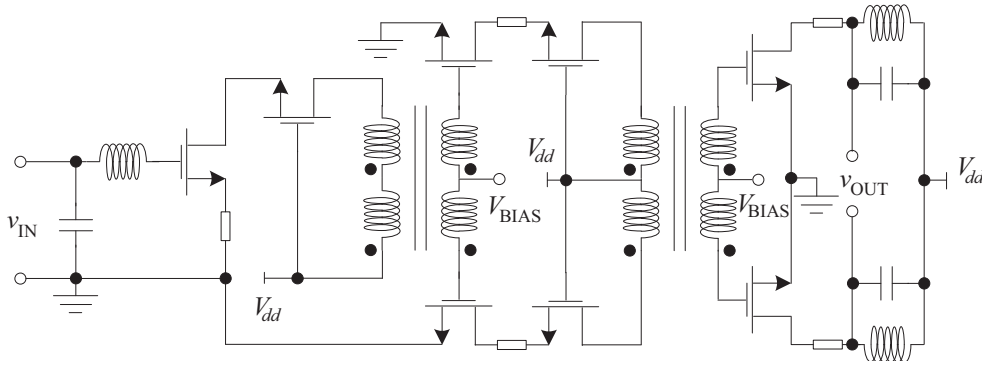

Figure 22. Simplified schematics of LNA [53].

the occupied chip area of spiral inductors with more than one turn were traded off for high Q and self-resonance frequency.

Lastly, typical LNA designs consider either single-ended input or differential input, and it is not common for an LNA design to support both single-end and differential input. Kuo et al. presented a wideband LNA design that supports both single-ended and differential inputs [54]. In addition, their compact-size design carried out the balun function in the single-ended operation mode, which eliminates the use of bulky transformer. The LNA topology is similar to that in [29], expect certain portion of bulky cross-coupling networks.

4.4. Gain Enhancement Techniques

As indicated in Frris' formula for noise factor, the gain of an LNA plays an important role in the overall noise performance of a receiver. The larger the gain, the less effect caused by those components followed by the LNA. Several techniques were considered to enhance the LNA gain.

4.4.1. Cascode LNA with Middle Inductor

Performance of a cascode LNA topology can be further improved by a middle inductor, which is placed in series between the CS and the CG transistors. The rationale behind this is to use the series inductor to tune out the middle pole of the cascode and to compensate for its lower f_T. This configuration was mentioned in [16], and the middle inductor was used as a choke to reduce DC voltage drop. Later, Yao et al. adopted this technique for a 60-GHz LNA design [55]. As shown in Figure 23, the series inductor L_M, forms an artificial transmission line with the gate-source and source-bulk capacitances of transistor M_2 and with the drain-bulk and gate-drain capacitance of transistor M_1. Importantly, they gave an algorithmic design methodology for CMOS cascode LNA design based on active device matching. With pre-calculated effective source resistance seen by the LNA across its bond pad, the methodology works for an inductively-loaded LNA. First, it sets the bias to a current density, J_{OPT}, which minimizes the transistor noise factor. Then, it chooses an optimum finger width, W_f, to maximize f_{MAX} and minimize the noise factor. Subsequently, the best L_M is obtained by maximizing f_T at the bias current density of J_{OPT}. After that, with all devices biased at J_{OPT}, it scales the number of fingers, N_f, and L_M to match the real part of optimal noise impedance, Z_{opt}, at the operating frequency. Next, it finds L_S, and adds L_G to tune out the imaginary parts of input impedance Z_{in} and optimal noise impedance Z_{opt}, respectively. Finally, it adds output matching network with inductive load to maximize the gain.

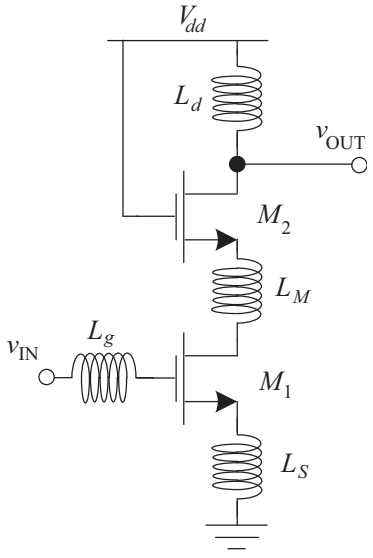

Figure 23. Cascode LNA with middle inductor [55].

Kraemer et al. presented a similar design using middle inductors together with the parasitics of transistors as artificial transmission lines [56], where lumped elements were employed exclusively. Their design features two-stage cascode topology and can be biased at two different supply voltages of 1.5 V and 1 V, respectively.

4.4.2. Negative Feedback

Negative feedback can be implemented through a resistive or active feedback network with a cascode topology to improve the LNA gain. As shown in Figure 24, active feedback provides better gain stability and requires smaller load resistance than resistive feedback, at the expense of increased design complexity. A single-to-differential topology with resistive feedback was proposed to increase the loop gain by double as compared to that of the conventional single-ended resistive feedback LNA through a source follower [57]. Their design can also reduce the NF and improve the linearity.

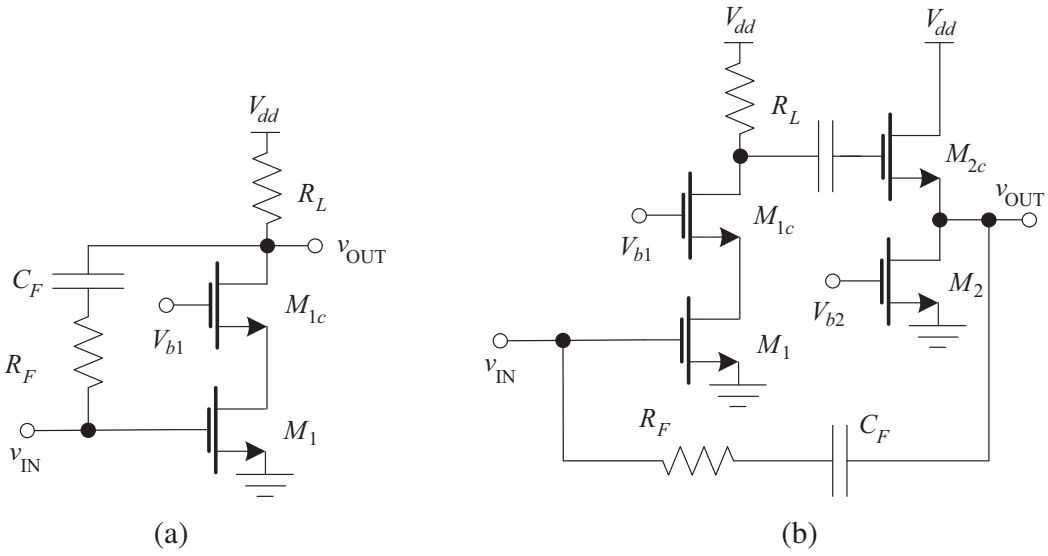

Figure 24. Negative feedback: (a) resistive feedback (b) active feedback [57].

4.4.3. Transformer Feedback

As shown in Figure 25, a transformer feedback g_m-boosting technique was proposed in an mmWave Cascode LNA design to increase the gain and reduce the noise [58]. Two designs were presented with impedance matching achieved by a transformer and transmission line, respectively.

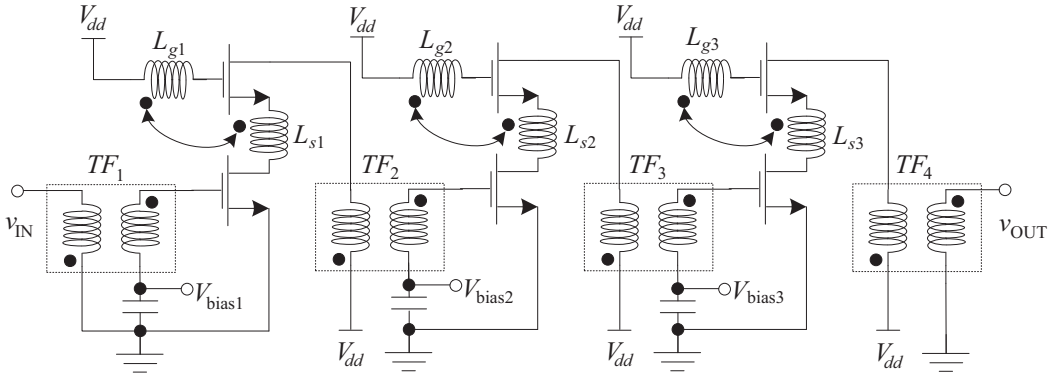

Figure 25. Transformer-based g_m-boosting LNA [58].

4.5. Power Dissipation Reduction

Power consumption is a critical issue in mobile devices as most of them are powered by batteries, or recently developed wireless power transfer and energy harvesting techniques. Therefore, it is desired to reduce the power consumption of a transceiver and prolong its operation time.

4.5.1. Current Reuse Technique

From Figure 6, the input can be matched to R_S by using inductors L_g and L_s. Under input matching condition, the noise factor, F, can be shown as

$$F \approx 1 + \left(8\omega^2 C_{gs}^2 R_S\right)/\left(3g_m\right) \tag{15}$$

In order to reduce F, Karanicolas proposed to increase g_m while keeping drain current at an reasonable level by applying current reuse technique [59]. As shown in Figure 26, the main idea of current reuse technique is to achieve g_m and ω_T of a single device with less current. With an appropriate aspect ratio, the compound device in Figure 26(b) can have the same transconductance as the device in Figure 26(a). Furthermore, by substituting the device M_2 in Figure 26(b) with a p-channel MOSFET (PMOS) device, we have a compound device in Figure 26(c), which has a transconductance that is nearly equal to that of the device in Figure 26(a) [59]. Thus, we can increase g_m while keeping the drain current manageable. In addition, single-stage LNAs have higher IIP3 than multi-stage LNAs at the expense of lower gain and worst reverse isolation [59].

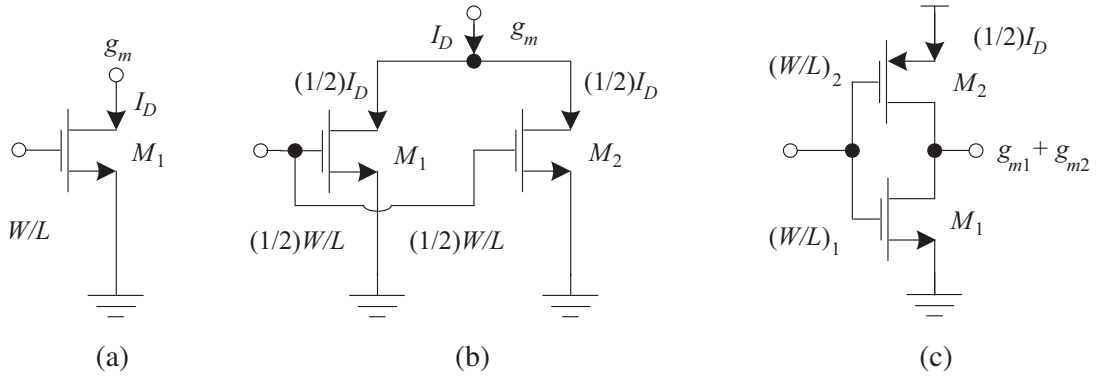

Figure 26. Illustration of current reuse technique [59].

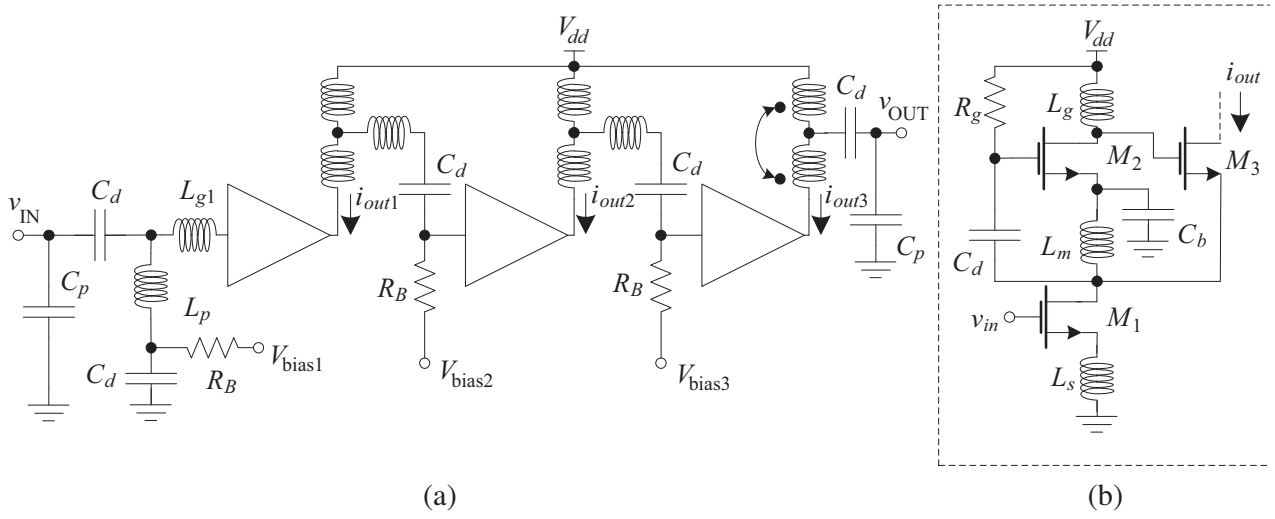

Figure 27. (a) Proposed LNA architecture. (b) Proposed transconductor [60].

Current reuse technique can be extended beyond the configuration using two transistors. As shown in Figure 27, Li et al. proposed a 60-GHz transconductor consisting of a CS transistor whose DC current is shared by other two transistors [60]. The modified cascade and current reuse CS-CS structure features both high equivalent transconductance and high output resistance at the expense of slightly deteriorated NF. Their LNA design achieved a NF of 6.1 dB with a power dissipation of 9.6 mW under 1 V power supply.

4.5.2. Forward Body Biasing

Forward body bias (FBB) technology can be applied to operate LNA at reduced supply voltage and low power consumption condition while providing sufficient gain [61]. With this technique, Lin et al. presented a three-stage CS LNA design [62], in which thin-film microstrip (TFMS) lines were used for matching networks and interconnects.

Parvizi et al. proposed to apply FBB to mitigate output conductance degradation due to short channel effects in ultra-low voltage (ULV)/ultra-low power (ULP) applications [63]. As shown in Figure 28, current reuse was also applied in CG transistors with active shunt-feedback structure for input matching. The design worked well with a low power supply of 0.5 V at 500 μA current. Even when the power supply dropped to 0.4 V, the design maintained good performance. They also presented another design using the same technique for applications in 0.1–2.2 GHz with a 1 V power supply [64].

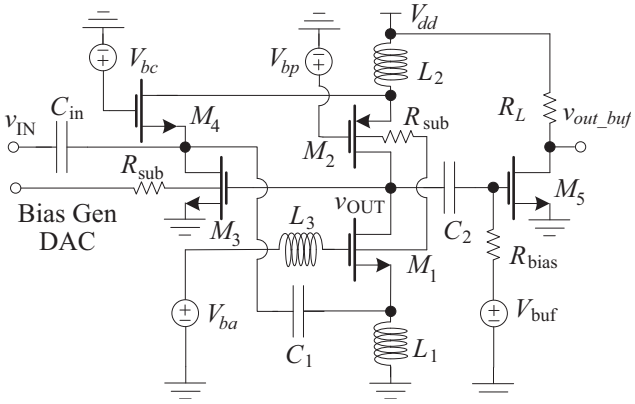

Figure 28. LNA with forward body bias [63].

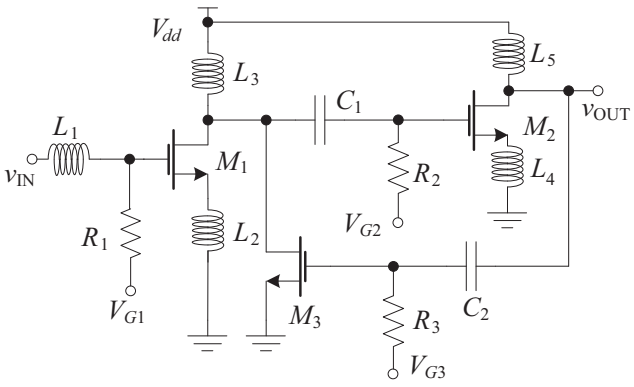

Figure 29. LNA with positive feedback [65].

4.5.3. Positive Feedback

As shown in Figure 29, Lai et al. proposed to apply positive feedback to enhance the gain within the operating band [65]. In addition, low power consumption was achieved by biasing the transistors in the moderate inversion region.

4.6. Wideband LNA Design

With the evolution of wireless standards, some radio front-ends require wideband operations, such as ultra wideband (UWB), cognitive radio (CR) [66] and software defined radio (SDR) [67]. Consequently, a wideband LNA is required. Different LNA topologies have been studied for wideband operations [51]. Wideband LNAs usually adopt distributed architecture and multi-stage topologies. The former results in high power consumption and large chip size [68]; the latter has a limited bandwidth due to intrinsic capacitances of transistors and other parasitic capacitances [69].

Distributed LNA topology [70] can achieve both broadband input matching and high gain, but requires large chip area and high power consumption due to the use of several spiral inductors and transmission lines. CG LNA can provide broadband input matching [71], but it requires high power consumption. In addition, CG LNA with switchable inductor [72] or inductive peaking

techniques [71, 73] could fulfill the UWB operation requirement. The NF of CG LNA is usually $2.2 \sim 3$ dB [74]. Interestingly, the conventional inductive source-degeneration topology is still applicable to marginally cover the band required [75].

For multi-stage LNAs, matching networks and inductive peaking techniques [73] are widely used to improve their bandwidth. Wideband input matching for the CS structure [76] usually adopts two methods: (1) resistive feedback, which requires a small chip area at the expense of extra nonlinearity; (2) BPF input matching network, which has limited nonlinearity influence, but requires a larger chip area. Matching networks can adopt four topologies, including L-type, π-type, T-type and combination of various types. They provide wideband matching at the expense of additional insertion loss and chip area. For example, Lu et al. reported a UWB LNA design using three-stage cascode topology with a CS follower as output buffer [77]. LC peaking and pre-compensation techniques were adopted to achieve wideband flat gain.

As shown in Figure 30, pole-converging was also proposed to be applied with negative drain-source transformer-feedback techniques to extend the bandwidth of a three-stage cascade LNA [69].

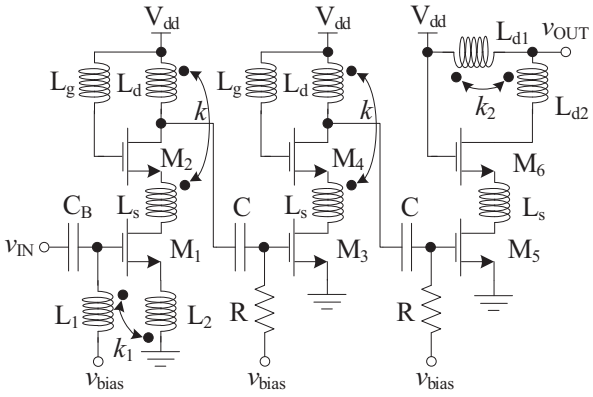

Figure 30. LNA with pole-converging technique [69].

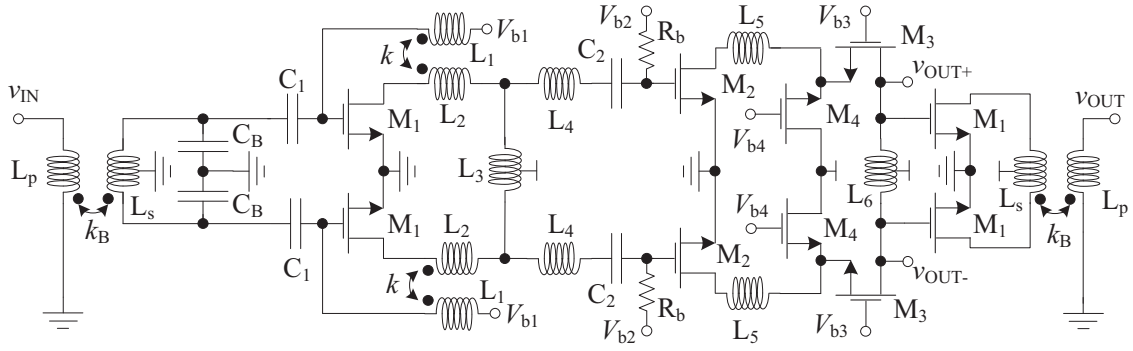

Figure 31. Proposed LNA with transformer feedback technique [51].

Various feedback techniques were investigated for wideband LNA designs: (1) negative feedback, (2) active feedback [64, 78], (3) resistive feedback [79, 80] and (4) reactive feedback (with magnetic coupling between the input MOSFET's gate and source through transformers) [81] can also achieve wideband operation. However, these techniques are not suitable for mmWave LNAs due to parasitics. As shown in Figure 31, transformer feedback can be adopted to improve the performance [51, 82].

Wideband LNA designs usually suffer from low linearity in terms of IIP3 [83]. Manstretta proposed a technique to increase the linearity by using two parallel forward paths for amplification and single-ended to differential conversion and one feedback path for second-order distortion cancellation [84]. Their design features an active feedback path and thus results in larger power dissipation. To reduce

power consumption, Carrillo et al. presented a single-ended to differential LNA design by replacing active loads and current mirrors by optimized inductors and transformers [85], using the folded cascode topology.

4.7. Process Techniques for LNA Designs

Several process techniques were investigated to improve the design of LNA for mmWave applications.

4.7.1. Round Table Layout

A *Round Table* layout was proposed for a 30-GHz CMOS LNA design to minimize key losses and improve the noise performance [8]. The layout comprises of an arrangement of unit cells. Each cell is small with local substrate guard ring and contacts on both sides of the gate. Furthermore, the overall matrix of unit cells links gate, drain and source terminals through multipath connections. Then, an extrapolated f_{MAX} of 300 GHz was achieved. As shown in Figure 32, CPW structure was used for matching networks due to its high characteristic impedance. In addition, their design adopted a single transistor as first stage to eliminate the noise generated by the cascode device, and used a 40 Ω stabilizing resistor between the two stages to improve stability.

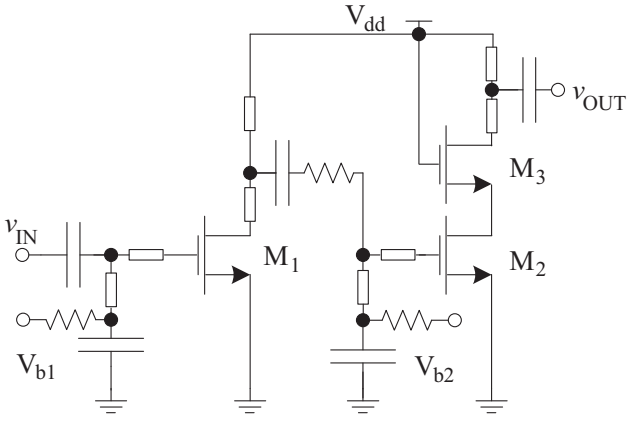

Figure 32. Cascode LNA with CPW structure [8].

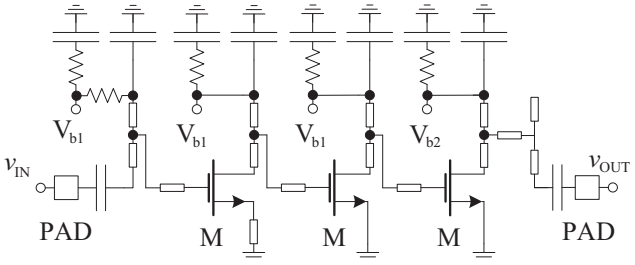

Figure 33. Schematic of a 28 nm FD-SOI CMOS LNA [87].

4.7.2. Above-IC Technology

On-chip transmission lines can be realized above the passivation with a thin-film post-processed technology, and this is believed to be a more attractive and cost-effective solution. This technology is known as *Above-IC technology*, which is used for packaging and bonding pad redistribution during chip manufacturing. Pavageau et al. presented a two-stage cascode LNA design using above-IC technology in [86]. In particular, the input, inter-stage and output matching networks were implemented using microstrip lines in above-IC and back-end-of-line (BEOL) technology.

4.7.3. Fully Depleted Silicon on Insulator

CMOS scaling (around 90 nm) brings up problems like slowed voltage scaling and increased leakage currents. Minor changes were proposed in the process to lengthen the bulk lifetime, among which fully depleted silicon on insulator (FD-SOI) is promising to scale down to 11 nm [6]. As shown in Figure 33, a W-band LNA was designed using 28 nm FD-SOI CMOS technology, with a gain over 12 dB from 53 to 117 GHz and a NF of 6 dB from 75 to 105 GHz [87].

Table 1. Summary of LNA design.

Ref.	f (GHz)	G (dB)	NF (dB)	P_{1dB} (dBm)	IIP3 (dBm)	Process (nm)	Die Area (μm^2)	P_{diss} (mW)	Topology[1]	Techniques
[48]	60	12.5	7.5	-	-	65	540×690	34	2-stage, cascode	transformer-based
[53]	60	22.3	6.1	2.7	-	65	460×460	35	2-stage, cascode	transformer-based
[105]	60	12.5	6.55	-13.3	-	90	730×900	60	2-stage, differential	transformer-based
[106]	60	10	3.8	-	4	65	330×170	42	1-stage, differential	transformer-based
[51]	60	16.4	6.8	3.8	-	65	270000	33.6	2-stage, differential	transformer-feedback
[107]	104-132	21.7	10.4	3.2	-	28	260000	18	4-stage, differential	capacitively neutralized transformer coupling
[17]	45-65	12.7	5.7	-	-	90	450×420	18	1-stage, cascode	transformer feedback
[82]	60	10	3.8	-	4	65	-	35	2-stage, CS	transformer feedback
[52]	60	30	4.6	-30.7	-26	65	820×600	8.9	3-stage, CS	transformer feedback with tuning capacitor
[69]	62.9-92.5	18.5	7.9	-	-	65	240000	27	3-stage, cascode	transformer feedback with pole converging
[38]	60	15	4.4	-18	-	90	320×440	3.9	3-stage, CS	lumped element
[56]	60	22.4 18.7	4.5 5.2	-3.4 -6.5	-	65	400×400	16.8 8.5	2-stage, cascode	lumped element
[88]	60	20	7	-	-	90	375×400	18	2-stage, cascode	lumped element
[89]	60	28	9	-26	-	65	350×550	120	3-stage, cascode	lumped element
[90]	60	13	4	-27.5	-	90	-	9.6	2-stage, cascode and CS	lumped element
[91]	60	8.6	5.5	-16	-	65	-	39	2-stage, differential	lumped element
[39]	60	19.1	5.5	-18	-	65	240×200	25	3-stage, cascode	LC-series resonate
[42]	60	13.7	7.8	-	-	90	1025×1100	45	3-stage, differential	transmission line
[92]	54.5-72.5	13.8	4.0	-12.5	-	28	380000	24	2-stage, cascode	transmission line
[93]	104	16.7	7.2	-	-	65	290000	48.6	5-stage, cascode	transmission line
[43]	60	6.5	4.5	-	-	130	400×300	4.8	1-stage, folded cascode	microstrip line
[44]	60	23.8	6.2	1.5	-	90	590×780	36	2-stage, hybrid	microstrip line hairpin matching
[94]	60	20	6.9	-23	-	130	670×570	67.2	3-stage, cascode	microstrip line
[95]	60	24	7.6	-	-5	65	-	30	4-stage, CS	microstrip line
[96]	60	18.6	5.7	-14.8	-	90	1400×500	28.8	3-stage, CS	microstrip line
[97]	60	7.2	10.0	-19	-	130	-	90	3-stage, cascode	microstrip line
[98]	60	15.7	6.2	-	-	90	113700	40.5	1-stage, differential	microstrip line
[99]	60	19	6.0	-38.5	-	65	-	-	2-stage, differential	microstrip line
[100]	60	18.7	8.3	-	-	90	-	-	4-stage, CS	microstrip line
[101]	60	15	8	-	-	90	-	-	3-stage, cascode	microstrip line
[102]	60	12.2	6	-7.2	-	90	1270×380	-	2-stage, CS	microstrip line
[103]	60	15.1	7.6	-19	-6.9	130	475000	37.2	3-stage, cascode	microstrip line
[104]	64	15.5	6.5	-10.7	-	90	1300×400	42.9	2-stage, cascode	microstrip line
[45]	60	20.3	7.6	-22.3	-11	65	849×560	37.2	3-stage, cascode	current sharing, microstrip line
[113]	60	12.2	4.9	-15	-4.7	130	1000×1090	29.1	6-stage, cascode and CS	current reuse
[116]	60	16.5	9	-20.8	-12	130	-	36.5	4-stage, cascode and CS	current reuse
[114]	60	20	9	-	-15	130	400×370	7.2	2-stage, differential	G_m-boosted, current reuse
[115]	60	30	-	-27	-	130		7.2	2-stage, differential	G_m-boosted, current reuse
[47]	60	10	4.1	-	3	90	577×346	15.2	1-stage, CS	VPW
[108]	60	10	4.1	-	3	90	200000	-	1-stage, cascode	elevated-center CPW
[109]	91	32	5.3	-	-	28	855×324	36	6-stage, cascode	CPW
[110]	143-166	15.7	8.5	-3	-	28	340000	32	4-stage, CS	FD-SOI slow-wave CPW
[55]	60	14.6	5.5	-0.5	-6.8	90	350×400	24	2-stage, cascode	middle inductor
[62]	60	12.6	6.3	-19.6	-	90	650×540	4.9	3-stage, CS	forward body bias
[117]	60	23.5	6.5	-6.8	1	65	600×250	45.6	4-stage, cascode	body-biasing, series-peaking
[86]	60	13.4	6.7	-	-	45	450×800	95	2-stage, cascode	Above-IC and BEOL
[121]	60	12	8	-5	-	65	960×1050	36	2-stage, cascode	CMOS SOI technique
[111]	60	26	6	-21	-	65	700×500	75	3-stage, cascode	capacitive coupling
[112]	80	15.2	5.5	-15.5	-	28	1200×1200	47	2-stage, differential, CS	capacitive cross-coupling
[118]	60	15	5.9	-15.1	-	65	1400×750	30.8	4-stage, cascode	shunt peaking
[119]	60	26	6	3.5	-12	45	150×150	21	2-stage, cascode	shunt peaking
[120]	60	20	7.3	-	-	90	-	-	3-stage, cascode	shunt peaking

[1] The topology is single-ended unless specified.

5. COMPARISON AND SUMMARY

Recent advance in CMOS technology enables us to achieve f_T to 246 GHz [6], and allows us to design CMOS circuit to operate in mmWave frequencies region [3]. However, the resistive substrate of CMOS exacerbates the effect of parasitic losses and complicates the design. The lower available gain of a transistor at mmWave frequency region leaves a small room for modeling errors and mismatches. Quality factors for matching elements are lower, and the proximity to the substrate increases the capacitive coupling and lowers the self resonance frequency (SRF) of passive devices. Therefore, the design of CMOS LNA in mmWave frequency depends on not only topologies and matching techniques, but also the layout of the circuit and the matching components. For example, we should reduce the layout parasitic so as to minimize the losses and improve the inherent performance of the amplifier [6].

From the discussion in Section 4, we can see that there are many approaches in designing an LNA. One may first choose a basic topology, for example, common-source, common-gate, cascode topology or differential topology; and then select an appropriate input/output impedance matching technique. For instance, CNM is able to match the circuit to achieve minimum noise factor at the expense of gain reduction due to the mismatch between the optimum impedance and the complex conjugate of the input impedance of the amplifier. In contrast, SNIM is able to match the impedance and noise simultaneously, but it leads to higher power dissipation. Next, the PCSNIM introduced in [18] able to achieve simultaneous noise and input matching with low power dissipation by adding an external capacitor, which is parallel with the gate and source terminal of the transistor. However, this technique will degrade the f_T of the transistor, reduce the overall gain, and even degrade the performance of the LNA in mmWave frequency since the cutoff frequency of transistor is crucial at high frequencies.

Noteworthily, we propose to classify the matching techniques in three groups, namely CNM, SNIM and indirect matching (IM), where IM is a collective name for other techniques. The rationale behind IM is to remove the impedance constraint by splitting the interface plane into two separate ones. Consequently, the source impedance matching can be achieved at the Z_S plane, and the impedance level at the local plane can be lowered, which gives rise to a larger g_m than the SNIM technique.

Different matching components have their respective advantages. Lumped elements [88–91] occupy less chip areas, but simulation of lumped elements needs very detailed knowledge of the substrate and the cost is relatively higher. Next, transmission lines [92, 93] have well-defined EM simulation environment, but they usually occupy comparatively larger chip areas. Microstrip lines are commonly used [94–104]. Transformer-based impedance matching is also feasible [105–107]. Furthermore, CPW [108–110] is easy to simulate and its measurement results are close to simulation results. However, CPW takes up more chip area. On the other hand, VPW results in higher impedance at the expense of complicated simulation and fabrication process.

To improve an existing LNA design, differential noise reduction techniques, such as capacitive cross coupling [29, 111, 112], resistive feedthrough [34] and G_m-boosted CG topology [23] can be applied. Furthermore, gain-enhancement techniques, such as middle inductor [55], negative feedback [20] and transformer-feedback [58] can be adopted. Finally, to reduce the power consumption, current reuse/sharing technique [59, 113–116], forward body biasing [63] and positive feedback [65] can be used to reduce power dissipation.

For wideband LNAs, matching networks and inductive peaking techniques can be applied [73, 117–120]. It was noticed that transformers are widely used for impedance matching and feedback networks in LNA designs at higher operating frequencies. Due to the space limit, we did not cover all the techniques on wideband LNA designs for UWB, CRs and SDRs. For example, designs of *reconfigurable* LNAs are important for SDRs [50] and review of their related techniques has been left out as part of our future work in this topic.

Finally, we may even use other process technologies to enhance the design, such as Round Table Layout [8], above-IC technology [86] and FD-SOI [110]. For example, Siligaris et al. presented a two-stage cascode LNA design using SOI CMOS technology [121]. In addition, nanowire transistors (NWTs) may be adopted at 5 nm CMOS technology [122] to further increase the operating frequency of an LNA.

Table 1 summarizes performance parameters of LNA designs presented in selected references discussed above, with a focus on those with operating frequencies at 60-GHz and above. For the sake of readability, Table 1 is sorted by different techniques. Within each category indicated by the related technique, the operating frequency is in the ascending order.

6. CONCLUSION

This paper aims to provide a useful and timely reference for microwave and millimeter wave LNA designer and researchers. We provided a comprehensive review starting with key performance metrics, followed by several device circuit models. After discussing various typical LNA topologies, we conducted a survey and comparison of recently-reported design techniques for LNA at microwave and millimeter wave frequencies. Due to limited access to various database and lack of time, our review does not focus on providing an exhaustive list of reported LNA design techniques. Instead, we have studied a number of typical and influential design techniques, and then compared their respective advantages and drawbacks.

Through our comparison, we found that indirect matching is promising in LNA designs at higher operating frequencies. In addition, process techniques such as fully depleted silicon on insulator is necessary with the continued CMOS scaling down towards 5 nm. Our future work includes: (1) to study and design reconfigurable LNAs at mmWave frequencies using indirect matching with inductors of higher Q factors using EM simulator. (2) to perform post-layout simulation, fabricate the design and conduct experimental measurement of our LNA design. (3) to optimize the trade-off among performance metrics like noise factor, gain and linearity. The linearity performance can be further improved by increasing the current drain. Nevertheless, the power consumption will be increased simultaneously. The trade-off can be adjusted accordingly in order to cater for a specific application.

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