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SYSTEM MOEDELING OF HIGH-SPEED DIGITAL PRINTED CIRCUIT BOARD USING SPICE

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1. INTRODUCTION

Implementation of digital systems is usually carried out in the form of printed circuit board (PCB) populated with active components such

as integrated circuits and passive components such as surface mount resistors, capacitors, sockets, connectors, cables, etc. These components together with the PCB traces and metal planes form the network which manifests as a digital PCB assembly. With the increase in operating frequency of devices in access of 100MHz and switching speed of digital devices within sub-nanoseconds, electromagnetic interference, stray parameters of components and unintentional radiation have become a major concern, affecting the integrity of a system. To cope with the issues of system performance, analog and digital circuit simulation tools are used to verify system performance in terms of signal integrity, noise margin and bandwidth under various signal patterns (vectors) and biasing during CAD layout process to ensure first-time-working prototypes. This article illustrates a structural modeling approach in which the digital PCB is considered as an assembly of parts which are modeled as electrical networks with input and output ports. The networks are linked together to form a complete system of equivalent circuit in SPICE format. Various methods have been developed by many authors [1–19] for modeling a certain aspect of the digital PCB system. Based on their work, the authors consolidate the methods and propose a structural approach to derive a system level equivalent circuit model for a digital PCB system. Section 2 outlines the modeling procedures using the structural approach. Section 3 gives the EM Field Method for deriving equivalent circuit models of sockets, connectors, interconnecting traces and discontinuities in PCB. Section 4 contains circuit models of discontinuities and IC buffers using measurement techniques. In Section 5, the power planes are modeled using a planar circuit approach [20]. A simple digital PCB system modeling example is presented in Section 6 to illustrate the proposed approach. Detailed system simulation is carried out using SPICE Version 6.1 on an IBM compatible PC. Both time and frequency domain simulations are performed. Areas of large current concentration in the power plane at any instance can be located. This allows one to determine the optimum location to install decoupling capacitors and filters to suppress EMI. An IC in the system is then replaced with a power validator. The power validator is a programmable load having the same footprint as the IC. It simulates the IC, drawing varying amount of current from the power distribution systems. An equivalent circuit is derived and SPICE simulation is performed to study the noise introduced by the die within the IC.

2. MODELING PROCEDURES IN THE PROPOSED STRUCTURAL APPROACH

A direct approach to derive an equivalent circuit network for the PCB assembly is through application of numerical methods which include differential method such as Finite Element Method (FEM) [2] and integral method such as Method of Moments (MoM) [3]. The conducting traces on the PCB and its surrounding are discretized into triangular elements and the integro-differential equations are transformed into a system of linear equations. An admittance matrix $\overline{\overline{Y}}(\omega)$ linking the equivalent voltage and current on the conducting elements is defined. Under quasi-static approximation equivalent circuit using passive elements such as R, L, C, and G can be assigned to the elements $y_{ij}(\omega)$ of the admittance matrix and an approximate circuit representing the system is constructed [4,5].

However the application of numerical method becomes extremely computer intensive when applied to practical PCB with hundreds of conducting elements scattered in different layers. An alternative approach, termed a structural approach by the authors, is to consider the PCB assembly to be divided into many distinct regions. Each region encloses certain elements of the system, for instance a group of traces, a via, a pad etc. The structural approach considers a digital PCB assembly to be integration of the following components:

(a) Transmission line interconnections such as PCB traces.
(b) Integrated circuit sockets, edge connectors, PCB headers, coaxial to PCB adapter etc.
(c) Discontinuities in interconnection such as vias, bends, crossing, T-junction etc as shown in Figure 1.
(d) Power distribution system consisting of power and ground planes.
(e) Discrete components such as surface-mount resistors, capacitors, integrated circuit sockets and packaging which are approximated as lumped circuits. The integrated circuit packaging refers to the physical elements which include the pins, enclosing, interconnection within the enclosing, but excluding the semiconductor die.
(f) The architecture and logical entity (which is often expressed using VHDL or Boolean Algebra) of the digital integrated circuit which is linked to the external environment via input/output buffers, power pins and packaging.

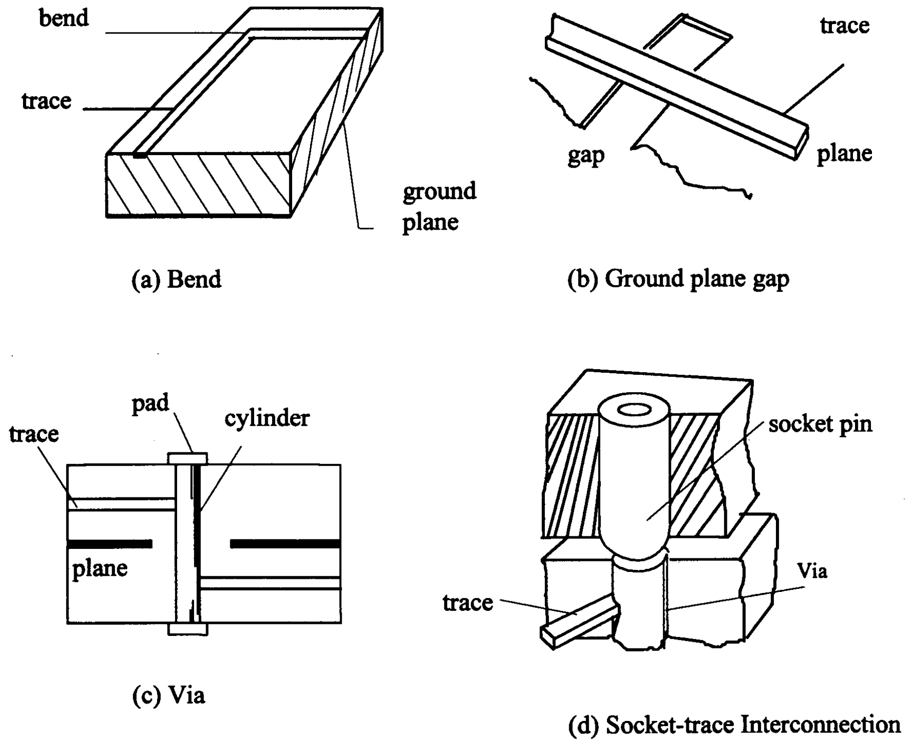


Figure 1. Common discontinuity structures in a PCB assembly system.

Each of the above components is taken to be a small module with input and ouput ports. Characteristics of the input and output relationship for a small module are defined through careful theoretical analysis, numerical method and measurement. Equivalent circuit models are derived for these modules in terms of linear time invariant circuit elements using resistor, inductor, capacitor, transmission line and dependent voltage and current. In some instances, such as in modeling of integrated circuit input-output buffers, no-linear time invariant dependent current and voltage sources may be required. These circuit elements are compatible with industry standard circuit simulator such as SPICE [6,7]. All necessary parameters are removed to simplify the model as much as possible, yet retaining the essence of the model. These modules are linked to form a large and complex electrical network which is then subjected to computer circuit analysis to determine

the time and frequency domain response of the system under specific bias and excitation. In many ways this approach is a simplification as compared to the direct method. However, it can only be applied for a loosely coupled system where quasi-static electromagnetic analysis is valid, and when radiation from the PCB conductors is small. By a loosely coupled system we mean a system of conductors which is sufficiently far apart such that the characteristic inductance, capacitance, resistance and conductance matrices representing the system can be approximated by sparse matrices. Upper frequency limit for quasi-TEM solution is dependent on dielectric thickness of the PCB. For instance dielectric thickness of 1.0mm between conducting layers has upper frequency limit of 2–4GHz [21]. From the circuit theory point of view, a distributed component can be considered as a lumped circuit if:

$$1 \leq \frac{1}{10}\lambda \tag{1}$$

$$\lambda = \frac{1}{f\sqrt{\varepsilon_r \varepsilon_o \mu_r \mu_o}} \tag{2}$$

where l is the electrical length and λ is the shortest electromagnetic wavelength in the system. At 2GHz, using $\varepsilon_r = 4.3$ for typical epoxy resin dielectric, $\lambda = 72.3\,\text{mm}$. In a typical PCB, most feature size, such as trace discontinuity and gap in power plane, ranges from 1 - 10 mm. Thus a conservative estimate for suitable frequency bandwidth using structural approach in PCB of average component density is between 0 to 1GHz. As radiation intensity from PCB conductors increases, equivalent network representing radiation coupling has to be incorporated. This would mean each conductor is strongly coupled to every other conductors in the system. This will invariably lead to a very complicated equivalent circuit.

It is also assumed here that the electromagnetic field configuration between the PCB trace and ground/power planes can be approximated as a two dimensional quasi-TEM field of and infinite length transmission line. Hence all PCB traces can be modeled as microstrip line and striplines. Employing the structural approach, a two trace example in Figure 2 could be modeled as three transmission line segments with inductors for the bend in AB. We can compare this with direct discretization approach where a mesh of RLCG elements are generated. Discretization is necessary in both approaches as it is required to estimate the quasi-TEM fields through numerical method. From Figure 2,

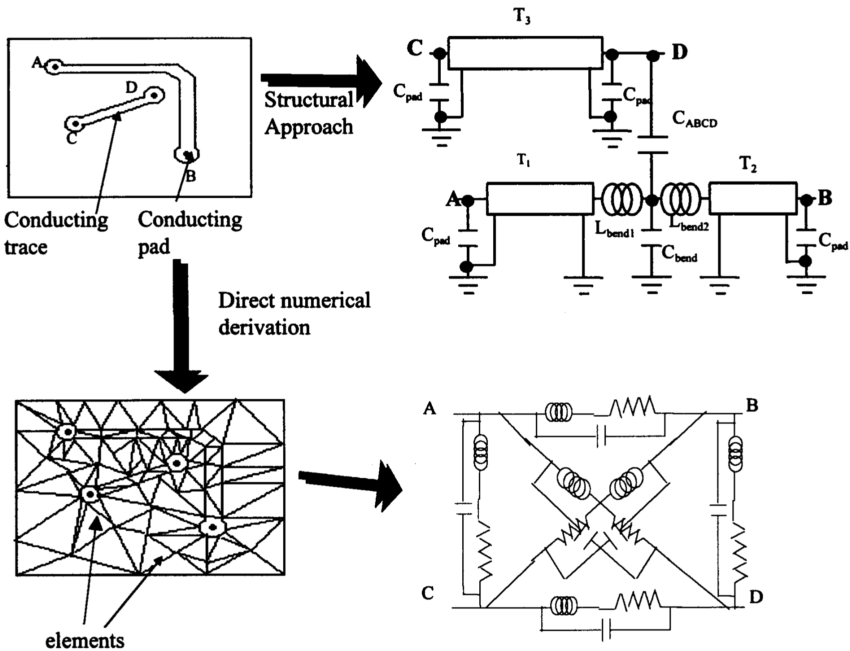


Figure 2. Discretization of PCB traces and their equivalent circuits using Structural Approach and Direct Numerical Derivation Technique.

it is obvious that a less complicated equivalent circuit is obtained using the structural approach. The accuracy of both approaches is limited by the quasi-static approximation.

3. DERIVATION OF EQUIVALENT CIRCUIT MODEL USING ELECTROMAGNETIC FIELD SOLUTION

3.1 Modeling Sockets and Connectors

Electromagnetic field solver software is used to determine approximate electromagnetic field configuration for a system of conductors and dielectric using numerical methods such as Finite Element Method (FEM) or Method of Moments (MoM). For modeling structures such as socket, package etc., the quasi-static approximation is adopted. The electromagnetic field configuration is assumed to be similar to the d.c.

field pattern when the frequency dependent portion $e^{j\omega t}$ is suppressed. The approximate resistance (R), conductance (G), capacitance (C) and inductance (L) matrices characterizing a system of conductors can be determined from the electromagnetic field configuration. These matrices will then represent lumped or distributed values depending on the conductor size and the shortest electromagnetic field wavelength encountered. Energy stored in the electric field is directly related to the capacitances of the equivalent circuit while energy stored in the magnetic field is related to the inductances of the equivalent circuit [8]. Power loss due to skin effect in the conductor is attributed to the equivalent resistance matrix of the equivalent circuit. The conductor power loss is dependent upon the boundary conditions of the magnetic field at the surface of all the conductors, hence resistance matrix can be estimated from the magnetic field [21]. The dielectric leakage and polarization loss can be included in the conductance matrix. The conductance matrix is derived from the capacitance matrix by considering the permittivity of the lossy dielectric to be complex, and hence it is dependent on the electric field [8]. Often the field solution for the lossy condition is very difficult to find, in which case the perturbation method is extremely useful and simple to carry out. This method assumes that the introduction of small loss does not substantially disturb the field from its lossless condition. The quasi-static $\mathbf{E}$ and $\mathbf{H}$ field are computed for lossless condition using either FEM or MoM on a three dimensional model of the object with suitable far field and boundary conditions. The lossless electromagnetic field is then applied to estimate the distributed parameters using the following equations [22]. For capacitance between conductors i and j:

$$C_{ij} = \frac{2}{V_i V_j}\left[\frac{\delta_{ij}}{2}\iiint \varepsilon \mathbf{E_i} \bullet \mathbf{E_j}\, d\Omega\right] \tag{3}$$

where δ_{ij} (Kronecker delta) is defined as:

$$\delta_{ij} = 1 \quad \text{if} \quad i = j; \quad \text{and} \quad \delta_{ij} = -1 \quad \text{if} \quad i \neq j \tag{4}$$

and $\mathbf{E_i}$ is the quasi-static electric field when V_i is applied to conductor i and all other conductors are grounded.

For inductance between conductors i and j:

$$L_{ij} = \frac{2}{i_i i_j}\left[\frac{1}{2}\iiint \mu \mathbf{H_i} \bullet \mathbf{H_j}\, d\Omega\right] \tag{5}$$

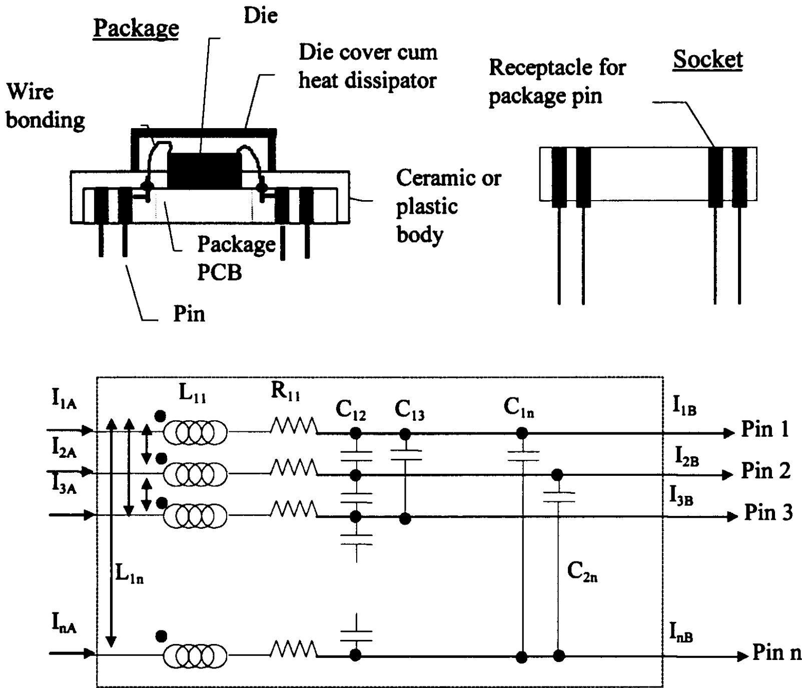


Figure 3. A Pin Grid Array (PGA) package and socket, and the equivalent circuit.

where $\mathbf{H}_\mathrm{i}$ is the quasi-static magnetic field when current I_i flows in conductor i while all other conductors are open-circuit.

For resistance between conductors i and j :

$$R_{ij} = \frac{\mathrm{Re}\left[R_s \displaystyle\int_{C_1+C_2+\cdots C_n} \mathbf{H}_\mathrm{i} \bullet \mathbf{H}_\mathrm{j}^* \, dl\right]}{I_i I_j} \quad \text{with} \quad R_s = \sqrt{\frac{\omega\mu}{2\sigma}} \tag{6}$$

where R_s is the skin resisuctor at angular frequency ω, σ is the conductivity of the conductor.

Finally for conductance between conductors i and j :

$$\overline{\overline{G}} = \omega(\tan\delta)\overline{\overline{C}} \quad \text{with} \quad \tan\delta = \frac{\varepsilon_r''}{\varepsilon_r'} + \frac{\sigma}{\omega\varepsilon_r'} \tag{7}$$

where $\overline{\overline{G}}$ and $\overline{\overline{C}}$ are the conductance and capacitance matrices, respectively, of the collection of conductors, and $\tan\delta$ is usually referred

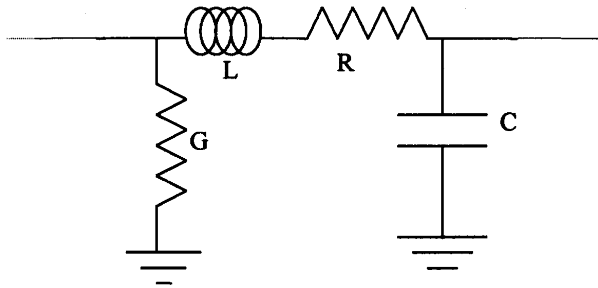


Figure 4. Distributed representation of lossy transmission line, assuming TEM and TEM propagation.

to as the loss tangent of the dielectric material with complex relative permittivity $\varepsilon_r = \varepsilon_r' - j\varepsilon_r''$ [23].

Electromagnetic field solution method is suitable for modeling passive components such as:

(a) integrated circuit package and socket
(b) single and parallel transmission lines
(c) transmission line discontinuities.

An integrated circuit socket and a package are shown in Figure 3 along with the equivalent circuit using lumped elements. Equations (3) to (7) can be employed to determine the values of the characteristic RLCG matrices elements. Note that for an integrated circuit socket or package, there is no ground plane or reference. Therefore the inductances of the equivalent circuit in Figure 3 is the self partial inductance and mutual partial inductance [9].

3.2 Modeling Transmission Line

Interconnection traces in PCB can be modeled as microstrip and stripline type transmission line. These transmission lines are sometimes laid adjacent to each other and are considered as a single entity, i.e. a muticonductor transmission line. A general lossy transmission line with its dominant mode of propagation being TEM, or quasi-TEM for inhomogeneous transmission line, can be represented by distributed parameters of the form shown in Figure 4 [10]. The parameters required to model the line are the RLCG values and the physical length of the line. Single lossy transmission line is supported in common

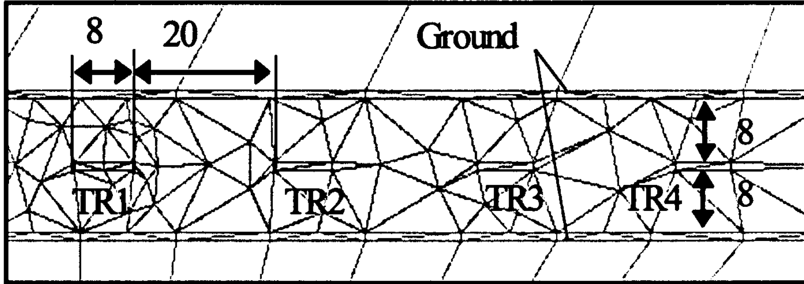


Figure 5. Discretization of couple stripline model into triangular elements (units are in mils).

SPICE simulators [5,6] using impulse response method based on convolution of the time domain impulse response and the excitation of the transmission line [11].

This representation is extended to the multiconductor transmission under quasi-TEM approximation using the generalized telegraphists' equations to describe the instantaneous voltage and current relationship in a multi conductor transmission line system. Distributed RLCG matrices are required to fully describe a multiconductor transmission line. Electromagnetic field solution approach using equations (3)–(7) is used to estimate these matrices. Any combination of input and output signals on the multiconductor transmission line is a linear superposition of intrinsic solutions called eigenvectors or modes [11]. The resistance matrice represents the accumulated skin effect losses due to these modal waves [8]. For lossy multiconductor transmission line matrix inverse Fourier transform or the matrix impulse response method can be utilized to relate the input and the output signals. It is not possible to represent general multiconductor transmission line using linear time invariant circuit elements as current state of the system output with respect to certain excitation also depends on previous output states [11]. However under special condition of lossless system, when:

$$\overline{\overline{R}} = \overline{\overline{0}} \quad \text{and} \quad \overline{\overline{G}} = \overline{\overline{0}} \tag{8}$$

a multiconductor transmission line can be decoupled through matrix

diagonalization technique and SPICE compliant equivalent circuit can be derived [12]. Figure 5 shows the cross section of a system of four adjacent striplines being partitioned into triangular elements by the FEM solver software. The inductance and capacitance matrices are estimated from the lossless quasi-static field. A lossless equivalent circuit model for the traces using matrix disagonalization of [12] is shown in Figure 6. The zero voltage sources V1 to V8 in the Figure are used by SPICE program for probing the current into each transmission line terminals. The diagonalization is achieved using matrix transformation of the multiconductor transmission line terminal currents and voltages. The transformation manifests as an array of dependent voltage and current sources on both terminals of the multiconductor transmission line. The transmission line network between these dependent sources represents the uncoupled multicounductor transmission line. Therefore to create an equivalent circuit for a general multiconductor transmission line, a new component with its corresponding mathematical expression has to be incorporated in the SPICE circuit simulator. Alternatively the lossless approximation can be made and an equivalent circuit of Figure 6 can be created using existing elements supported by SPICE based circuit simulator. The linear transformation of terminal voltages and currents is carried out by the dependent voltage and current sources. Transmission lines T1 to T4 are decoupled from each other as a result of the transformation. Most PCB traces are made of gold plated copper, and dielectric losses is negligible below 1 GHz so that lossless assumption can be accepted most of the time.

3.3 Transmission Line Discontinuities

Introduction of passive discontinuities such as the example in Figure 1 into an infinite length transmission line will distort the uniform electromagnetic field present in the transmission line. This distortion of field in the vicinity of the discontinuity can be viewed as a superposition of induced higher order evanescent fields to match the boundary conditions of the discontinuity. Higher order fields are usually reactive since loss due to dielectric is negligible and the discontinuity is normally made of excellent conducting material.

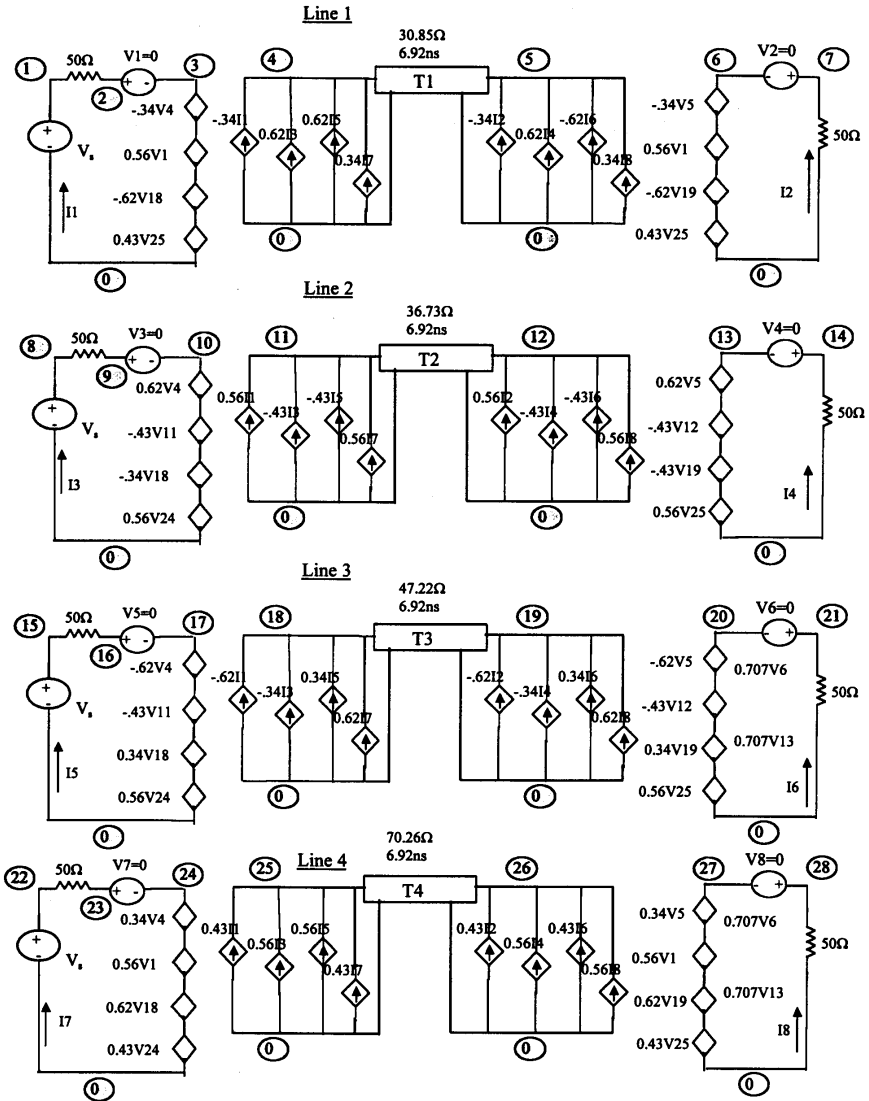


Figure 6. Equivalent circuit in SPICE format for lossless traces using matrix diagonalization.

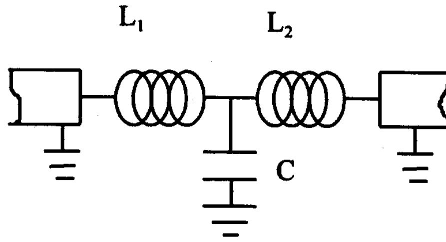


Figure 7. A general T-type equivalent circuit for passive transmission line discontinuity.

Associated with the higher order local fields are charge and flux that will complement the infinite transmission line distribution. These are known as excess charge and excess flux. Associated with the excess charge, a lumped equivalent capacitance can be assigned at the discontinuity [13, 14]. Similarly a lumped equivalent inductor is assigned for excess flux at the discontinuity [15]. A general T-type equivalent circuit for passive transmission line discontinuity is proposed in Figure 7 based on the above argument [16]. The concept can even be extended to discontinuity such as bends in multiconductor transmission line [17]. Figure 8 illustrates a via discontinuity modeling example and comparison of time domain reflectometry and SPICE simulation wave form. The via is modeled using FEM based electromagnetic field solver software to determine the equivalent lumped capacitance and inductance of the discontinuity from excess charge and flux. A model of the via is defined with appropriate boundary conditions. For instance it is assumed that at the six surfaces of the cube enclosing the model, the electric field is normal to the surface while the magnetic field is tangential to the surface. The static scalar and vector potential are estimated using FEM and the electromagnetic fields can be determined from these potentials. The process of estimating the excess field from the total field is known as deembedding [15]. As it is difficult to represent a three dimensional object of very small thickness effectively using tetrahedral elements, the component and solder side pads are removed to simplify the discretization process of the problem region. Furthermore the ground planes are declared as Dirichlet boundary condition

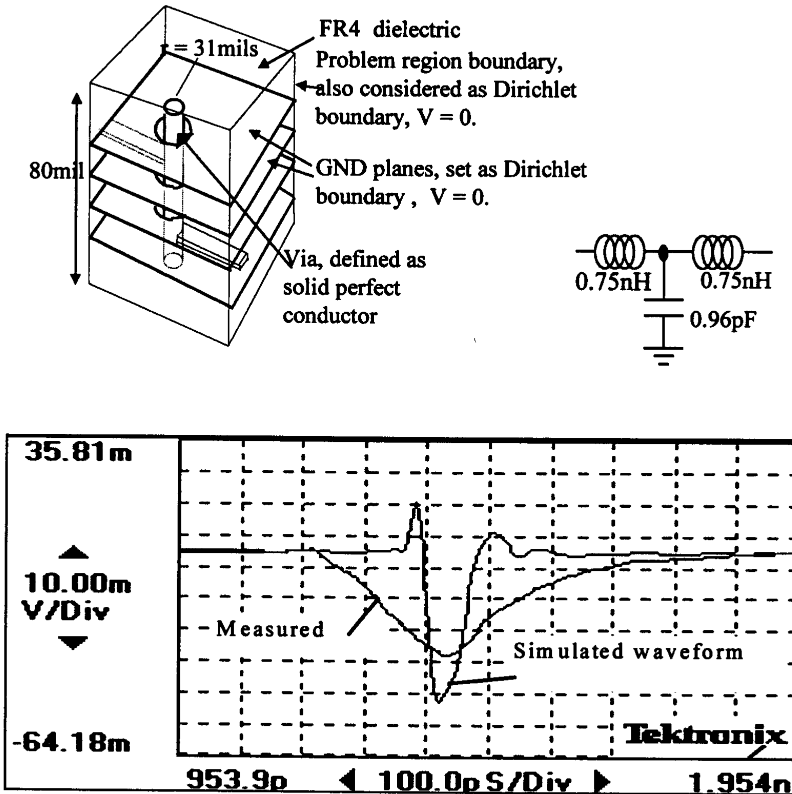


Figure 8. Comparison between measured and simulated result for a via discontinuity using Time Domain Reflectometry technique.

with scalar potential set to zero. Figure 8 gives a comparison of Time Domain Reflectometry (TDR) measurement performed on an actual trace with via and the result obtained from simulated TDR measurement using symmetrical T model. The schematic for obtaining the simulated TDR measurement is shown in Figure 9. The discrepancy in time axis for the waveforms in Figure 8 is due to the assumption that stray capacitance and inductance are lumped. For cases when two geometrically different transmission lines are connected through a discontinuity, a non-symmetrical T model must be used.

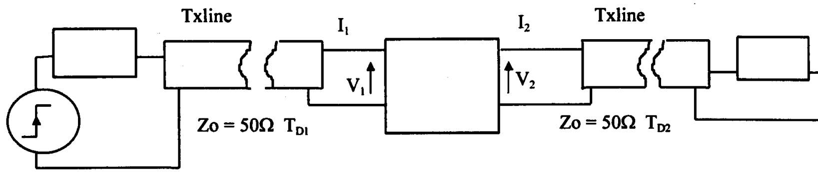


Figure 9. Schematics of circuit used for a via.

4. DERIVATION OF EQUIVALENT CIRCUIT MODEL THROUGH MEASUREMENT

Measurement based methods are able to account for most parasitic effects encountered. Measurement is performed in time and frequency domain using Time Domain Reflectometry (TDR) and S-parameters characterization techniques, respectively. It is possible to carry out measurement at d.c. condition to derive the current - voltage relation for an integrated circuit buffer so that an equivalent circuit can be derived. Generally the following elements can be effectively modeled using measurement approach:

(a) single transmission line discontinuity
(b) integrated Circuit input/ouput buffer
(c) discrete components such as resistor, capacitor and inductor.

4.1 TDR Measurement Method

TDR is based on the knowledge that a reference transmission line connected to an unknown load will reflect a portion of the incident electrical energy back to fulfill the boundary conditions between the transmission line and the load. By studying the reflected voltage waveform of a step pulse from an unknown load, much information can be obtained on the nature of the load [18, 19, 20, 22]. An equivalent lumped circuit which would give the approximate measured response can be assigned to the load. This TDR technique is used for discrete components with single input and output connections, as well as components with multiple connections such as integrated circuit sockets, packages and transmission line discontinuities. Advanced TDR method such as differential TDR can also derive equivalent circuits for parallel transmission lines, I.C. sockets and packages [24, 25].

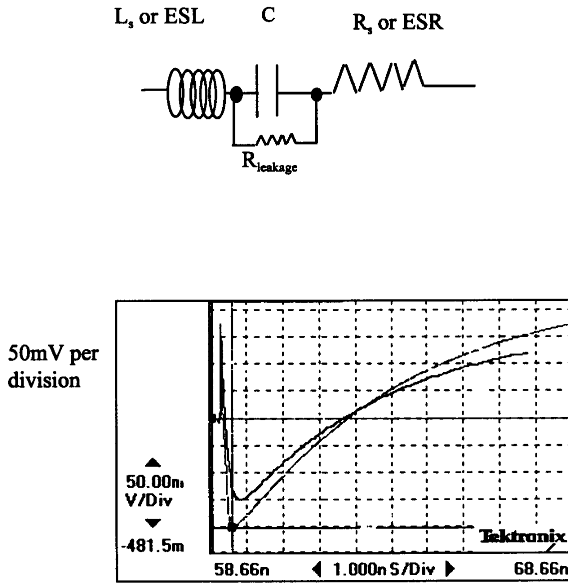


Figure 10. A close-up view of measured and theoretical TDR response for a leaded $100pF$ ceramic capacitor. The estimated parameters: $C = 100pF$; $ESL = 8nH$, $ESR = 0.06Ohm.$.

An example of deriving equivalent circuits for a leaded ceramic capacitor is shown in Figure 10. A model of a practical capacitor is shown on top of the figure. Laplace transformation is employed to determine the time domain reflected voltage response of the proposed equivalent circuit for capacitor. The expression for the reflected voltage is given by:

$$V_g(t) = V_{step}\, U\left(t - 2\frac{1}{\nu}\right)$$
$$\left\{ \begin{array}{l} 1 + A\exp\left[-\dfrac{(R+R_o)+\sqrt{(R+R_o)^2 - 4\frac{L}{C}}}{2L}\right] \times \left[t - 2\dfrac{l}{\nu}\right] \\ + B\exp\left[-\dfrac{(R+R_o)+\sqrt{(R+R_o)^2 - 4\frac{L}{C}}}{2L}\right]\left[t - 2\dfrac{l}{\nu}\right] \\ + V_{step} U(t) \end{array} \right\} \tag{9}$$

where:

$$A = 2R_o \frac{\left[(R+R_o) - \sqrt{(R+R_o)^2 - \frac{4L}{C}}\right]}{\left\{(R+R_o\left[(R+R_o) - \sqrt{(R+R_o)^2 - \frac{4L}{C}}\right] - \frac{4L}{C}\right\}} \quad (10)$$

$$B = 2R_o \frac{\left[(R+R_o) + \sqrt{(R+R_o)^2 - \frac{4L}{C}}\right]}{\left\{(R+R_o\left[(R+R_o) + \sqrt{(R+R_o)^2 - \frac{4L}{C}}\right] - \frac{4L}{C}\right\}} \quad (11)$$

TDR measurement is obtained for the capacitor and compared with theoretical curve given by equation (9). The corresponding values of the R, L and C elements are obtained through computer optimization, typically using Method of Steepest Descent [26]. The objective function would be the square of the norm for the difference between measurement and calculated voltage R_{leakage} in capacitor is very large $(> 10M\Omega)$ while C_{shunt} is often very small for well designed resistor $(> 1pF)$, thus these parameters are usually ignored.

The sharp spike in Figure 10 is due to the effective series inductance. Insufficient resolution of the sampling head of the digital sampling oscilloscope resulted in the discrepancy between measurement and simulation spike level.

4.2 Impedance Profile Method

Impedance profile approach is another effective way to derive the approximate lossless model for transmission line discontinuities. This approach is based on analyzing the impedance profile of a general transmission line [19, 20]. A transmission line interconnection system can be considered as a one dimensional system with the local impedance being a function of distance along the length of interconnection. Here for simplicity of analysis, the interconnection is assumed to be lossless.

The idea is to consider an interconnection such as a transmission line system, including the discontinuities as consisting of many small transmission lines segments, each with characteristic impedance Z_i , This concept is illustrated in Figure 11. The time Δt required for an electromagnetic wave to transverse each segment is the same. Therefore it is evident that in general the physical lengths l_i of the segments are not equal. A real impedance R_i can be assigned to each segments

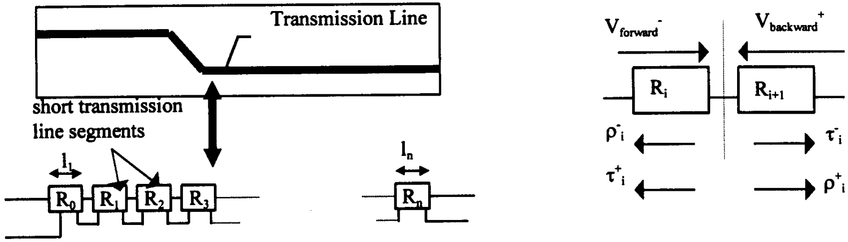


Figure 11. Assignment of an interconnection system to a series connection of transmission line segments for derivation of equivalent circuit.

with:

$$R_i = \sqrt{\frac{L_i}{C_i}} \tag{12}$$

where L_i and C_i are the local per unit length inductance and capacitance of segment i respectively. Corresponding to each intersection between segments i and $i+1$, a reflection coefficient ρ and transmission coefficient τ can be defined. The reflection and transmission coefficients can be defined for the forward and backward incident waves. Using "-" to denote forward direction and "+" to denote backward direction as shown in Figure 11, the forward reflection and transmission coefficients are related to the impedance by:

$$\rho_i^-(t) = \frac{R_{i+1} - R_i}{R_{i+1} + R_i} = -\rho_i^+(t) \tag{13}$$

$$\tau_i^-(t) = \frac{2R_{i+1}}{R_{i+1} + R_i} \tag{14}$$

$$\tau_i^+(t) = 1 - \rho_i^-(t) \qquad)15)$$

Assuming R_i is known, R_{i+1} can be determined from Equation (13) as:

$$R_{i+1} = \frac{1 + \rho_i^-(t)}{1 - \rho_i^-(t)} \tag{16}$$

By sampling the incident and reflected voltage waveform and similarly discretized into narrow rectangular pulses, a matrix equation can be

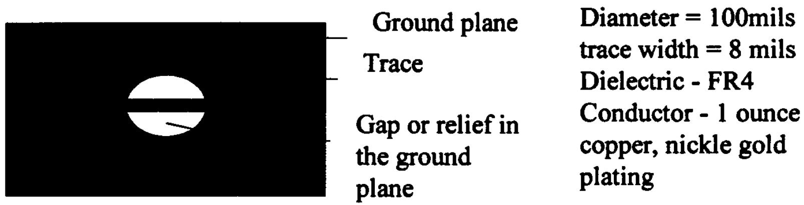
formed [19, 25].

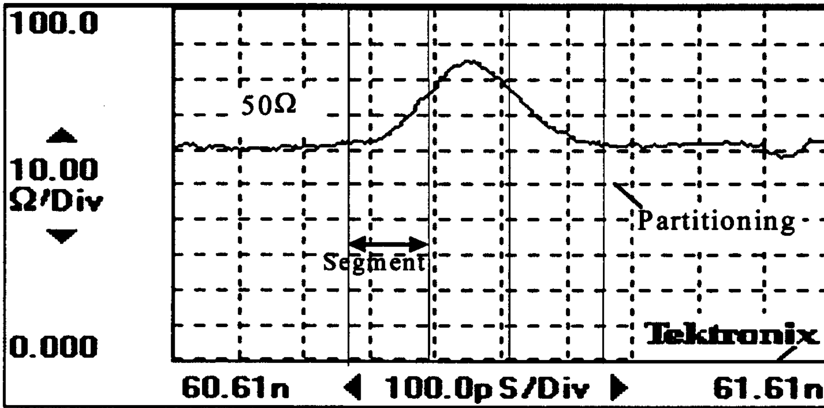
$$\begin{bmatrix} \mathrm{Ref}[1] \\ \mathrm{Ref}[2] \\ \mathrm{Ref}[3] \\ \vdots \\ \mathrm{Ref}[n] \end{bmatrix} = \begin{bmatrix} c_1 & 0 & 0 & \dots & 0 \\ c_2 & c_1 & 0 & \dots & 0 \\ c_3 & c_2 & c_1 & \dots & 0 \\ \vdots & \dots & \dots & \ddots & 0 \\ c_n & c_{n-1} & \dots & c_2 & c_1 \end{bmatrix} \begin{bmatrix} \mathrm{Inc}[1] \\ \mathrm{Inc}[2] \\ \mathrm{Inc}[3] \\ \vdots \\ \mathrm{Inc}[n] \end{bmatrix} \tag{17}$$

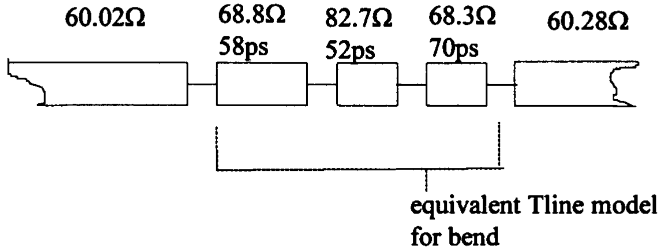
where $\mathrm{Ref}[i]$ and $\mathrm{Inc}[i]$ refer to the measured incident and reflected voltage at time $t = \Delta t.i$. The value of coefficient c_i is determined from equation (17) and is a function of ρ_i^-, $\rho_{i-1}^- \dots \rho_1^-$ [22, 25]. Therefore ρ_i^- can be determined. R_i of each sub-segment of the transmission line can then be calculated from equation (13). By comparing the impedance profile of a controlled transmission line system and an impedance profile of transmission line with discontinuity, variation due to discontinuity can be pinpointed. The discontinuity is then modeled as a sequence of short transmission lines by partitioning the location where variation in impedance occurs. The modeling example considered a ground plane gap in a stripline. The structure of the ground plane gap and the impedance profile are shown in Figure 12A. Comparison between measurement and simulation results is shown in Figure 12B. The important observation here is that stray inductance becomes dominant in the presence of gap in planes, causing the increase of effective impedance seen.

4.3 Frequency Domain Measurement Method

S-parameter measurement is convenient for discrete components with single input and output connections. It is based on measurement of an unknown network d.c. and S-parameter values S_{11} and S_{12} [27]. The equivalent circuit model parameters are extracted by computer optimization which proposes an equivalent circuit using RLCG circuit elements. The simulated d.c. and S-parameters can be correlated with measured data by tuning the values of the RLCG elements [28, 29]. Elaborate calibration structures have to be incorporated into the PCB for the device under test (DUT) to obtain reliable measurement results. A modeling example to derive the approximate equivalent circuit for the discontinuity of an SMA to transmission line adapter is shown in Figure 13. Two SMA to PCB adapters are connected back to back in a 6 layer PCB. A T-type equivalent circuit similar to Figure 7 is







* The effective impedance in each segment is the average within the segment

Figure 12A. Impedance profile of ground plane gap and partitioning for equivalent circuit computation.

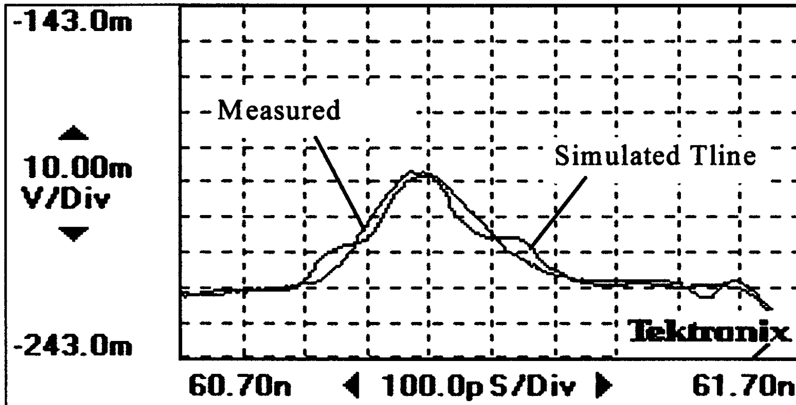


Figure 12B. Comparison between measured and simulated result of ground plane gap using segmented transmission line model.

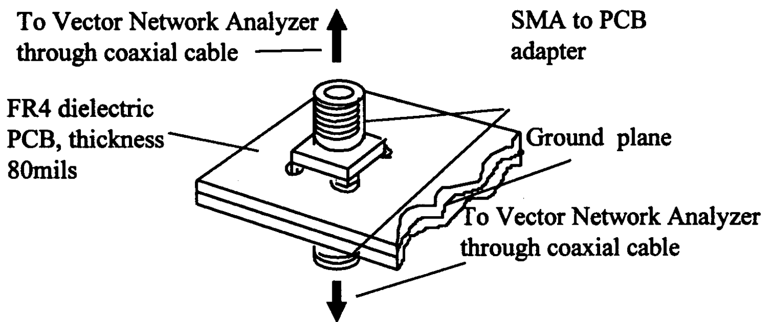


Figure 13. The experimental setup for derivation of equivalent circuit for the discontinuity from a SMA to a transmission line adapter.

proposed for the equivalent circuit. The optimization problem can be formulated using the least square criteria (l_2) [26]. The least square optimization attempts to minimize the square of the errors between a stream of theoretical data and measured data by tuning the parameters within the theoretical function. The quantity to be minimized (error)

is usually referred to as the objective function. Implementation of least square optimization in frequency domain measurement is accomplished by comparing the real and imaginary parts of theoretical S_{11} and S_{12} with measured S_{11} and S_{12}, respectively, at m frequency points using weighting constants of unity. Since the discontinuity is symmetry, $L_1 = L_2$ and $S_{11} = S_{22}$, $S_{12} = S_{21}$. Thus the objective function is:

$$\begin{aligned} F(L,C) = & \sum_r \{\mathrm{Re}[S_{11}(j\omega_r)] - \mathrm{Re}[S_{11_r}]\}^2 \\ & + \sum_r \{\mathrm{Re}[S_{12}(j\omega_r)] - \mathrm{Re}[S_{12_r}]\}^2 \\ & + \sum_r \{\mathrm{Im}[S_{11}(j\omega_r)] - \mathrm{Im}[S_{11_r}]\}^2 \\ & + \sum_r \{\mathrm{Im}[S_{11}(j\omega_r)] - \mathrm{Im}[S_{11_r}]\}^2 \end{aligned} \tag{18}$$

where:

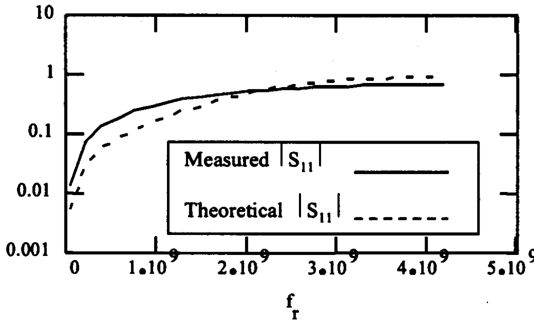
$$S_{11}(s) = \frac{\left(s^2 + \frac{2L}{C} - Z_o^2\right) s}{s^3L^2 + 2Z_oLs^2 + \left(\frac{2L}{C} + Z_o^2\right) s + \frac{2Z_o}{C}} \tag{19}$$

$$S_{12}(s) = \frac{\left(s^2 + \frac{2L}{C} - Z_o^2\right) s}{s^3L^2C + 2Z_oLCs^2 + (2L + Z_o^2C)\, s + 2Z_o} \tag{20}$$

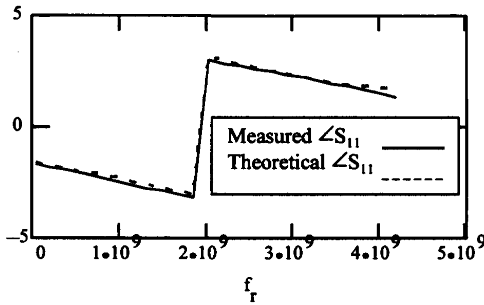
Z_o is the intrinsic impedance of the reference transmission lines on both sides of the SMA adapters. $F(L,C)$ corresponds to the error, a small value for $F(L,C)$ means that the theoretical and measured scattering parameters are close to each other. Iteration approach such as method of steepest descent [26] is used to obtain the stationary point of the problem. Values for the partial derivatives are computed using perturbation method. In order to check that the solution does provide a strong minimum point, a sufficient condition is that the Hessian matrix must be positive definite at the stationary point [26]. In this example the partial differentiation value is very large and could cause the iteration to oscillate wildly. Secondary variables are introduced to replace L and C to eliminate such undesirable effect [22]:

$$L(x) = L_o + x\Delta L \quad \text{and} \quad C(y) = C_o + y\Delta C \tag{21}$$

L_o, C_o, ΔL, and ΔC are fixed values while x and y are variables.



(A) Comparison of measured and theoretical results of magnitude of S_{11}



(B) Comparison of measured and theoretical results of phase of S_{11}

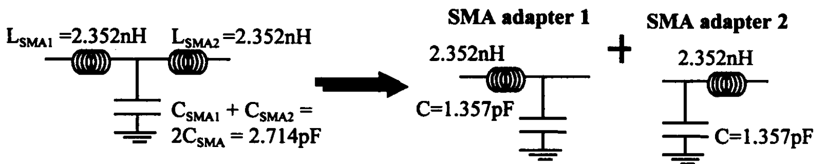


Figure 14. Comparison of measured and theoretical results of S_{11} .

Figure 14 shows a comparison of the simulated and measured S_{11} . In the Figure the T type equivalent circuit is separated into two LC circuits for each of the adapters.

4.4 Modeling I.C. Buffer

Accurate evaluation of a buffer can be performed on die level by using microprobes and applying a stimulus and observing the results with a curve tracer. Most integrated circuit manufacturers provide an ensemble of performance curves in addition to circuit diagram of the integrated circuit. These curves normally include the d.c. I-V plot of the buffers input and output, slew rate versus loading, ouput impedance versus frequency or load, etc. The concept of Analog Behavioral Modeling (ABN) is to derive a representation of the input/output (I/O) buffer from this information using basic circuit devices such as voltage control current sources, independent voltage and current sources, and RLCG elements from the curves. This would result in a much simpler model, retaining the essential information (non-linear and parasitic effect) of the buffer, yet hides the user from the proprietary information such as fabrication technology and actual schematics pertaining to the manufacturer. The standard method of presenting the buffer information is based on the IBIS (Input/Output Buffer Information Specification) standard [30, 31]. An example for a simple integrated circuit output buffer and its equivalent SPICE schematic using circuit elements based on IBIS standard is illustrated in Figure 15. The SPICE compliant output buffer consists of pull-up/pull-down ramp generators, voltage controlled current sources functioning as pull-up/pull-down V-I drivers as well as ESD protection diodes, and finally the package model. The ramp generators are to account for the finite slew rate observed at the output while the V-I drivers are the sources which provide energy to transmit signal to external loads.

5. MODELING POWER PLANES

Modern PCB layout utilizes a whole conducting plane, called power plane to deliver and sink electrical power to all the various active components attached to the PCB due to their low impedance. As the operating speed of components increases, the rate of loading change and transient current increases accordingly, thus impedance of the power plane becomes important and it must be viewed as a broad transmission line with low characteristic impedance. A pair of VCC and GBD planes is shown in Figure 16. The planes are discretized into square elements of side "**a**". The center of each element is called a node. Using the concept of balanced transmission line and finite difference

time domain (FDTD) method [20], the discretized pair of power planes can be represented as a mesh of inductor and capacitor whose values depend on the size of the elements, dielectric constant and separation thickness.

$$C = \left(\frac{2\varepsilon}{d}\right) a^2 \tag{22}$$

$$L = \left(\frac{\mu d}{2}\right) \tag{23}$$

Here all dielectric materials are assumed to be non-magnetic. The main assumptions for the model to be valid are:

(a) Separation between VCC and GBD planes is much smaller ($< 0.05\lambda$) than the shortest wavelength encountered in the system.
(b) $E_x = E_y = 0$ at the electric wall (perfect conductor)

Note that the electromagnetic fields satisfy the Helmholtz wave equation in the region between the plane. For details of the modeling, the readers are referred to [20].

6. SIMULATION EXAMPLES

A simple digital system is shown in Figure 17. The scenario modeled is a transceiver module plug-in-card communicating with an integrated circuit fixed to a PCB via interconnections made up of connectors, traces and sockets. Only the analog aspect of the system is being considered. The digital aspect which includes the logical architecture of the integrated circuit and the equivalent circuit of the semiconductor die will not be considered and pulse voltage generators will be used instead to imitate the digital portion sending out streams of output signal. The integrated circuit package is of the Pin Grid Array (PGA) family. Bypass capacitors and termination resistors are employed for noise suppression and for reducing unwanted reflections in the traces respectively. Input/output buffers in the integrated circuit and the plug in card are assumed to be CMOS type compatible with PCI-1 specification. The PCB is an eight layer board capable of functioning under operating frequency close to microwave region. Dominant electromagnetic interference effect occurs in the vicinity of sockets, via discontinuity and package as the conductors are usually very close together. An external power supply modeled by the feedback circuit of

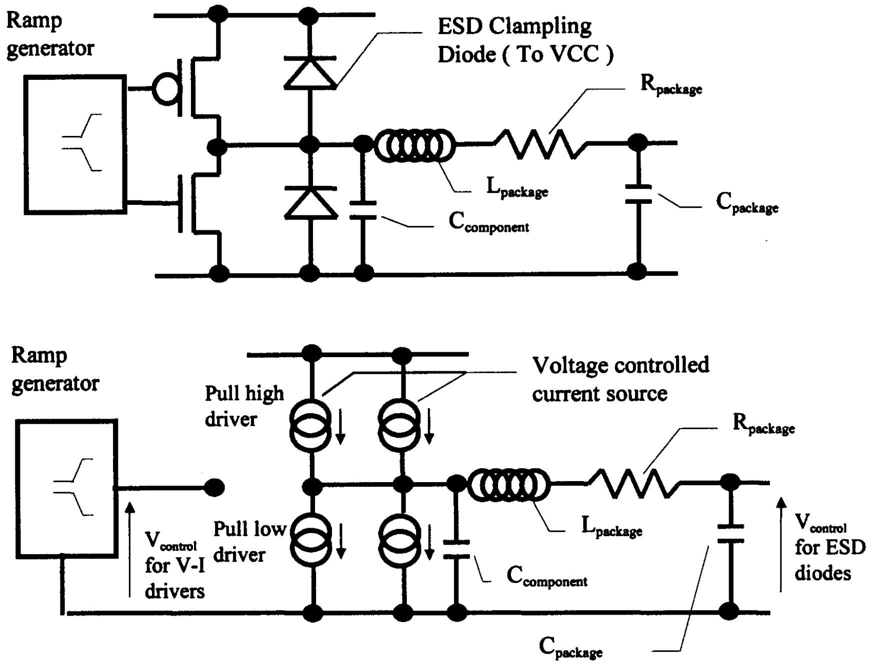


Figure 15. Schematics of output buffer and its SPICE model using Analog Behavioral Modeling.

[1] provides power to both the transceiver card and the PCB. Within the PCB, power is supplied to the IC through power planes.

A SPICE equivalent circuit for the system in Figure 17 is derived using a combination of the methods discussed. Detailed system simulation is carried out using PSPICE Version 6.1 on a IBM compatible PC. Figures 18-20 show the type of analysis that could be performed using a circuit simulator. Both time and frequency domain simulation can be performed. Figure 18 shows the normalized current distribution on the VCC plane at $t = 20ns$. Numerical value of the instantaneous current along the mesh for power planes is derived from the circuit simulator and displayed using graphical software. Note that only differential mode current is shown. The figure shows location where large transient current is concentrated in the power plane at a particular instance. This helps the designer to determine the optimum location to install decoupling capacitors and filters for EMI suppression. The

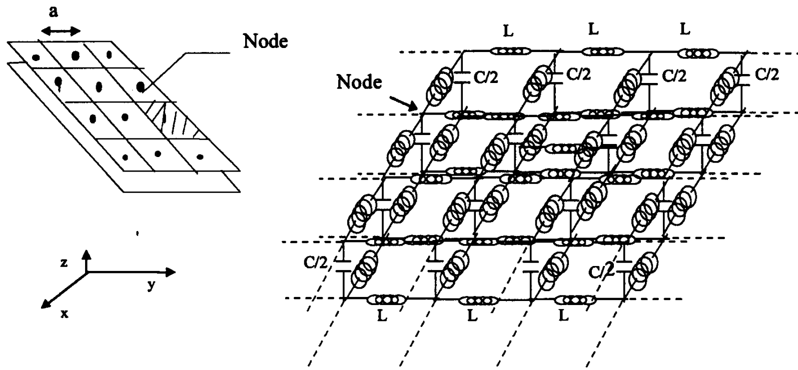


Figure 16. Equivalent circuit for a combination of VCC and GND planes

designer could also use such information to reposition the components to archive a more uniform current flow. Figure 19 shows the coupled voltage waveform on adjacent trace as seen at the input to a buffer on the die. All signal lines can be activated and the total coupled noise in each trace can be examined to ensure that noise margin of the system is not exceeded. In Figure 20 the frequency response is shown when a sinusoidal source is forced on one of the transceiver buffers while all active voltage sources are set to zero volt. From the figure, bandwidth of the interconnection can be estimated and any inherent resonance frequency in the interconnection can be pin-pointed. From Figure 20 it is seen that digital signal and its harmonics would have to be limited to 800 MHz and below to avoid oscillation.

A second simulation is run to compare the noise observed on the die within the integrated circuit. The integrated circuit is removed, in its place a device called a power validator is inserted. The multilayer PCB with socket is linked to a feedback power supply. All equivalent circuit of the system is derived using the methods described in previous sections and SPICE simulation is performed. In this case, the power validator functions as a changing load. Internal switching circuit in the power validator modulates its load impedance from low to high every $13\mu s$. The load impedance is maintained at low state for $6\mu s$ before reverting to high state. When its impedance is low the power validator draws up to 2A of transient current; and draws less than $35mA$ when

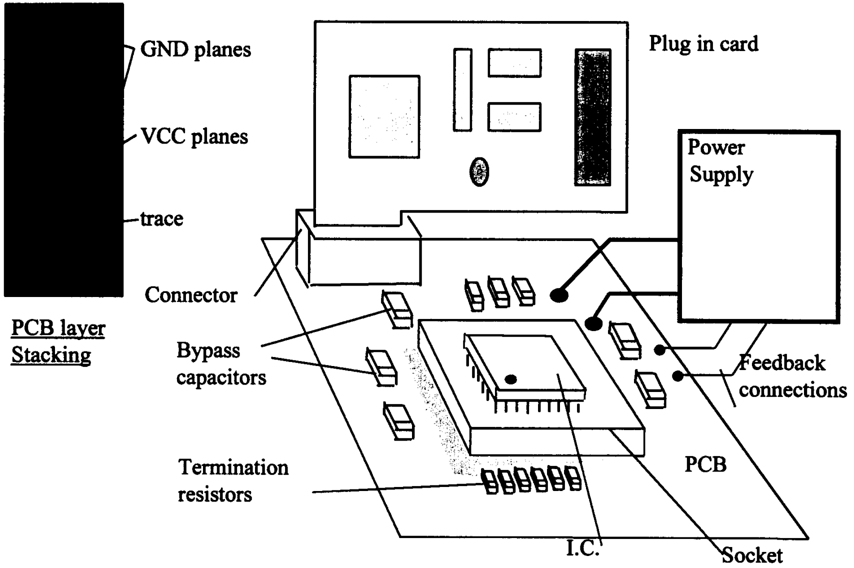


Figure 17. A digital PCB system and the cross-section of the PCB.

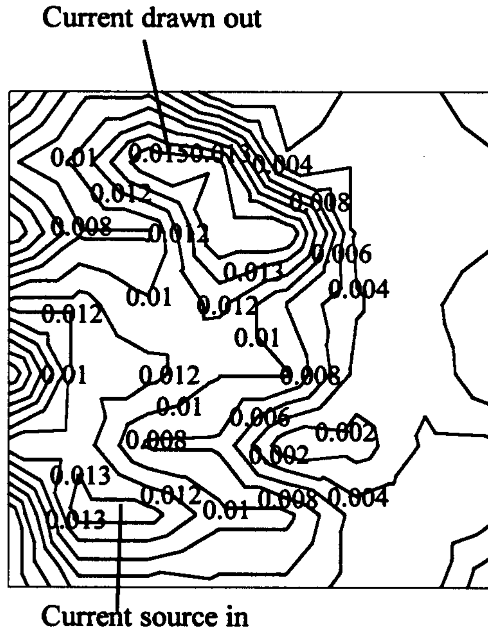


Figure 18. Normalised current on the VCC plane at $t = 20ns$.

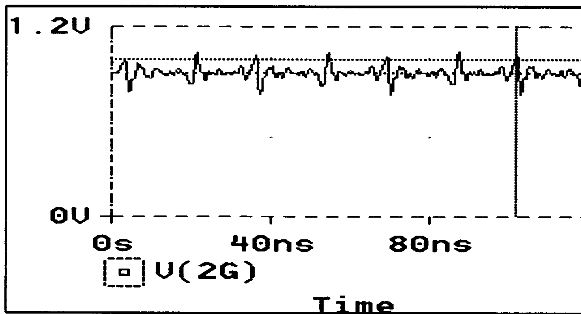
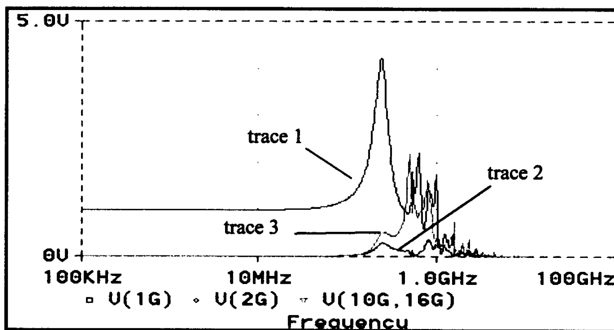


Figure 19. Coupled noise as seen on adjacent traces.



Trace 1 : Response of bond pad 1 at die
Trace 2 : Response of adjacent interconnection seen at bond pad 2
Trace 3: Response of power supply connection seen as the voltage difference between bond pad 10 (VCC) and bond pad 16 (GND)

Figure 20. Frequency response with a sinusoidal source at Transceiver No.1, and all other independent sources removed.

its impedance is high. Transition period for the load impedance is approximately $20ns$. The voltage fluctuation in VCC terminals within the power validator is probed using digital sampling oscilloscope. The measured and simulated results are compared in Figure 21. Note that both give similar trends. The positive spike corresponds to situation when the load impedance of the power validator changes from low to

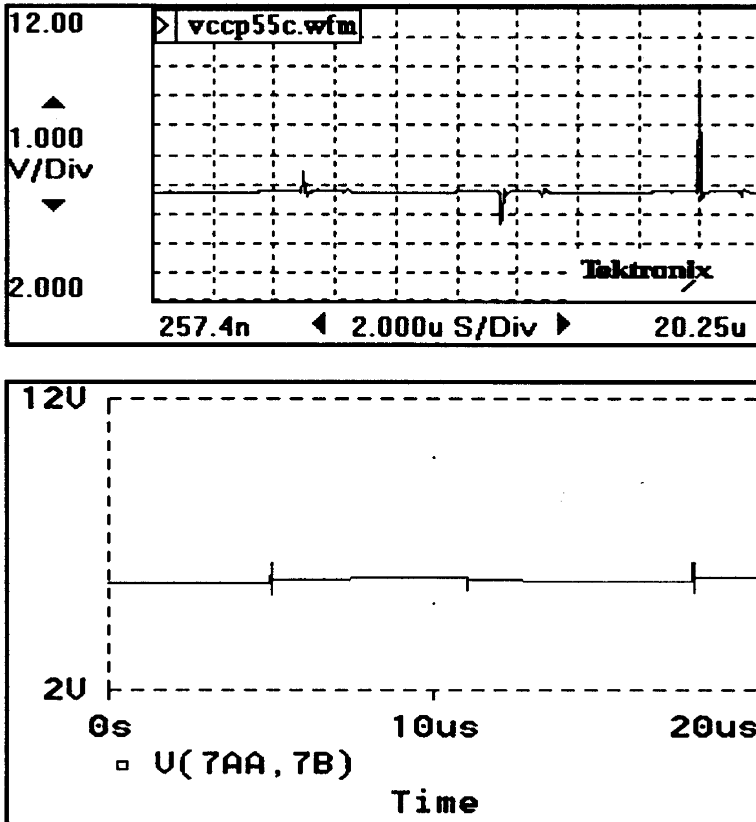


Figure 21. Comparison between measured and simulated VCC noise when a power validator replaces the actual IC.

high, and vice versa for the negative spike. The spikes occur due to non-zero impedance between the load and power supply, and the finite response time of the supply.

7. CONCLUSIONS

A system modeling and simulation approach for a high-speed PCB assembly is proposed in this article. Summarized below are limitations of this modeling approach:

(a) Differential current distribution on power planes due to electrical signal on PCB traces is not incorporated
(b) Common-mode current distribution on power planes is ignored. Unintentional radiation is largely due to common-mode current [32]. Full-wave formulation [33] would have to be employed instead of planar circuit approach in order to incorporate common mode current on the power planes.
(c) Frequency range of system only valid from d.c. to 1GHz or as long as quasi-TEM
(d) Extremely Large and complex schematics usually encounter convergence and stability problems during numerical solution in SPICE. This is due to the fact that SPICE utilizes multi-dimensional Newton-Raphson method to determine the transient solutions of nodal voltages for the non-linear network during intermediate steps. Risk of non-convergence of solutions increases when the number of nodes is large and with the presence of signals with rapid transition rate.
(e) Susceptibility analysis is not included, therefore the effect of the system when under external radiation is not investigated.

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