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MODELING OF BIPOLAR JUNCTION TRANSISTOR IN FDTD SIMULATION OF PRINTED CIRCUIT BOARD

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Abstract—A simple and efficient approximate method to incorporate nonlinear bipolar junction transistor (BJT) into Finite-Difference Time-Domain (FDTD) framework is presented. This method applies Taylor expansion on the nonlinear transport equations of the BJT based on Gummel-Poon model [5]. The results are two coupled one-step explicit finite difference schemes for the electromagnetic fields in the vicinity of the BJT, which can be solved easily. A simulation example is carried out for a power amplifier and the result compares well with the measurement. A two-step simulation scheme is introduced to hasten the process of reaching transient steady state. Finally, brief comments on treating the FDTD framework as a dynamical system is included. This perspective is useful for analyzing the stability of FDTD framework with nonlinear lumped elements.

1. INTRODUCTION

This paper proposes a simple and systematic approach to incorporate bipolar junction transistor (BJT) based on Gummel-Poon model into FDTD formulation. The Gummel-Poon model has been successfully used in circuit simulator such as SPICE [5]. It is more accurate over the older Ebers-Moll BJT model as it considers the secondary effects of the BJT device physics. Good coverage of BJT modeling using Ebers-Moll model is provided in [2, 3]. Current methods of incorporating nonlinear components in FDTD usually result in nonlinear update equations for the electric field [2–4]. This necessitates the use of Newton-Raphson method, which suffers from the possibility of non-convergent and rapidly becoming extremely complex to implement with a complicated model such as Gummel-Poon BJT model. The proposed method circumvent these problems by linearizing the I-V curve of the nonlinear component at the current operating point and use this to derive the update equations for the electric field. Following the spirit of [7], the current-voltage relationships across the base-emitter (BE) and base-collector (BC) junctions of the BJT are approximated by two variable Taylor expansion. Ignoring higher order terms leads to two update equations for the electric fields across the BE and BC junctions. It can be argued that in requiring the space and time discretization to fulfill acceptable dispersion and Courant Stability Criterion [1], the time-step is usually limited to one tenth of the period of the highest harmonics. This by itself limits the time-step to a sufficiently small value, rendering the proposed method accurate. Since it is an explicit one-step update scheme, this method is fast and suitable for modeling a system with many transistors. Together with the two-step transient simulation approach as described in Section 5, considerable time saving can be achieved. A comparison with measurement taken from a class-A BJT power amplifier verifies the accuracy of this approach.

2. THE GUMMEL-POON TRANSISTOR MODEL

The Gummel-Poon model is a charge control model. The current flowing through the BE and BC junctions of the transistor is controlled by the majority charge carrier density profile of the base region. For instance in NPN transistor, the current through BE and BC junctions will be partly determined by the integration of the hole charge density along the base. References [5] and [6] provide a complete treatment of the physics. The Gummel-Poon model accounts for the following effects: (1) Low-current drop in transistor beta or hfe due to recombination of carriers in the BE junction (2) Complete description

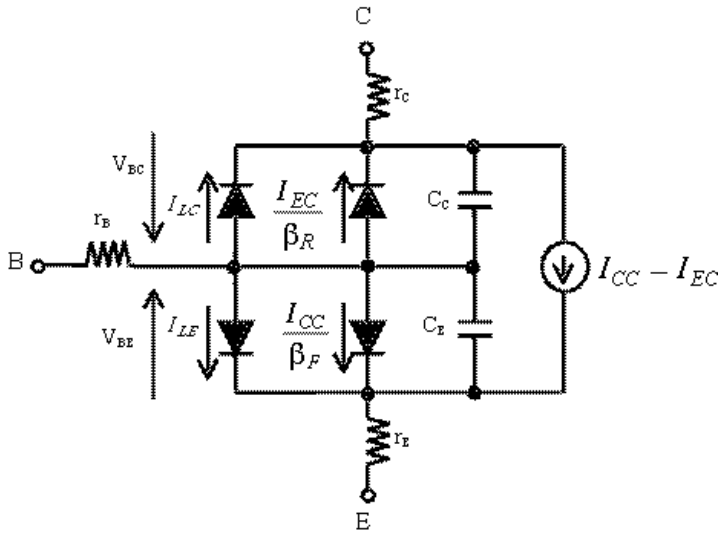

Figure 1. Gummel-Poon model for bipolar junction transistor.

of base-width modulation (also known as Early effect) (3) High-level injection during device saturation (4) Leakage current in BE and BC junction. An equivalent circuit for the Gummel-Poon BJT model for an NPN transistor is shown in Figure 1. The expressions for various diode current components are given by [5]:

$$I_{CC} = \frac{I_{ss}}{q_b}\left(\exp\left(\frac{V_{BE}}{V_{TE}}\right) - 1\right), \quad V_{TE} = n_F \frac{kT}{q} \tag{1a}$$

$$I_{EC} = \frac{I_{ss}}{q_b}\left(\exp\left(\frac{V_{BC}}{V_{TC}}\right) - 1\right), \quad V_{TC} = n_R \frac{kT}{q} \tag{1b}$$

$$I_{LE} = I_{SE}\left(\exp\left(\frac{V_{BE}}{V_{TEL}}\right) - 1\right), \quad V_{TEL} = n_E \frac{kT}{q} \tag{1c}$$

$$I_{LC} = I_{SC}\left(\exp\left(\frac{V_{BC}}{V_{TCL}}\right) - 1\right), \quad V_{TCL} = n_C \frac{kT}{q} \tag{1d}$$

$$q_b = \frac{q_1}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2} \tag{1e}$$

$$q_1 = 1 + \frac{V_{BE}}{V_B} + \frac{V_{BC}}{V_A} \tag{1f}$$

$$q_2 = \frac{I_{SS}}{I_{KF}}\left(\exp\left(\frac{V_{BE}}{V_{TE}}\right) - 1\right) + \frac{I_{SS}}{I_{KR}}\left(\exp\left(\frac{V_{BC}}{V_{TC}}\right) - 1\right) \tag{1g}$$

The junction capacitance in Figure 1 is the nonlinear capacitance due to depletion region and diffusion process. The capacitance expression is almost similar to that given by [7], except now distinction is made between BE and BC junction capacitance:

$$C_E(V_{BE}) = \tau_F \frac{\partial I_{CC}}{\partial V_{BE}} + C_{JE}\left(1 - \frac{V_{BE}}{V_{JE}}\right)^{-m_E}, \quad V_{BE} < (FC \cdot V_{JE})$$

$$\tau_F \frac{\partial I_{CC}}{\partial V_{BE}} + \frac{C_{JE}}{F_{2E}}\left(F_{3E} + \frac{m_E V_{BE}}{V_{JE}}\right), \quad V_{BE} \geq (FC \cdot V_{JE}) \tag{2a}$$

$$F_{2E} = (1 - FC)^{1+m_E}, \quad F_{3E} = 1 - FC \cdot (1 + m_E) \tag{2b}$$

$$C_C(V_{BC}) = \tau_R \frac{\partial I_{EC}}{\partial V_{BC}} + C_{JC}\left(1 - \frac{V_{BC}}{V_{JC}}\right)^{-m_C}, \quad V_{BC} < (FC \cdot V_{JC})$$

$$\tau_R \frac{\partial I_{EC}}{\partial V_{BC}} + \frac{C_{JC}}{F_{2C}}\left(F_{3C} + \frac{m_C V_{BC}}{V_{JC}}\right), \quad V_{BC} \geq (FC \cdot V_{JC}) \tag{2c}$$

$$F_{2C} = (1 - FC)^{1+m_C}, \quad F_{3C} = 1 - FC \cdot (1 + m_C) \tag{2d}$$

Observe that for both C_E and C_C, the diffusion capacitance component is only due to current across the PN junction, leakage currents I_{LE} and I_{LC} are not taken into account as these are due mainly to surface channel [5]. A brief summary of the various parameters is given as follows:

I_{ss} = transport saturation current
β_F = Ideal maximum forward beta
β_R = Ideal maximum reverse beta
n_F = Forward current emission coefficient
n_R = Reverse current emission coefficient
V_A = Forward Early voltage
I_{KF} = Corner for forward beta high-current roll-off
I_{SE} = Base-emitter leakage saturation current
n_E = Base-emitter leakage current emission coefficient
V_B = Reverse Early voltage
I_{KR} = Corner for reverse beta high-current roll-off
I_{SC} = Base-collector leakage saturation current
n_C = Base-collector leakage current emission coefficient
V_{JE} = Base-emitter built-in potential
m_E = Base-emitter P-N grading factor
C_{JE} = Base-emitter zero-bias P-N capacitance
τ_F = Ideal forward transit time
V_{JC} = Base-collector built-in potential
m_C = Base-collector P-N grading factor
C_{JC} = Base-collector zero-bias P-N capacitance

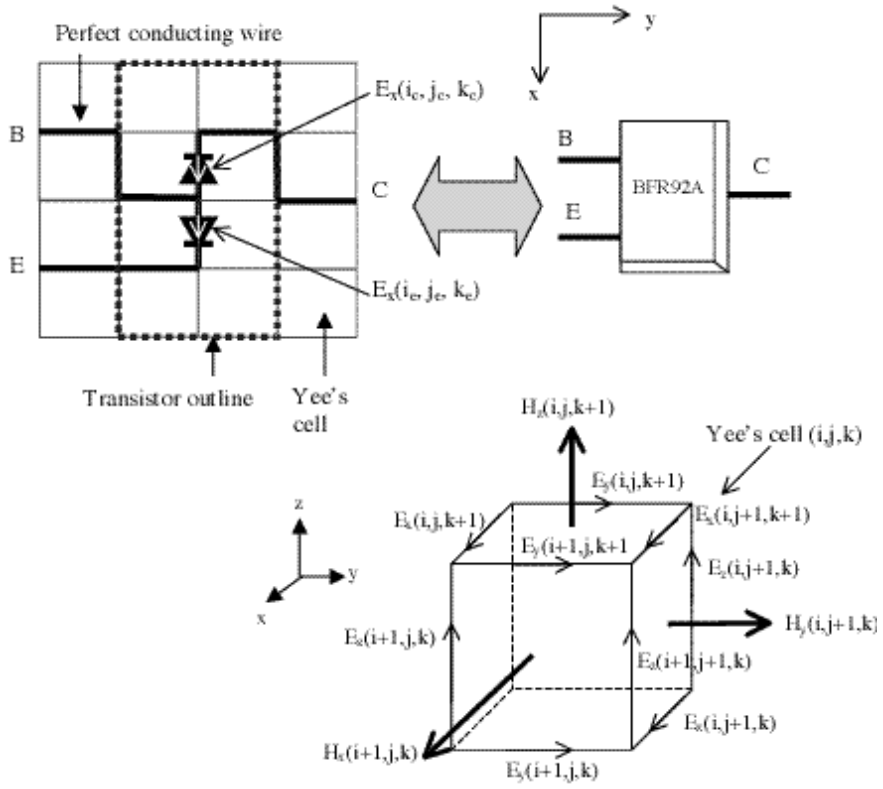

Figure 2. Modeling a SOT-23 plastic package transistor, also shown is the field convention for Yee cell.

τ_R = Ideal reverse transit time
F_C = Forward bias depletion capacitance coefficient
r_B, r_C, r_E = Base-spreading resistance, collector and emitter resistance.

3. FORMULATION

The formulation of FDTD according to Yee's leapfrog scheme is widely known and will not be elaborated [1]. The PN junctions of the BJT must coincide with one of the sides of the Yee cell. One way to model a BJT housed in a surface-mount package such as SOT-23 is illustrated in Figure 2 where the plastic enclosing the silicon is ignored. Note that in Figure 2 the convention for (x, y, z) indexes of E and H fields on the Yee cell is slightly different from [1] in order to avoid non-integer

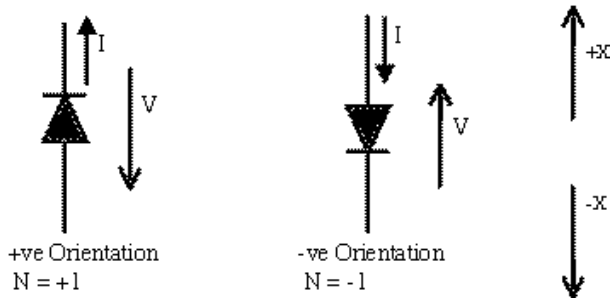

Figure 3. Positive and negative orientation of the PN junction.

indexes. For the moment let us assume both BE and BC junction to be aligned with the X-axis. From Figure 1, the total collector and emitter current can be written as:

$$\begin{aligned} I_C &= N_C\left(I_{LC}+\left(1+\frac{1}{\beta_R}\right)I_{EC}-I_{CC}+C_C\frac{dV_{BC}}{dt}\right) \\ &= N_C\left(I_{CS}+C_C\frac{dV_{BC}}{dt}\right) \qquad (3a) \\ I_E &= N_E\left(I_{LE}+\left(1+\frac{1}{\beta_F}\right)I_{CC}-I_{EC}+C_E\frac{dV_{BE}}{dt}\right) \\ &= N_E\left(I_{ES}+C_E\frac{dV_{BE}}{dt}\right) \qquad (3b) \\ V_{BC} &= N_C\cdot E_x(i_c,j_c,k_c)\Delta x \quad V_{BE}=N_E\cdot E_x(i_e,j_e,k_e)\Delta x \qquad (3c) \end{aligned}$$

N_C and N_E assume the values of $+1$ or -1 depending on the orientation of the PN junction BC and BE. This is shown in Figure 3. Thus for the example illustrated in Figure 2, $N_C=-1$ and $N_E=1$. Let V^n and I^n be voltage and current imposed on the transistor junctions at time $t=n\Delta t$. At half time step away from t, I_C can be expressed as:

$$\begin{aligned} I_C^{n+\frac{1}{2}} &= I_C\left(V_{BE}\left(t+\frac{\Delta t}{2}\right),\ V_{BC}\left(t+\frac{\Delta t}{2}\right)\right) \\ &\cong N_C\left[I_{CS}^n+\left.\frac{\partial I_{CS}}{\partial V_{BE}}\right|_{V_{BE}^n}\left(V_{BE}^{n+\frac{1}{2}}-V_{BE}^n\right)\right. \\ &\quad \left.+\left.\frac{\partial I_{CS}}{\partial_{BC}}\right|_{V_{BC}^n}\left(V_{BC}^{n+\frac{1}{2}}-V_{BC}^n\right)\right]+N_C\left[C_C^n+\left.\frac{dC_C}{dV_{BC}}\right|_{V_{BC}^n}\right. \\ &\quad \left.\left(V_{BC}^{n+\frac{1}{2}}-V_{BC}^n\right)\right]\left(\frac{V^{n+1}-V^n}{\Delta t}\right)+(\text{Higher Order Terms}) \qquad (4) \end{aligned}$$

To simplify the expression even further we ignore dC_C/dV_{BC}. Using equation (3c), $N_C^2 = 1$ and $V^{n+\frac{1}{2}} \cong \frac{1}{2}\left(V^{n+1} + V^n\right)$, equation (4) can be written as:

$$\begin{aligned} I_C^{n+\frac{1}{2}} &= N_C I_{CS}^n + \frac{\Delta x}{2}\frac{\partial I_{CS}}{\partial V_{BC}} \\ &\quad \Big|_{V_{BC}^n} x + N_C N_E \frac{\Delta x}{2}\frac{\partial I_{CS}}{\partial V_{BE}}\Big|_{V_{BE}^n} y + \frac{C_C \Delta x}{\Delta t} x \end{aligned} \tag{5}$$

where $x = E_x^{n+1}(i_c, j_c, k_c) - E_x^n(i_c, j_c, k_c)$ and $y = E_x^{n+1}(i_e, j_e, k_e) - E_x^n(i_e, j_e, k_e)$. Discretizing the Ampere's Law $\nabla \times \vec{H} = J_x + \varepsilon \dfrac{\partial E_x}{\partial t}$ at the BC junction following Yee's scheme [1]:

$$\begin{aligned} \nabla \times \vec{H}_C^{n+\frac{1}{2}}(i_c, j_c, k_c) &= \frac{{I_C}^{n+\frac{1}{2}}}{\Delta y \Delta z} + \frac{\varepsilon}{\Delta t}\left(E_x^{n+1}(i_c, j_c, k_c) - E_x^n(i_c, j_c, k_c)\right) \\ &= \frac{I_C^{n+\frac{1}{2}}}{\Delta y \Delta z} + \frac{\varepsilon}{\Delta t} x \end{aligned} \tag{6}$$

where

$$\begin{aligned} \nabla \times \vec{H}_C^{n+\frac{1}{2}}(i_c, j_c, k_c) &= \frac{H_z^{n+\frac{1}{2}}(i_c, j_c, k_c) - H_z^{n+\frac{1}{2}}(i_c, j_c - 1, k_c)}{\Delta y} \\ &\quad \frac{H_y^{n+\frac{1}{2}}(i_c, j_c, k_c) - H_y^{n+\frac{1}{2}}(i_c, j_c, k_c - 1)}{\Delta z} \end{aligned}$$

Substituting (5) into (6) for $I_C^{n+\frac{1}{2}}$, the following linear equation is obtained:

$$B_1 x + C_1 + E_1 y = 0 \tag{7}$$

where

$$\begin{aligned} B_1 &= \frac{\Delta t \Delta x}{\varepsilon \Delta y \Delta z}\left(\frac{1}{2}\frac{\partial I_{CS}}{\partial V_{BC}}\Big|_{V_{BC}^n} + \frac{C_C^n}{\Delta t}\right) + 1 \\ C_1 &= \frac{\Delta t N_C}{\varepsilon \Delta y \Delta z} I_{CS}^n - \frac{\Delta t}{\varepsilon}\left(\nabla \times \vec{H}_C^{n+\frac{1}{2}}\right) \\ E_1 &= \frac{\Delta t \Delta x N_C N_E}{2\varepsilon \Delta y \Delta z} \cdot \frac{\partial I_{CS}}{\partial V_{BE}}\Big|_{V_{BE}^n} \end{aligned}$$

Similar procedures are carried out for emitter current I_E, the resulting linear equation is:

$$B_2 x + C_1 + E_2 y = 0 \tag{8}$$

where

$$\begin{aligned} B_2 &= \frac{\Delta t \Delta x N_C N_E}{2\varepsilon \Delta y \Delta z} \cdot \left.\frac{\partial I_{ES}}{\partial V_{BC}}\right|_{V_{BC}^n} \\ C_2 &= \frac{\Delta t N_E}{\varepsilon \Delta y \Delta z} I_{ES}^n - \frac{\Delta t}{\varepsilon}\left(\nabla \times \vec{H}_E^{n+\frac{1}{2}}\right) \\ E_2 &= \frac{\Delta t \Delta x}{\varepsilon \Delta y \Delta z}\left(\frac{1}{2}\left.\frac{\partial I_{ES}}{\partial V_{BE}}\right|_{V_{BE}^n} + \frac{C_E^n}{\Delta t}\right) + 1 \end{aligned}$$

$$\begin{aligned} \nabla \times \vec{H}_E^{n+\frac{1}{2}}(i_e, j_e, k_e) &= \frac{H_z^{n+\frac{1}{2}}(i_e, j_e, k_e) - H_z^{n+\frac{1}{2}}(i_e, j_e - 1, k_e)}{\Delta y} \\ &\quad \frac{H_y^{n+\frac{1}{2}}(i_e, j_e, k_e) - H_y^{n+\frac{1}{2}}(i_e, j_e, k_e - 1)}{\Delta z} \end{aligned}$$

Equations (7) and (8) can be solved simultaneously to yield the update equation for electric fields across the BE and BC junctions of the BJT.

$$E_x^{n+1}(i_c, j_c, k_c) = E_x^n(i_c, j_c, k_c) + \frac{C_1 E_2 - C_2 E_1}{B_2 E_1 - B_1 E_2} \tag{9a}$$

$$E_x^{n+1}(i_e, j_e, k_e) = E_x^n(i_e, j_e, k_e) + \frac{B_1 C_2 - B_2 C_1}{B_2 E_1 - B_1 E_2} \tag{9b}$$

The update equations for magnetic fields surrounding the BE and BC junctions are given by:

$$\begin{aligned} &H_y^{n+\frac{1}{2}}(i, j, k) = H_y^{n-\frac{1}{2}}(i, j, k) \\ &-\frac{\Delta t}{\mu}\left[\frac{E_x^n(i, j, k+1) - E_x^n(i, j, k)}{\Delta z} - \frac{E_z^n(i+1, j, k) - E_z^n(i, j, k)}{\Delta x}\right] \end{aligned} \tag{10a}$$

$$\begin{aligned} &H_z^{n+\frac{1}{2}}(i, j, k) = H_z^{n-\frac{1}{2}}(i, j, k) \\ &-\frac{\Delta t}{\mu}\left[\frac{E_y^n(i+1, j, k) - E_y^n(i, j, k)}{\Delta x} - \frac{E_x^n(i, j+1, k) - E_x^n(i, j, k)}{\Delta y}\right] \end{aligned} \tag{10b}$$

with $i \in \{i_c, i_e\}$ $j \in \{j_c, j_e\}$ $k \in \{k_c, k_e\}$

Equation (9a), (9b), together with (10a) and (10b) provide the complete description of the electromagnetic fields in the vicinity of the BJT. The derivation can be easily adapted for transistor with BE

and BC junctions oriented along the Y and Z axes by permutation of $\Delta x, \Delta y$ and Δz. It can even be applied for the mix orientation case, for instance when BE junction is oriented along X axis while BC junction is oriented along the Y axis.

4. AMPLIFIER MODEL

A simple class-A power amplifier is constructed on FR4 substrate printed circuit board using the schematic shown in Figure 4. The BJT employed is BFR92A, a wide-band 5 GHz NPN transistor in SOT-23 plastic package. The SPICE model supplied by the manufacturer [8] provides all the parameters needed to model the device. A precision RF signal source generating a sinusoidal signal at 800 MHz and -6 dBm power is fed to the amplifier while the output is connected to a digital sampling oscilloscope. All connectors are 50 Ohms. The amplifier is capable of power amplification up to 3.0 GHz. A frequency of 800 MHz is chosen since it is sufficiently high to demonstrate the effectiveness of this method for modeling microwave circuits yet low enough to ignore the following effects: (1) Connector mismatch (2) FR4 dielectric loss (3) Skin effect loss of the copper trace (4) The oscilloscope bandwidth (10.0 GHz effective) (5) Stray parameters of the surface mount resistors.

A versatile simulation program using FDTD approach is developed. The program comes with a graphical user interface (GUI) allowing user to 'construct' a three-dimensional model interactively. The top view of the actual power amplifier and the corresponding FDTD model as shown in the user interface is depicted in Figure 4. The discretization used is $\Delta x = 0.75$ mm, $\Delta y = 0.8$ mm, $\Delta z = 0.55$ mm and $\Delta t = 1.0$ ps, 77 cells along X axis, 28 cells along Y axis and 11 cells along Z axis. First order Mur absorbing boundary condition (ABC) is employed at the model edge.

5. TWO STEPS TRANSIENT SIMULATION

Since the model contains large capacitance, notably the decoupling capacitor C_{dec} and the coupling capacitors C_{C1}, C_{C2}, the actual simulation is performed in two steps. Without this scheme it would otherwise requires hundreds of thousands of time-steps to reach the transient steady state. In the first step (also known as d.c. simulation) simulation is performed with all the capacitors within the circuit removed. This includes the nonlinear capacitance in the BJT. The sinusoidal source is also replaced with a short circuit while the system is energized by a step voltage source representing the 5 V supply. Once

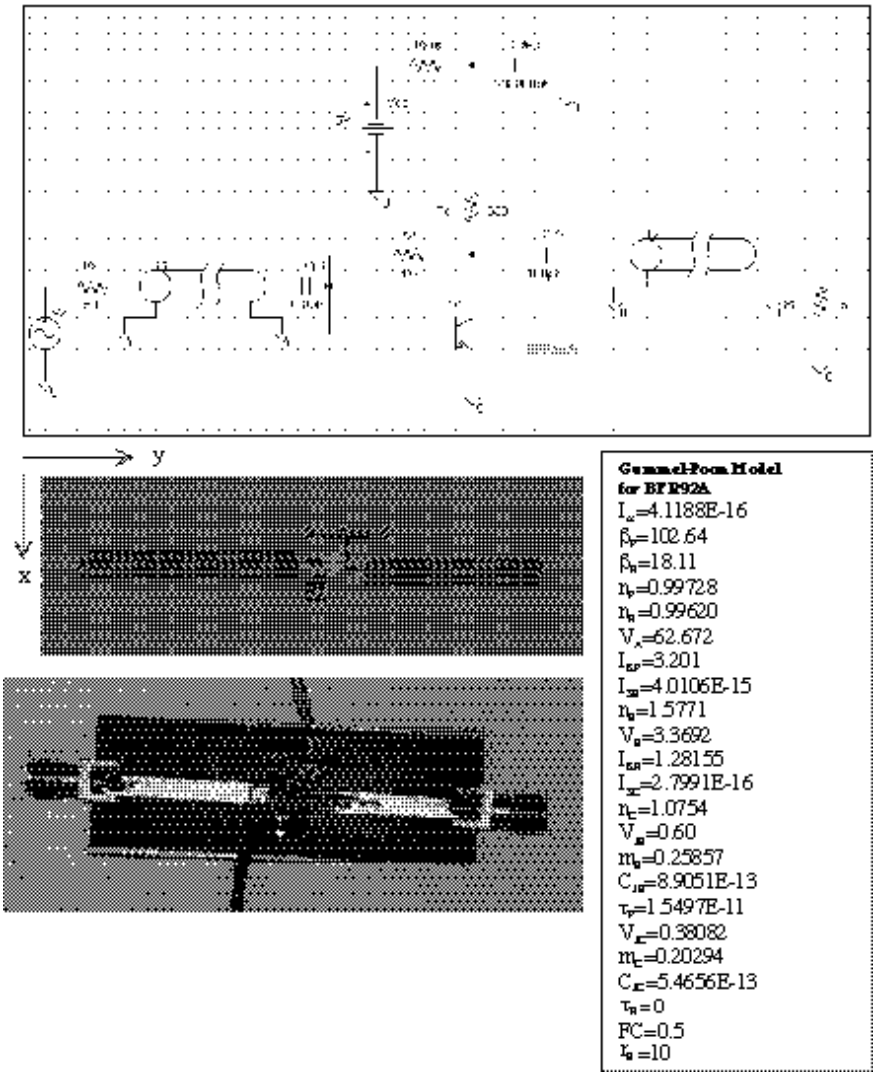

Figure 4. Top view of the power amplifier, FDTD model and actual printed circuit board.

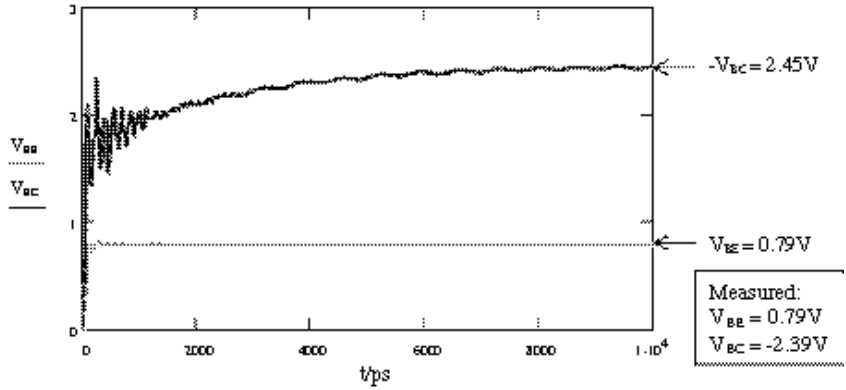

Figure 5. Simulated voltage waveforms for d.c. simulation. Also shown are the measured values.

steady state is reached, the electric and magnetic fields on each Yee cell are used as the initial value for the second step, the transient simulation. During the transient simulation all capacitors and the sinusoidal source are activated. This procedure is similar to the approach used by the SPICE computer program [5] for the transient analysis of electronic circuits.

6. COMPARISON BETWEEN THE SIMULATION AND THE MEASUREMENT

Figure 5 shows the voltage across the BE and BC junction of the BJT during d.c. simulation. Note that only 10 nanosecond or 10000 time-steps are required to reach d.c. steady state. Comparison of collector and base voltage with measurement is also included. Figure 6 shows the voltage at the load resistor R_L after running transient simulation for 340 nanoseconds. Both time domain and frequency domain values are shown. A good match between the measurement and the simulation is obtained. Total time-steps requirement is 350,000. Skipping the d.c. simulation and directly running the transient simulation would require more than one million time-steps to reach the transient steady state. A time saving of more than 50% in terms is achieved.

7. COMMENTS ON STABILITY

A system modeled by FDTD can be thought of as a discrete dynamical system [9]. The current electric and magnetic field components of the

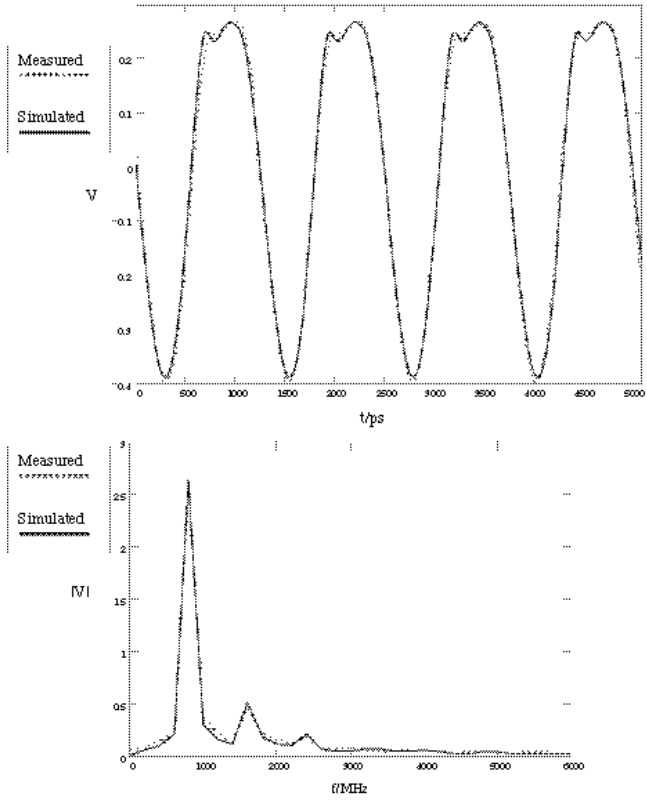

Figure 6. Simulated versus measured voltage waveform and spectrum across load resistance for transient simulation.

system depend only on previous step values. This can be seen from the update equations for dielectric region and lumped components such as resistor, capacitor [2], diode [7] and BJT as shown here. Therefore the state variables of this system are the electric and magnetic components. From the state variables we can compute secondary quantities such as the energy of the system. If we can show that the energy of the system is always bounded for a power signal, then we can argue that the system will be stable. A mathematical treatment of this subject is beyond the scope of this paper. Nevertheless, properly formulated lumped components will not contribute net energy to the FDTD system (except for source). The components will either absorb energy or absorb and release the energy as in reactive elements. Hence a system with properly formulated nonlinear components will be inherently stable. However these nonlinear components will generate harmonics. It is

seen that absorbing boundary condition (ABC) implemented at the edge of the model domain will become less effective for the high frequency signals [10]. The high frequency signal reflects against the numerical boundary and grows exponentially as the simulation proceeds, resulting in instability. Thus proper formulation and effective ABC at high frequency are the keys to long term stability of the system. Using the current method and model shown in Figure 4, numerical experiments indicate that it is dynamically stable up to 25 GHz using Mur's first order ABC.

8. CONCLUSIONS

In this paper an efficient and practical scheme for FDTD modeling of BJT based on Gummel-Poon model is proposed. The method is stable and accurate for reasonably small time discretization as indicated by the comparison with measurement. The scheme can be easily integrated into a FDTD program to model a practical BJT in a printed circuit board environment. This method can be extended to model other active components with complicated equivalent circuit. The Gummel-Poon model for the BJT can be further enhanced by incorporating more secondary effects such as the change of base-spreading resistance with current, distributed BE capacitance, τ_F modulation etc. [5]. These are omitted as they are assumed to have little effect on the BJT model used in this paper.

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