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TRANSIENT ANALYSIS OF MICROSTRIP-LIKE INTERCONNECTIONS GUARDED BY GROUND TRACKS

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Abstract—Guarded ground tracks are extensively used in high density routing for mitigation of crosstalk. However, these ground tracks can influence the electrical properties of the interconnect line also. We present a novel analytical model for extraction of line parameters of high-speed interconnect lines guarded by ground tracks. Based on the proposed model, transient response of such interconnect structures is presented. It is seen ground tracks can significantly affect the time-domain response of the interconnect lines. The computed interconnect circuit parameters are compared with finite-difference time-domain simulations. The proposed model can be practically used for time-domain analysis of microstrip lines also. The results obtained would be useful in design of high-speed interconnections for MCM, RF and MIC related applications.

1. INTRODUCTION

The important considerations in the design layouts for high-speed interconnections are signal integrity as well as mitigation of crosstalk. A typical high frequency integrated circuit has 0.5 mm of pin to pin spacing. With bends and vias being present in a routing topology, the adjacent microstrip like lines can couple with each other. It is also possible that the signal overshoots and undershoots at the terminal output may get aggravated due to area constraints. Ground tracks adjacent to high-speed interconnections are often used for reduction of crosstalk in a variety routing topologies [1, 2] and high-speed mixed signal systems [3–6]. While full-wave spectral domain analysis for crosstalk reduction using additional ground tracks has been discussed in detail [7]; the effect of such ground tracks on the propagation delay of the interconnect line itself is usually lost sight of. From the point of view of multichip system design, a parametric study of the effect of these grounds tracks on the delay prediction in high-speed interconnects is imperative.

A microstrip line is an inhomogeneous transmission line structure that consists of a strip conductor on a flat dielectric substrate with a metallic ground plane on its reverse side. Traditionally, it is found that the line parameters of a microstrip line are related to width of the strip, height of the substrate and the dielectric constant of the substrate. However in the presence of ground tracks, the interconnect circuit parameters change significantly due to modified boundary conditions offered by these ground tracks. Although the placement of ground tracks reduces the crosstalk between closely spaced signal and data lines in a multichip environment, it may severely penalize the propagation delay time of such structures. This phenomenon is not reported in the available literature and thus forms the basic motivation for our work.

In this paper, we present time-domain analysis of a microstrip-like interconnect line with adjacent ground tracks. The interconnect line is represented by a second-order equivalent circuit, whose circuit parameters are extracted using variational technique [8, 9], which offers a relatively simple approach for the solution of such type of problems, and verified using FDTD simulations. Standard transfer function technique is then used to obtain 50% delay and 90% rise time. The analytical model for the interconnect transmission line impedance with ground tracks leads to an easy estimation of line inductance and capacitance suitable for delay and transient analysis of the interconnect structure by a suitable circuit simulator such as PSPICE. The equivalent delay parameters are obtained using PSPICE.

The proposed study may find applications in design and analysis of high-speed transmission line interconnects [10–15], which are essential design units in MICs, RFICs, and MCM and in novel transmission line and interconnect structures [17–30].

The organization of the paper is as follows: In Section 2, we propose the theory for extraction of circuit parameters of a microstrip-like interconnect line flanked by ground tracks on either side. The equivalent interconnect parameters are then calculated and are compared with FDTD simulations in Section 3. SPICE computed results for 50 % delay time (τ_d) and 90 % rise time (τ_r) is also presented in this section. The paper concludes in Section 4.

2. THEORY

Figure 1 shows the cross-section of the interconnect line which is at the centre over a ground plane at the bottom and resembles a standard microstrip-like structure. In order that the interconnect line carrying signal is isolated, grounded metallic traces have been placed on both sides of the line. The interconnect line is assumed to be very thin having a width 'w'. The thickness of the dielectric (lower region) is b_2 having a permittivity ε_2. The ground tracks, coplanar with the interconnect line, has a separation 'd' from the line on both sides. The interconnect line, therefore, sees grounded planes both below vertically and sideways laterally.

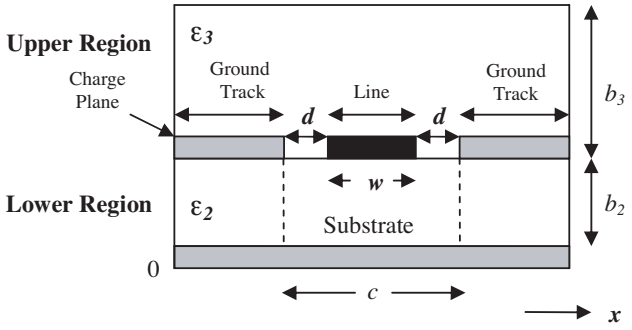

Figure 1. Lateral view of the interconnect structure.

The standard technique for determining the line capacitance is explained in details by authors in [8] and is reproduced in the Appendix and hence only salient steps leading to the variational formula for the capacitance are presented here. The variational expression for the capacitance of the interconnect structure, as shown in Fig. 1, is given

by

$$C = \frac{(1+0.25A)^2}{\sum_n \left((L_n + AM_n)^2 P_n / Y\right)} \tag{1}$$

where

$$\begin{aligned}
L_n &= \sin(\beta_n w/2) \\
M_n &= (2/\beta_n w)^3 \left[\begin{array}{l} 3\left\{(\beta_n w/2)^2 - 2\right\}\cos(\beta_n w/2) \\ +(\beta_n w/2)\left\{(\beta_n w/2)^2 - 6\right\}\sin(\beta_n w/2) + 6 \end{array} \right] \\
P_n &= (2/n\pi)(2/\beta_n w)^2 \\
\beta_n &= n\pi/c \\
A &= -\frac{\sum_{n\ odd} (L_n - 4M_n)\, L_n P_n / Y}{\sum_{n\ odd} (L_n - 4M_n)\, M_n P_n / Y} \\
n &= 1,\, 2,\, 3 \ldots \infty
\end{aligned}$$

Note that in Equation (1) the only parameter that needs to be determined is the admittance Y at the charge plane. To compute the admittance Y, we take shield walls (both lateral and top) in the upper region at very large distance to simulate open boundary conditions of an open microstrip structure and electric walls in the specified physical distance in the lower region. The admittance of the lower region in Fig. 2 is given by

$$\begin{aligned}
Y_{Lower,n} &= \varepsilon_0 \varepsilon_2 \coth(\beta_n b_2) \\
\beta_n &= n\pi/c \\
c &= 2.d + w
\end{aligned} \tag{2}$$

where, ε_2 and b_2 is the permittivity and height of the dielectric layer, respectively, and is computed for odd values of n excluding $n = 0$. The distance c is shown by dotted lines. The admittance of the upper region is given by

$$\begin{aligned}
Y_{Upper,n} &= \varepsilon_0 \varepsilon_3 \coth(\beta_n b_3) \\
\beta_n &= n\pi/c' \\
c' &\gg w \\
b_3 &\gg b_2
\end{aligned} \tag{3}$$

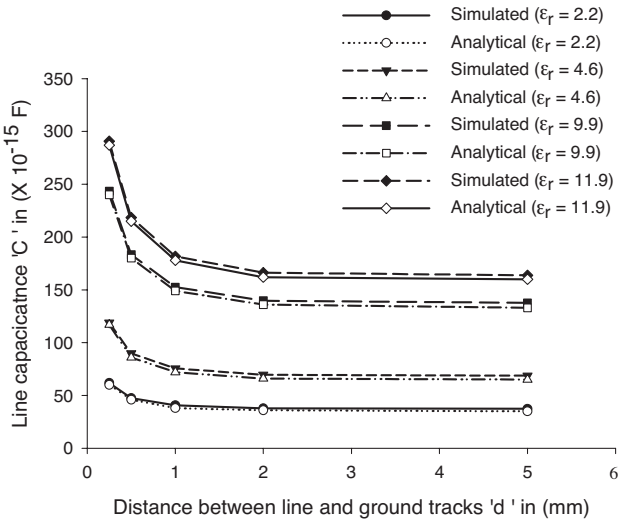

Figure 2. Line capacitance versus line to ground track separation 'd' ($w = 1\,\text{mm}$, $b_2 = 0.79\,\text{mm}$).

where, ε_3 and b_3 is the permittivity and height of the dielectric layer (upper region), respectively and is computed for even values of n excluding $n = 0$. Here c' is a variable distance and is kept much greater than the line width 'w'. Substituting Equations (2) and (3) in (1), we compute the line capacitance for these two regions; C_{Lower} and C_{Upper}, respectively.

The total capacitance of the interconnect structure would now be a summation of C_{Lower} and C_{Upper}. The capacitance formula given by Equation (1) is applicable to any single conductor stripline-like transmission line interconnects with one or more dielectric layers. If the interconnect has a small but finite thickness 't', Equation (1) can still be used by replacing Y in Equations (2) and (3) by Y/h (β_n, t) as reported in [8, 9]. The expression for h (β_n, t) for the structure considered is given by

$$h(\beta_n, t) = \frac{1}{2}\left[1 + \frac{\sinh\{\beta_n(b_2 - t)\}}{\sinh\{\beta_n b_2\}}\right] \tag{4}$$

The results are obtained through quasi-static analysis and are valid for $h/\lambda_g \leq 0.02$, where h is the thickness of the substrate (in this case b_2) and λ_g is the guide wavelength. The line inductance (L) of a interconnect line can be computed using standard formulae [8, 9] and

is given by

$$L = 1/(v^a)^2 C_a \tag{5}$$

Here, ν^a is the velocity of propagation in air and C_a is the capacitance of the line with all dielectrics replaced by air. As is seen in the above expressions, we propose a simple methodology to extract circuit parameters of an interconnect line guarded by ground tracks. The proposed design model is versatile and can qualitatively be used to analyze microstrip lines also. It can be seen as the separation 'd' increases, the admittance parameter Y_{Lower} modifies and formulation given above reduces to the basic microstrip formulation. The results are valid for a range of dielectric substances. It may be of interest to the readers that the proposed analysis is quasi-static in nature and is thus valid for low frequency applications. However, the results obtained in this paper are accurate up to 5–7 GHz, which incidentally happens to be the frequency of interest in current high-speed interconnects. The novelty of our work lies in the calculation of new admittance parameters (as given by equations (2) and (3)) which are obtained due to the modified boundary conditions as discussed above.

Out of all the analytical methods, the variational method treats the dielectric boundary conditions in a generalized way. Thus it is possible to analyze multilayer microstrip lines also without much difficulty. The accuracy of this method is insensitive to the choice of the trial function (discussed in the Appendix). Thus it is possible to take into account all the dielectric boundary conditions no matter how many planar boundaries exist in these lines [8].

The method is based on the calculation of the line capacitance by the static field theory, and, therefore it is an approximation to the EM theory. Unlike conformal mapping and other analytical techniques — which are also the static field theory — the analytical treatment of multiple boundaries is easier by the variational method [8, 9]. The computational time is also far lesser than other techniques. All of this makes the variational method combined with the transverse transmission line technique a natural choice for analysis of the interconnect structure discussed in our paper. In the following section we present the results obtained from the above discussions.

3. RESULTS

Figure 2 gives a plot of line capacitance C versus line to ground distance 'd' for the interconnect structure shown in Fig. 1 obtained using the above formulation. The results are compared *FDTD* simulations (obtained using commercially available field simulator CST Microwave

Studio) and are valid up to 5–7 GHz. The plot is obtained for a line width 'w' = 1 mm and substrate height $b_2 = 0.79$ mm. Similar results are obtained for other substrate heights also. The results are general and are valid for a range of dielectric constants ($2.2 \leq \varepsilon_r \leq 12$). The circuit parameters extracted using the proposed model closely matches with those obtained by *FDTD* simulations, thus establishing the accuracy of our technique. Note that all values are per unit length. It should be noted that the variation in the values of line inductance is marginal. However the line capacitance increases significantly as the ground tracks are brought closer to the interconnect line. Careful investigation of the interconnect structure under study can give physical insights for the variation in the values of line capacitance. In general, the line capacitance consist of three components; the overlap capacitance $C_{overlap}$, the lateral capacitance $C_{lateral}$, and the fringe capacitance C_{fr}. While the overlap and fringe components remain practically unchanged, the lateral capacitance increases substantially as the ground tracks move closer to the interconnect lines. This is attributed to the increase in the capacitance values and is shown in Fig. 3.

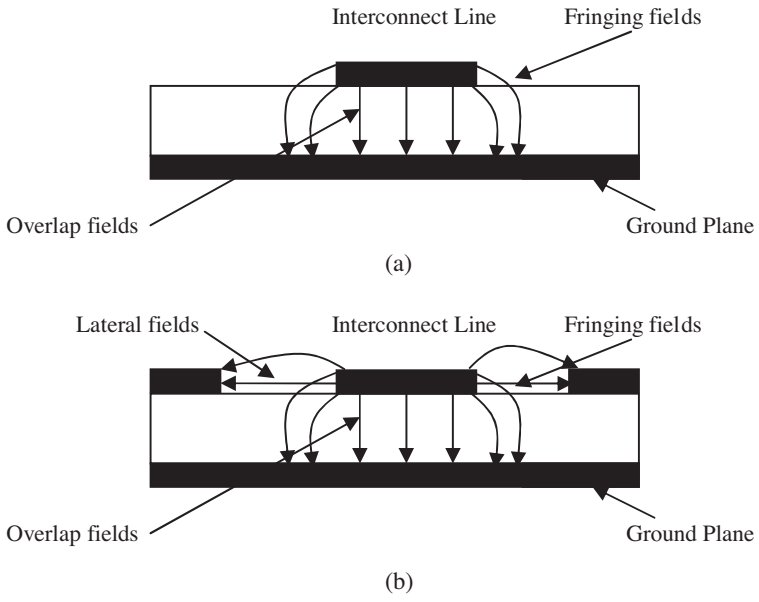

Figure 3. Field distribution in the interconnect structure with and without ground tracks. (a) Field distribution without ground tracks, (b) Field distribution with ground tracks.

High-speed interconnects are characterized by RLC parameters [16]. While the L, C values can be determined from the above technique, the line resistance (R) is purely a function of the interconnect geometry and is not affected by the presence of adjacent ground traces. For this reason we have not considered the line resistance in our analysis as it would only scale the delay values. We consider a unit step input (with a source resistance $R_S = 50\,\Omega$) and a standard $50\,\Omega$ load. The equivalent RLC circuit can now be analyzed using PSPICE simulator. The 50% delay ($\boldsymbol{\tau_d}$) and 90% rise time ($\boldsymbol{\tau_r}$) can be computed using SPICE models. These delay parameters are obtained for a variety of substrates and are given in Table 1.

Table 1. Equivalent delay parameters ($b_2 = 0.79\,\text{mm}$).

		SPICE Results			
ε_r	d (mm)	$w = 1\,\text{mm}$		$w = 0.5\,\text{mm}$	
		τ_d *(ps)*	τ_r *(ps)*	τ_d *(ps)*	τ_r *(ps)*
2.2	0.05	5.93	9.62	5.73	8.96
	0.25	5.42	8.35	5.22	7.81
	0.5	5.3	8	5.03	7.44
	1	5.23	7.88	5	7.36
	5	5.2	7.86	4.98	7.3
4.6	0.05	9.11	16.4	8.6	14.5
	0.25	8	12.98	7.53	11.66
	0.5	7.62	12.12	7.11	10.83
	1	7.55	11.84	6.97	10.53
	5	7.55	11.84	6.9	10.5
9.9	0.05	15.41	34.85	14.08	27.9
	0.25	12.68	23	11.51	19.08
	0.5	11.91	20.65	10.73	17.21
	1	11.63	19.74	10.6	16.67
	5	11.63	19.74	10.5	16.6
11.9	0.05	17.73	42.8	16.04	33.75
	0.25	14.32	27.11	12.85	21.83
	0.5	13.35	23.91	11.93	19.47
	1	13.02	22.78	11.68	18.74
	5	13.02	22.78	11.6	18.7

It is evident from Table 1, that the introduction of ground tracks alongside the interconnect lines result in tremendous increase in the

delay values. In some cases this increase is more than 30% also. This is a severe penalty on the overall performance of any electronic system. The delay values are computed for $b_2 = 0.79\,\text{mm}$. However, similar results are obtained for other substrate heights also. The increased lateral capacitance is attributed to this increase in the delay values.

4. CONCLUSION

In this paper, we present a simple method for extraction of circuit parameters and subsequent delay estimation in high-speed interconnects in a typical multichip environment. The use of ground tracks is a common design practice in any typical layout topology as it guarantees significant crosstalk reduction in coupled interconnects. This is however at the cost of increased propagation delay. The proposed study can be used in almost all routing schemes as well as in multilayer structures. The results are valid for a range of substrates and for frequencies up to 5–7 GHz.

APPENDIX A. COMPUTATION OF CAPACITANCE FOR MICROSTRIP-LIKE STRUCTURES

Consider the interconnect structure shown in Fig. 4. The Green's function $G(x,\, y/x_0,\, y_0)$ due to a unit charge located at $(x_0,\, y_0)$ satisfies Poisson's differential equation

$$\nabla^2 G(x, y/x_0, y_0) = (-1/\varepsilon)\delta(x - x_0)\delta(y - y_0) \tag{A1}$$

where, $\delta(x - x_0)$ and $\delta(y - y_0)$ are Dirac's delta functions and ε is the dielectric constant of the region containing the charge. The Green's

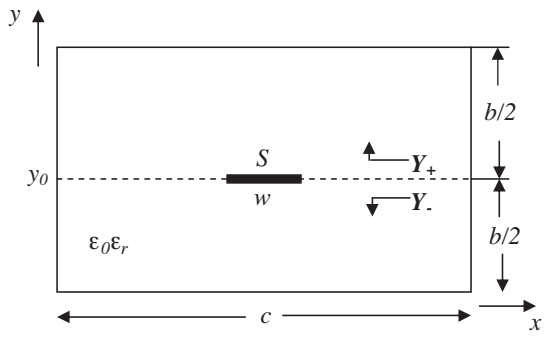

Figure 4. General microstrip-like interconnect structure.

function can be expressed as

$$G(x, y/x_0, y_0) = \sum_n \sin(\beta_n x) G_n(y), \tag{A2}$$

where,

$$\beta_n = n\pi/c$$

Substituting (A2) in (A1), $G_n(y)$ satisfies the following equation:

$$(d^2/dy^2 - \beta_n^2) G_n(y) = -(2/c\varepsilon) \sin(\beta_n x_0) \delta(y - y_0) \tag{A3}$$

Solving Equation (A3) using *transverse transmission line* method [8], we have

$$G_n(y) = (2/\beta_n c Y) \sin(\beta_n x_0) \tag{A4}$$

where, Y is the admittance at the charge plane, $y = y_0$. Here Y is the sum of admittances Y_+ and Y_-. Substituting (A4) in (A2), the Green's function at the charge plane $y = y_0$, is given as

$$G(x, y/x_0, y_0) = \sum_{n=1}^{\infty} (2/n\pi Y) \sin(\beta_n x) \sin(\beta_n x_0) \tag{A5}$$

The capacitance of the interconnect structure shown in Fig. 4 is obtained using (A5) in the following variational expression [8]:

$$\frac{1}{C} = \frac{\int_S \int_S G(x, y_0/x_0, y_0) f(x) f(x_0) dx dx_0}{\left[\int_S f(x) dx\right]^2} \tag{A6}$$

where $f(x)$ is the charge distribution on the line (S) and is given as

$$f(x) = \left(\frac{1}{w}\right)\left[1 + A\left|(2/w)(x - c/2)\right|^3\right] \text{ for } (c-w)/2 \le x \le (c+w)/2$$

and

$$= 0 \quad \text{otherwise} \tag{A7}$$

where, A is an arbitrary constant and is determined by maximizing the line capacitance C. Substituting (A5) and (A7) in (A6) and evaluating

the integral we get

$$C = \frac{(1+0.25A)^2}{\sum\limits_{n\,odd} (L_n + AM_n)^2 P_n / Y} \tag{A8}$$

where

$$\begin{aligned}
L_n &= \sin(\beta_n w/2) \\
M_n &= (2/\beta_n w)^3 \left[\begin{array}{l} 3\left\{(\beta_n w/2)^2 - 2\right\}\cos(\beta_n w/2) \\ +(\beta_n w/2)\left\{(\beta_n w/2)^2 - 6\right\}\sin(\beta_n w/2) + 6 \end{array} \right] \\
P_n &= (2/n\pi)(2/\beta_n w)^2 \\
A &= -\frac{\sum\limits_{n\ odd} (L_n - 4M_n)\, L_n P_n / Y}{\sum\limits_{n\ odd} (L_n - 4M_n)\, M_n P_n / Y}
\end{aligned} \tag{A9}$$

The characteristic impedance Z can now be computed as $Z = 1/v^a\sqrt{CC_a}$ [9]. Here, C is the capacitance per unit length of the structure, C_a is the capacitance per unit length of the structure with all dielectrics replaced by air, and v^a is the velocity of propagation in air. Due to the introduction of ground tracks, modified boundary conditions require the recalculation of the admittance Y (Y_+ and Y_-) in our case. The modified boundary conditions and the admittance parameters are given in Section 2 of the text.

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