Progress In Electromagnetics Research B, Vol. 54, 337–356, 2013

ANALYSIS, DESIGN OPTIMIZATION AND PERFORMANCE COMPARISON OF BIAS ADAPTED AND ASYMMETRICAL DOHERTY POWER AMPLIFIERS

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Abstract—Doherty type Power Amplifier (DPA) design is one of the most practical efficiency enhancement methods that provide moderate linearity. Asymmetrical device usage and employment of bias adaptation are among the most commonly used Doherty architectures in recent applications. In this paper, the efficiency performances of bias adapted DPA and asymmetrical DPA are compared based on the efficiency expression that is derived in terms of the conduction angle. The efficiency of bias adapted DPA is analyzed in terms of conduction angle of the peaking device; various bias waveforms are proposed and their effects on enhanced efficiency performance are demonstrated. This paper also facilitates an approach to determine the required relative periphery of the peaking amplifier in order to have a fully load modulated asymmetrical DPA. Both DPA structures are designed and implemented at the output power of 50 dBm with nearly 60% drain efficiencies in 6 dB load modulation region. The measurements verify the better efficiency characteristics of the bias adapted DPA and asymmetric DPA in comparison to the conventional DPA. For the first time in the literature, as a fair comparison, the performances of asymmetrical DPA and bias adapted DPA are compared on the same platform and their advantages as well as drawbacks are demonstrated using measurement results.

Received 15 July 2013, Accepted 18 September 2013, Scheduled 18 September 2013

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1. INTRODUCTION

High-efficiency power amplifiers (PAs) are the key components of modern communication systems; they form the final stage of the transmitters for transmitting high output power signals. Designing an efficient PA has a great importance particularly for the mobile systems to save power and to minimize the complexity of cooling structures. Doherty power amplifier (DPA) is a promising technique for improving the efficiency under output power backed-off conditions. The DPA has lower circuit complexity and cost effective implementation as compared to its alternatives. In W. H. Doherty's original study, the DPA was constructed on vacuum tube amplifiers [1]. The efficiency analysis of solid-state DPA in class-B/class-B configuration was reported by Raab in 1987 [2]. However, class-B/class-B realization using solid-state transistors requires driving level controlled attenuator which should have a special behavior of being shaped at least in two distinct regions with highly nonlinear characteristics [3]. In an alternative usage of DPA with solid state transistors, the carrier power amplifier (CPA) is biased in class-B and the peaking power amplifier (PPA) is biased in class-C so that it turns on the transition point. However, conventional symmetrical Doherty power amplifier (SDPA) in which the CPA and PPA employ the same periphery transistors results in reduced maximum output power due to the lack of full load modulation at the maximum drive level [4, 5]. In order to improve the performance of class-B/class-C SDPA, different techniques have been proposed and implemented. One of the most cost effective solutions is using uneven power divider in favor of the PPA [6]. Nevertheless, uneven input power division reduces the output power delivered by CPA and consequently reduces the gain at the low power levels at which only the CPA operates. The multi-way Doherty structure is another method to increase the overall performance [7–10]. However, multi-way structure results in higher structural complexity and more expensive implementation.

Two of the most popular solutions proposed to improve the performance of realizable DPA are using larger periphery transistor for the class-C biased PPA section or applying a proper bias adaptation to the PPA section [11]. The former method is called as asymmetrical Doherty power amplifier (ADPA) and has been widely used in recent applications [12–15]. The latter one is known as bias adapted Doherty power amplifier (BA-DPA) and it is realized by using an additional control circuit to change the bias condition of the peaking device from off-state to class-B. Similar to ADPA, the BA-DPA has been widely used in recent applications and promising measurement results have

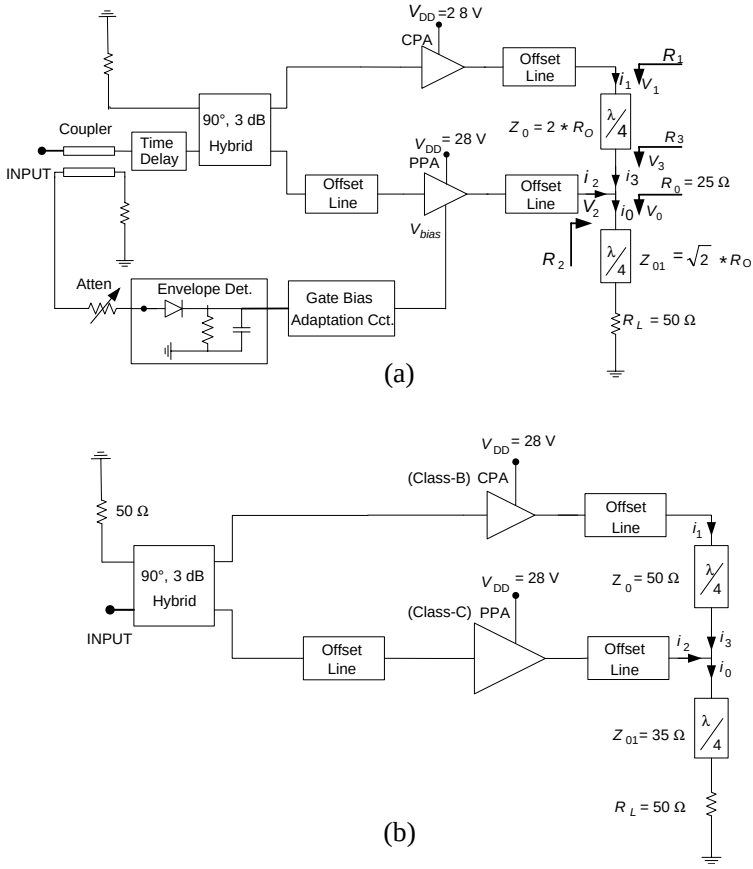

Figure 1. Doherty power amplifier structures for 6 dB load modulation region. (a) Bias adapted-DPA (BA-DPA). (b) Asymmetrical DPA (ADPA).

been reported [16–18]. The structures of the BA-DPA and ADPA are given in Figures 1(a) and (b), respectively.

In this paper, utilization of gate bias adaptation for PPA is analytically investigated and enhanced efficiency characteristic of BA-DPA in load modulation region (high power region) over ideal, class-B/class-B DPA is shown. In addition, the efficiency performance of the ADPA is investigated and the required periphery ratio of the PPA to CPA for proper Doherty operation for different load modulation regions is introduced. The conduction angle based efficiency expression is used to compare the improvements in the efficiency characteristics of the ADPA and BA-DPA. Analytically

predicted achievements are verified by the implementations of the BA-DPA, ADPA and conventional SDPA. Although the ADPA and BA-DPA methods have been widely researched and realized up to date, these applications differ with at least one aspect in terms of specific application frequency, power level and employed transistor technology. Therefore, to the authors' knowledge, a fair comparison between the ADPA and BA-DPA techniques has not been reported as yet. In this paper, optimally designed ADPA with adequate maximum conduction angle and adequate periphery PPA is compared with BA-DPA technique which was implemented at the common operation frequency, with similar output powers and by employing the same technology transistors.

2. ANALYSIS AND DESIGN OPTIMIZATION OF BA-DPA

In the BA-DPA application, peaking power amplifier (PPA) is kept on deep class-C bias with zero conduction angle up to the transition point, after which the PPA starts to conduct. After the transition point, quiescent current of the PPA is adaptively brought to class-B scheme, identical to the carrier power amplifier (CPA)'s biasing. On the other hand, the ADPA has a fixed class-C biased PPA. Thus, the conduction angles of the PPAs become an important parameter for efficiency performance. The presented efficiency analysis of BA-DPA is based on the conduction angle, $\gamma' = 2\gamma$. The efficiency analysis of BA-DPA is then extended to comprise ADPA case with appropriate periphery scaling conditions.

In both cases, the theoretical efficiency is identical to that of the ideal class-B/class-B DPA in the low power region. In the load modulation region where the actual Doherty operation is present, the range of normalized voltage factor, k can be defined as in (1), and in this region, the ideal configuration of DPA offers the efficiency as given in (2) [2]:

$$0.5 \leq k = \frac{V_O}{V_{\mathrm{DD}}} \leq 1 \tag{1}$$

$$\eta_{\mathrm{DPA}} = \frac{P_{\mathrm{RF}}}{P_{\mathrm{DC}}} = \frac{\pi}{4} k^2 \frac{1}{\left[\frac{3}{2}k - \frac{1}{2}\right]} \tag{2}$$

In the high power region, the efficiency of BA-DPA can be analyzed based on the conduction angle variation and by taking the quiescent current I_{dq} as a negative valued current for class-C amplifiers analogous to class-A/B amplifiers [19]. The drain current waveforms of

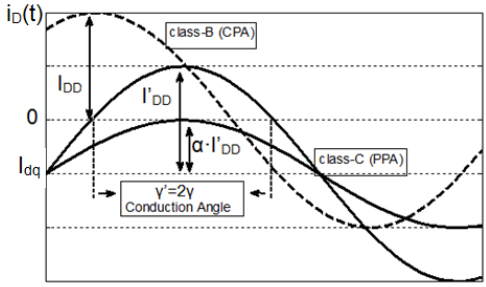

Figure 2. Drain current waveforms of CPA and PPA.

the class-B CPA (dashed line) and class-C PPA (solid lines) are given in Figure 2. In the load modulation region where both amplifiers are active, the drain current swings of the CPA and PPA are assumed to be I_{DD} and I'_{DD}, respectively. Assuming the drain current waveform of class-C biased PPA, $i'_D(t)$, with a swing of I'_{DD} is as in Figure 2, $i_{2,\mathrm{DC}}$ and V_2 can be written in terms of the drain current swing (I'_{DD}) and conduction angle ($\gamma' = 2\gamma$) as given in (3):

$$\left\{\begin{array}{l} i_{2,\mathrm{DC}} = \dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} i'_D(\theta)d\theta = \dfrac{I'_{\mathrm{DD}}}{\pi}\left\{\sin(\gamma) - \gamma\cdot\cos(\gamma)\right\} \\ |V_2| = -\dfrac{1}{\pi}\displaystyle\int_0^{2\pi} i'_D(\theta)\cdot R_2\cdot\sin(\theta)d\theta = \dfrac{I'_{\mathrm{DD}}\cdot R_2}{2\pi}\left\{2\cdot\gamma - \sin(2\cdot\gamma)\right\} \end{array}\right\} \tag{3}$$

Referring to Figure 1(a) and recalling $V_2 = V_O$, the mathematical expressions of PPA's fundamental output current, i_2, DC current, $i_{2,\mathrm{DC}}$, voltage, V_2, RF output power delivered, P_2, and DC power dissipated, $P_{2,\mathrm{DC}}$, can be given as:

$$|i_2| = \frac{|V_2|}{R_2} = \frac{I'_{\mathrm{DD}}}{2\pi}\left\{2\cdot\gamma - \sin(2\cdot\gamma)\right\} \tag{4}$$

$$P_2 = \frac{1}{2}\cdot|V_O|\cdot|i_2| = \frac{1}{2}|V_O|\frac{I'_{\mathrm{DD}}}{2\pi}\left\{2\cdot\gamma - \sin(2\cdot\gamma)\right\} \tag{5}$$

$$P_{2,\mathrm{DC}} = V_{\mathrm{DD}}\cdot i_{2,\mathrm{DC}} = V_{\mathrm{DD}}\frac{I'_{\mathrm{DD}}}{\pi}\left\{\sin(\gamma) - \gamma\cdot\cos(\gamma)\right\} \tag{6}$$

CPA is saturated in the examined region, and its output voltage is equal to the supply voltage assuming rail to rail operation from the transistor and neglecting the knee voltage effect, $V_1 = V_{\mathrm{DD}}$. Moreover, $\lambda/4$ length transmission line satisfies $Z_O = \sqrt{R_1 R_3}$ and $\alpha = 1/2$

for classical 6-dB load modulation region. In order to express the power delivered by CPA, i_3, i_1 and $i_{1,\mathrm{DC}}$ can be written as in (9) with the aid of (7) and (8) which state the power conservation on $\lambda/4$ length transmission line and proper characteristic impedance required for proper load modulation, respectively [2]:

$$|i_3|^2 \cdot R_3 = |i_1|^2 \cdot R_1 = \frac{|V_1|^2}{R_1} = \frac{V_{\mathrm{DD}}^2}{R_1} = \frac{|V_3|^2}{R_3} = \frac{|V_O|^2}{R_3} \tag{7}$$

$$Z_0 = \frac{R_O}{\alpha} = 2 \cdot R_O \tag{8}$$

$$|i_3| = \frac{1}{2}\frac{V_{\mathrm{DD}}}{R_O}, \quad |i_1| = \frac{1}{2}\frac{|V_O|}{R_O}, \quad \frac{i_{1,\mathrm{DC}}}{|i_1|} = \frac{2}{\pi} \tag{9}$$

The expressions related to the delivered RF power and consumed DC power of the CPA in the load modulation region can then be written as (10) and (11) by using the results of (9):

$$P_1 = \frac{1}{2} \cdot |V_O| \cdot |i_3| = \frac{1}{4}\frac{|V_O| \cdot V_{\mathrm{DD}}}{R_O} \tag{10}$$

$$P_{1,\mathrm{DC}} = V_{\mathrm{DD}} \cdot i_{1,\mathrm{DC}} = \frac{1}{\pi}\frac{|V_O| \cdot V_{\mathrm{DD}}}{R_O} \tag{11}$$

In order to express the efficiency of the structure, I'_{DD} available in both P_2 and $P_{2,\mathrm{DC}}$ should be written in terms of common parameters. I'_{DD} can be expressed in terms of i_2 using (4) and i_2 can be written as $|i_2| = |i_O| - |i_3|$ using the (in-phase) current conservation at the combination node of the structure. Hence, I'_{DD} can be expressed in terms of the known parameters as in (12):

$$I'_{\mathrm{DD}} = \frac{|V_O| - \frac{1}{2}V_{\mathrm{DD}}}{R_O} \cdot \frac{2\pi}{\{2 \cdot \gamma - \sin(2 \cdot \gamma)\}} \tag{12}$$

Assuming in-phase operation between the CPA and PPA as in the ideal configuration of DPA, total RF output power, DC power consumption and resultant efficiency of the BA-DPA in the load modulation region can now be easily calculated in terms of normalized voltage factor, $k = V_O/V_{\mathrm{DD}}$, and conduction angle, $\gamma' = 2\gamma$ (radians) of the PPA as given in (13)–(15):

$$P_O = P_1 + P_2 = \frac{|V_O|^2}{2 \cdot R_O} \tag{13}$$

$$\begin{aligned} P_{\mathrm{DC}} &= P_{1,\mathrm{DC}} + P_{2,\mathrm{DC}} \\ &= \frac{V_{\mathrm{DD}}^2}{R_O}\left[\frac{|V_O|}{2\pi V_{\mathrm{DD}}} + 2\left\{\frac{|V_O|}{V_{\mathrm{DD}}} - \frac{1}{2}\right\}\left\{\frac{\sin(\gamma) - \gamma \cdot \cos(\gamma)}{2 \cdot \gamma - \sin(2 \cdot \gamma)}\right\}\right] \end{aligned} \tag{14}$$

$$\eta_{\text{BA-DPA}} = \frac{P_O}{P_{\text{DC}}} = \frac{k^2}{2\left[\frac{k}{\pi} + \{2k-1\}\left\{\frac{\sin(\gamma) - \gamma \cdot \cos(\gamma)}{2 \cdot \gamma - \sin(2 \cdot \gamma)}\right\}\right]} \tag{15}$$

Efficiency of the BA-DPA was calculated in terms of conduction angle where $0 \leq \gamma \leq \pi/2$ for transition of PPA from OFF-state to class-B biasing. However, in practice, instead of conduction angle variation, gate bias voltage, V_{gs} variation is much more useful. The conduction angle can be expressed in terms of drain current as in (16) [19]:

$$\gamma = \cos^{-1}\left(\frac{I_{dq}}{I_{\text{DD}}}\right) \tag{16}$$

Then, the relation between γ and V_{gs} can be expressed as given in (17) by the aid of (16) where K is a physical constant of the transistor related to transistor's internal parameters such as channel width and length [20]:

$$\gamma = \cos^{-1}\left(\left|\frac{-K(V_{gs} - V_{TH})^2}{I_{\text{DD}}}\right|\right) \tag{17}$$

Two basic adaptation schemes were investigated in this study, but many other schemes can be proposed and examined using the efficiency equation given as (15). In the first case, efficiency characteristic with linearly changing V_{gs} and in the second case the efficiency characteristic with linearly changing conduction angle are observed. The efficiency characteristics in load modulation regions for ideal DPA and BA-DPAs deduced from (15) are given in Figure 3. Analysis and theoretical plots show that BA-DPA offers higher efficiency characteristic in load modulation region with a shallower dip than the ideal DPA.

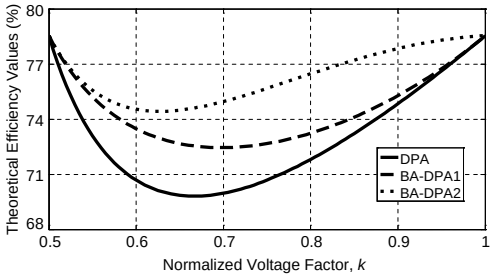

Figure 3. Theoretical efficiency characteristics in load modulation region (DPA: ideal, class-B/class-B DPA, BA-DPA1: linearly changing gate voltage adaptation, BA-DPA2: linearly changing conduction angle adaptation).

3. ANALYSIS AND DESIGN OPTIMIZATION OF ADPA

Another alternative topology of DPA is ADPA in which the different periphery devices with class-B/class-C configurations are used. The structure of the ADPA with higher periphery device in PPA section is given in Figure 1(b). In (15), the closed form of efficiency equation in terms of the conduction angle ($\gamma' = 2\gamma$) of PPA has been derived for BA-DPA in the usual 6 dB load modulation region. In BA-DPA case, full load modulation of CPA by PPA is guaranteed by adapting the biasing scheme which provides class-B condition for PPA at the maximum output power.

The class-C biased PPA that has same periphery with CPA cannot reach the output current and power of the CPA at the maximum drive level due to the insufficient driving signal. It results in the lack of full load modulation for the CPA and reduced output power of overall Doherty amplifier. Hence, the efficiency Eq. (15) is not valid for symmetrical DPA which is implemented by the same periphery devices.

If higher periphery device is used in PPA, the output current of the PPA can reach the output current of CPA at the maximum output power. Hence, the full load modulation condition can be satisfied by appropriate scaling of PPA device and this configuration is referred as ADPA. Assuming the drain current waveform of class-B biased CPA is $i_D(t)$ (dashed line) and the drain current waveform of class-C biased PPA is $i'_D(t)$ (solid lines) as shown in Figure 2. Here, the waveform with the swing of $\alpha \cdot I'_{\mathrm{DD}}$ represents the drain current of the PPA driven at the transition point after which the PPA starts to conduct and I'_{DD} represents the drain current of the PPA at the maximum driving level. The fundamental output current of CPA, namely i_1, and the fundamental output current of PPA, namely i_2, can be expressed as (18) [19]:

$$|i_1| = \frac{I_{\mathrm{DD}}}{2} \quad \text{and} \quad |i_2| = \frac{I'_{\mathrm{DD}}}{2\pi} \{2 \cdot \gamma - \sin(2 \cdot \gamma)\} \tag{18}$$

The drain current swings, I_{DD} and I'_{DD}, are proportional to the driving level, and the driving level of Doherty amplifier can be expressed in terms of normalized voltage factor, k, as in (19) with the linear operation property of DPA:

$$\alpha \leq k = \frac{V_O}{V_{\mathrm{DD}}} = \frac{V_{IN}}{V_{IN,\max}} \leq 1 \tag{19}$$

The range of load modulation region is determined by the transition point, α, after which the PPA starts to conduct. Since the PPA is class-C biased, its conduction angle is proportional to its driving level. Assuming the class-C amplifier does not reach to the

saturation level and it has constant transconductance, the conduction angle should satisfy the boundary conditions given in (20) for proper operation with adequate peripheries:

$$\left\{\begin{array}{ll}\gamma = 0, & k = \alpha\\ \gamma = \gamma_{\max}, & k = 1\end{array}\right\} \tag{20}$$

First boundary condition in (20) is defined at the transition point where the PPA is in off-state and the second boundary condition is defined at the maximum driving point where class-C PPA reaches its maximum conduction angle. Since the conduction angle of non-saturated class-C biased PPA depends on current swing, I'_{DD}, and bias point, I_{dq}, the equations given in (21) can be deduced for the same boundary conditions:

$$\left\{\begin{array}{ll}\gamma = \cos^{-1}\left(\left|\dfrac{I_{dq}}{\alpha \cdot I'_{\mathrm{DD}}}\right|\right) = 0, & k = \alpha\\ \gamma = \cos^{-1}\left(\left|\dfrac{I_{dq}}{I'_{\mathrm{DD}}}\right|\right) = \gamma_{\max}, & k = 1\end{array}\right\} \tag{21}$$

The relation between the (virtual) quiescent current and drain current swing of class-C amplifier can be deduced from Figure 2 as in (22):

$$|I_{dq}| = \alpha \cdot I'_{\mathrm{DD}} \tag{22}$$

The maximum conduction angle, $\gamma'_{\max} = 2\gamma_{\max}$, is obtained in terms of α as given in (23) by using the second boundary condition of (21) and (22):

$$\gamma_{\max} = \cos^{-1}(\alpha) \tag{23}$$

In order to satisfy full load modulation of CPA by PPA, their fundamental output currents should have the same amplitude at the maximum driving point, $k = 1$. This equality can be written as in (24) by the modification of (18) for the maximum driving point:

$$|i_2|_{\max} = \frac{I'_{\mathrm{DD}}}{2\pi}\left\{2 \cdot \gamma_{\max} - \sin(2 \cdot \gamma_{\max})\right\} = |i_1| = \frac{I_{\mathrm{DD}}}{2} \tag{24}$$

Since I_{DD} and I'_{DD} are determined by the device peripheries, necessary periphery ratio (RoP) of the PPA device to the CPA device for full load modulation can be deduced as given in (25) by using (24):

$$\mathrm{RoP} = \frac{I'_{\mathrm{DD}}}{I_{\mathrm{DD}}} = \frac{\pi}{[2 \cdot \gamma_{\max} - \sin(2 \cdot \gamma_{\max})]} \tag{25}$$

The necessary periphery ratios, (25), and corresponding maximum conduction angles, (23), for proper Doherty operation are summarized in Table 1 for different load modulation regions.

Table 1. Maximum conduction angle of PPA at $k = 1$ and required periphery ratios for different load modulation regions.

Load Modulation Region (α)	12 dB (1/2)	9 dB ($1/2\sqrt{2}$)	6 dB (1/4)
Maximum Conduction Angle, $2 \cdot \gamma_{\max}$	0.84π	0.78π	0.67π
Periphery Ratio, RoP	1.5	1.8	2.6

The efficiency characteristic of the ADPA with appropriate periphery ratio devices can be observed by using the efficiency equation given in (15). Although it has been derived for bias adapted DPA, it can also be used for a properly sized, fixed biased class-C DPA. In (15), k and γ are not independent parameters; for a class-C biased PPA with an appropriate periphery, γ can be interpreted in terms of driving level, k. For a fixed I_{dq} level class-C amplifier, γ is a function of I'_{DD} as given by (26) and I'_{DD} is proportional to the driving level, k, for a constant transconductance device [19]:

$$-I_{dq} = I'_{\mathrm{DD}} \cos(\gamma); \quad 0 \leq \gamma \leq \pi/2 \tag{26}$$

The theoretical efficiency characteristic of ADPA derived for 6 dB load modulation region with appropriate $\gamma_{\max}$ and RoP is shown in Figure 4 in comparison to the BA-DPA and ideal class-B/class-B DPA.

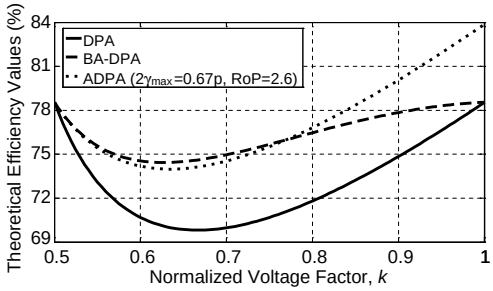

Figure 4. Theoretical efficiency characteristic of asymmetrical DPA (ADPA) with $2 \cdot \gamma_{\max} = 0.67\pi$ and RoP = 2.6 in comparison to bias adapted-DPA (BA-DPA) and ideal class-B/class-B DPA.

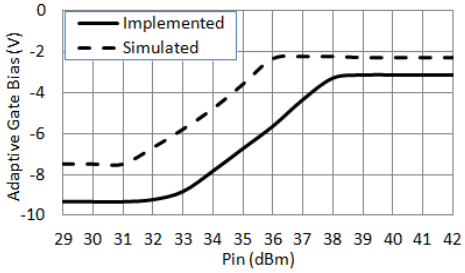

Figure 5. Bias adaptation schemes used in simulation and implementation of bias adapted-DPA (BA-DPA).

4. EXPERIMENTAL VALIDATION OF BA-DPA AND ADPA

Gallium nitride (GaN) transistors have higher current density, higher breakdown voltage and higher output power capability. They have higher efficiency, reduced C_{ds} parasitic values at high frequencies compared to the other transistor technologies. Due to these advantages, GaN on SiC transistors from Cree Inc. (Durham, USA) have been utilized in this study. The BA-DPA has been designed by using push-pull transistor (CGH40090PP) that includes 2 pieces 45 W transistor in a single package. In ADPA structure, single packaged 45 W transistor (CGH40045) for the class-AB carrier device and ∼2.6 times larger sized 120 W transistor (CGH400120) for the class-C peaking device have been utilized. For comparison purpose, a conventional symmetric DPA has been implemented by using each side of the push-pull transistor (CGH40090PP) similar to BA-DPA. Light class-AB biasing scheme for the CPA is typically preferred to the class-B in order to reduce cross over distortion, to increase overall DPA linearity and to increase the gain at the expense of slight degradation in efficiency [21]. Matching networks have been optimized for maximum efficiency within 50 MHz operational bandwidth centered at 1500 MHz.

Input power of BA-DPA is sampled by the coupler and this sampled power is used to drive the bias adaptation circuit that provides appropriate bias voltage to the PPA [18]. The linearly changing, simple bias adaptation schemes used in the simulations and implementation of the BA-DPA are given in Figure 5.

Based on the load pull simulations the optimum load impedances were determined as $Z_{L,opt} = 7.2 + j2.5\,\Omega$ and $Z_{L,opt} = 3 - j1.2\,\Omega$ for class-AB biased 45 W and class-C biased 120 W transistors, respectively. The CPA has been designed to have high efficiency in

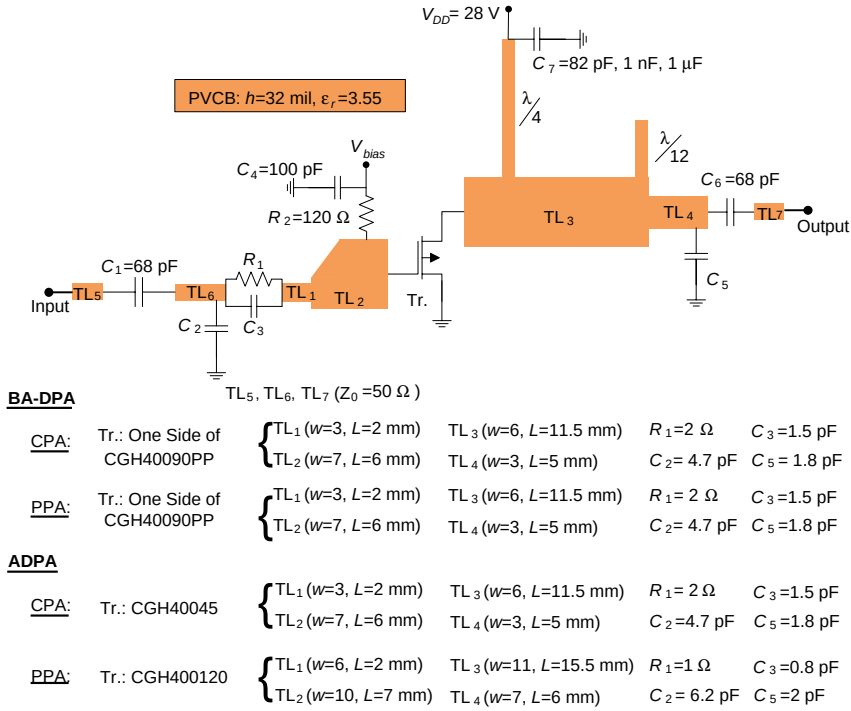

Figure 6. CPA and PPA sections of bias adapted-DPA (BA-DPA) and asymmetric DPA (ADPA).

both low power region where $Z_L = 100\,\Omega$ and high power region where $Z_L = 50\,\Omega$ [22]. Moreover, since the DPA is very sensitive to harmonic levels, 2nd and 3rd harmonic filtering is the second function of the output matching circuit. The drain bias has been provided at the end of $\lambda/4$ length stub that was shortened by using decoupling capacitors in order to reduce the memory effect as well [23]. The memory effects on PAs are spectral re-growth, IMD asymmetry and BW dependent IMD characteristics [24, 25]. In an ideal Doherty operation, in-phase power combination at the end point is easily achieved by using simple $\lambda/4$ delay line prior to PPA. However, in practice, optimum phase changes slightly with the frequency. Thus, extra delay lines called as offset lines are added into the output side of the CPA and PPA. These offset lines are used to obtain optimized efficiency from CPA and to represent high output impedance from the PPA at low power levels below the transition point. In low power region, the off-state output impedance of PPA is capacitance. It is transformed to a high resistive value by using

an offset line after its matching circuitry and power leakage from CPA is reduced to a negligible value [26]. The CPA and PPA sections that were designed and used in the simulation phases of the BA-DPA and ADPA are given in Figure 6. As concluded from the analysis carried in the previous part, the appropriately biased class-C PPA should satisfy two conditions simultaneously. It should start to conduct at the transition point where the CPA saturates and it should represent full load modulation to the CPA by providing sufficient maximum current at the peak output power level. In order to determine the most appropriate biasing level, the large signal characteristics of the ADPA such as output power, gain and efficiency have been simulated. The simulated drain efficiency and gain characteristics of the ADPA are given in Figure 7 for different biasing schemes between $V_{gs} = -4\,\mathrm{V}$ and $-5\,\mathrm{V}$. With the $-4\,\mathrm{V}$ biasing point, the peaking device starts to conduct earlier than the saturation of the carrier device and the maximum efficiency is not achievable at the transition point. On the other hand, more dip class-C biasing with $-5\,\mathrm{V}$, causes late conduction and insufficient conduction angle for peaking device resulting in lower gain at the transition point and reduced output power due to the lack of load modulation.

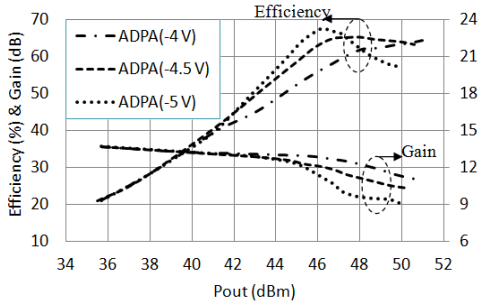

Figure 7. Simulation performances of asymmetric DPA (ADPA) with different bias points of class-C biased PPA.

The quiescent currents of the CPAs used in both DPAs have been set to 200 mA. The gate bias voltages of the PPAs in the ADPA and SDPA are $-4.6\,\mathrm{V}$ and $-4.3\,\mathrm{V}$ respectively. The pinch-off voltage of the transistors has been measured as around $-3.1\,\mathrm{V}$. The offset lines of 2 mm and 3 mm have been used at the output of PPAs in BA-DPA and ADPA respectively. The offset line of 3 mm was found to be optimum at the output of CPA sections of both DPAs. 1-tone harmonic balance simulation results given in Figure 8(a) show that both the ADPA and BA-DPA can provide enhanced efficiency over

conventional SDPA in nearly 6 dB power range between the transition point (44.5 dBm) and maximum power point (50.5 dBm). Moreover, both the BA-DPA and ADPA have ∼1.0 dB higher output power than SDPA which is not driven properly due to the same sized transistors used in class-C PPA and class-AB CPA. At the maximum power point, the efficiency degradation of the ADPA with respect to the analytical result is due to non-constant transconductance of the class-C biased PPA that starts to saturate before the maximum power level.

In the implementation phase, slight post-tunings on the layouts have been done by observing the overall responses such as output power, efficiency and gain characteristics. The fabricated ADPA and BA-DPA are shown in Figure 9. The realized ADPA and BA-DPA have been tested in terms of gain and drain efficiency characteristics as given in Figure 8(b). Although there is nearly 1 dB reduction in the maximum power level with respect to the simulation results, the measured efficiency and gain characteristics at the center frequency of 1.5 GHz have high conformance with the simulated ones. The maximum output power has been noted as 49.6 dBm. Both amplifiers have better efficiency characteristic and nearly 1 dB higher output power than the conventional SDPA. In the load modulation region of 6 dB, the efficiency of BA-DPA has very similar characteristic to ideal Doherty operation and it is above 57% through the load modulation region. The ADPA has an efficiency curve in a different shape from the ideal case but still has acceptable efficiency enhancement, between 56% and 63%, in the load modulation region. The BA-DPA has better gain characteristic because the class-C biased peaking device lowers the overall gain of the ADPA.

The linearity characteristics of the ADPA and BA-DPA have

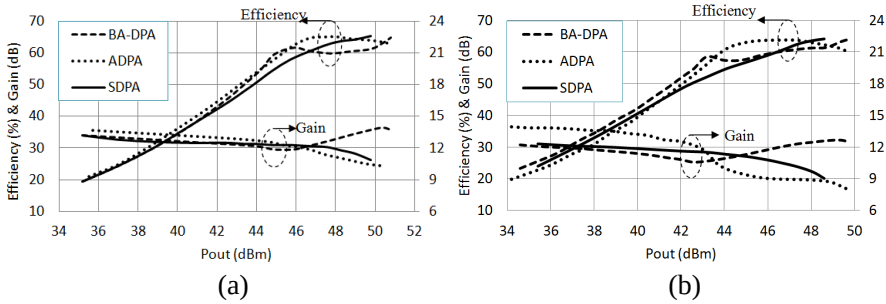

Figure 8. Drain efficiency and gain characteristics of bias adapted-DPA (BA-DPA) and asymmetric DPA (ADPA) in comparison to symmetrical DPA (SDPA). (a) Simulated. (b) Measured.

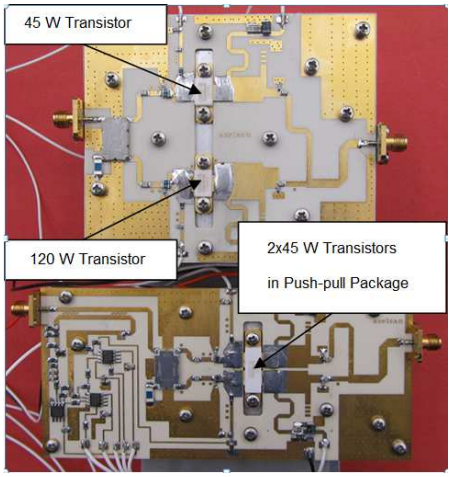

Figure 9. Photograph of the fabricated asymmetric DPA (ADPA) and bias adapted-DPA (BA-DPA).

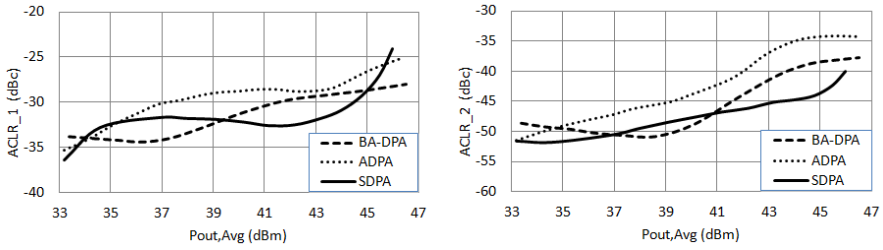

Figure 10. Measured Linearity characteristics of of Asymmetric DPA (ADPA) and Bias Adapted-DPA (BA-DPA) in Comparison to Symmetrical DPA (SDPA); W-CDMA signal with PAPR = 6.5 dB. (a) $ACLR_1$ (5 MHz offset). (b) $ACLR_2$ (10 MHz offset).

also been observed experimentally as shown in Figure 10. A single carrier wideband code-division multiple access (W-CDMA) signal with a peak-to-average power ratio (PAPR) of 6.5 dB has been applied and the adjacent-channel leakage ratio (ACLR) of the amplifiers has been measured. The BA-DPA has achieved an $ACLR_1$ (5 MHz offset) of -29 dBc and an $ACLR_2$ (10 MHz offset) of -40 dBc in the 6 dB power backed off. At the same output power level, the $ACLR_1$ and $ACLR_2$ of the ADPA have been measured as -27 dBc and -36 dBc, respectively. The linearity performances can be further improved by using the pre-

Table 2. Measured performance summary of the implemented DPAs under W-CDMA signal (PAPR = 6.5 dB).

DPA Type	$P_{out,\max}$ (dBm)	G (dB) @ $P_{out,avg}$ = 43.5 dBm	η_{avg} (%) @ $P_{out,avg}$ = 43.5 dBm	$\mathrm{ACLR}_1/\mathrm{ACLR}_2$ (dBc) @ $P_{out,avg}$ = 43.5 dBm
BA-DPA	49.6	11.4	60.5	$-29/-40$
ADPA	49.5	10.2	61.6	$-27/-36$
SDPA	48.6	10.6	56.2	$-32/-45$

Table 3. Comparison of similar topology DPAs.

Reference	[13]	[14]	[15]	[16]*	[18]	This Work
Frequency (GHz)	2.50	2.14	2.14	2.65	2.14	1.50
Pout, max (dBm)	~ 47	~ 42	~ 46.2	~ 50.5	~ 38	49.5/49.6
η^* (%)	∼52	∼48	∼44	∼56	∼40	56/57
DPA Type	ADPA	ADPA	ADPA	BA-DPA	BA-DPA	ADPA/BA-DPA

η^*(%): worst drain efficiency in 6 dB PBO region.
[16]*: three-stage DPA.

distortion techniques [27, 28].

The measurement results of the fabricated DPA structures using W-CDMA signals with a peak-to-average power ratio (PAPR) of 6.5 dB are summarized in Table 2.

Table 3 compares the performance of the fabricated DPAs in this study with those present in the literature. The comparison is based on CW performances of the amplifiers.

The measurement results verified that both the BA-DPA and ADPA structures offer well enhanced efficiency and output power characteristics with respect to the conventional SDPA. The conduction angle of the class-C biased peaking device has important role on the efficiency, gain, power and linearity characteristics of the overall Doherty amplifier. The gain degradation of the ADPA in the load modulation region where the class-C biased peaking device starts to conduct results in poorer power-added efficiency. On the other hand, BA-DPA ensures the full load modulation of the carrier device through the bias adapted peaking device, so the output power is inherently maximized.

The control circuit of the BA-DPA is the most common drawback of the structure. Although its simple implementation ensures a cost effective solution, the envelope detector and bias shaping circuit inherently limit the instantaneous (modulation) bandwidth of the amplifier. The BA-DPA with a simple control circuit as one realized here can be used for the signals whose aggregated bandwidth is up to a few MHz. However, it is not a candidate for the wideband signals like long-term evaluation signals in which the bandwidth can reach 100 MHz. On the other hand, the larger periphery transistor requirement of the ADPA avoids having a cost effective solution. It is a waste of periphery and in some extreme cases the discrete transistor with an appropriate periphery cannot be available. Furthermore, the larger periphery transistor having lower input and output impedances inherently limits the maximum operation bandwidth of the amplifier because the matching network that matched the lower impedance to the terminal impedance (50 Ω) has narrower bandwidth. The simulated and measured results have verified the bandwidth limitation of the higher periphery transistor. The targeted frequency band of 50 MHz has been achieved with only 2–3% efficiency degradation for both DPAs. However, in the wider bandwidth of 200 MHz, the efficiency degradations have been observed as 16% and 22% for the BA-DPA and ADPA, respectively.

5. CONCLUSION

In this paper, analysis of a BA-DPA in terms of its efficiency characteristic has been presented. The ideal efficiency characteristics of the BA-DPA with different bias adaptation schemes have been illustrated. The derived analytical expression has indicated that the optimized efficiency characteristics with a shallow dip in the load modulation region can be obtained by using the BA-DPA. Moreover, the maximum conduction angle and periphery requirement of the class-C biased PPA to realize fully load modulated ADPA have been investigated. The appropriate maximum conduction angles and relative peripheries for the PPA have been evaluated for different load modulation regions. The ideal efficiency characteristic of the ADPA with adequate periphery devices has been illustrated in comparison to the BA-DPA and ideal DPA. The design optimizations of the ADPA and BA-DPA based on the analytical findings have been presented for maximum efficiency criteria in the load modulation region.

In addition, for the first time in the literature, this paper has reported a performance comparison between two common DPA techniques; ADPA and BA-DPA, under the same conditions in

terms of the output power, operation frequency and employed transistor technology. The optimally designed and implemented amplifiers have verified the analytical findings by achieving enhanced efficiency performance in the load modulation region. Both amplifiers have presented well enhanced efficiency and output power over the conventional symmetric DPA. Furthermore, the analyzed and optimally designed DPA structures present higher efficiency value and better efficiency characteristics near to the ideal one with respect to those available in the literature. Other discussions such as the waste of periphery limiting the operation bandwidth for an ADPA and the bias control circuit limiting the instantaneous bandwidth for a BA-DPA have been carried based on the implementations.

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