

## DESIGN AND OPTIMIZATION OF NONUNIFORMLY SPACED LONGITUDINAL SLOT ARRAYS

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**Abstract**—A new numerical method is presented for the design and optimization of linear arrays of nonuniformly spaced longitudinal slots on the broad wall of rectangular waveguides, based on the Method of Least Squares (MLS). Elliott’s design theory for travelling-wave-fed slot arrays is extended to nonuniformly spaced slots. As a common approach in MLS, an error function is formulated according to the design goals (namely the input impedance matching and pattern synthesis) and then minimized with respect to the design parameters (namely slot lengths, offsets, spacings and excitations). Having the slot parameters, one can design a linear slot array which accounts for the desired input impedance matching and array pattern. This approach has the advantage of combining the “nonuniform pattern synthesis”, which includes the external mutual coupling and element pattern of slots, with “impedance matching” and “calculation of the array parameters”. This procedure increases the design speed as well as synthesizing any desired pattern. The MLS design results and those obtained by HFSS simulation software are in good agreement and verify the accuracy of the proposed method.

### 1. INTRODUCTION

Slot antennas are widely used in many applications as they often represent the best tradeoff between cost and performance [1–7]. In this regard, it is important to reduce the design time while maintaining the desired accuracy using computer aided procedures. Various methods of analysis for slot antennas are reported in [8–13].

Longitudinal slot arrays cut on the broad wall of the rectangular waveguide are probably the most common configuration used due to

the absence of cross polarized components compared to other types of slots [14].

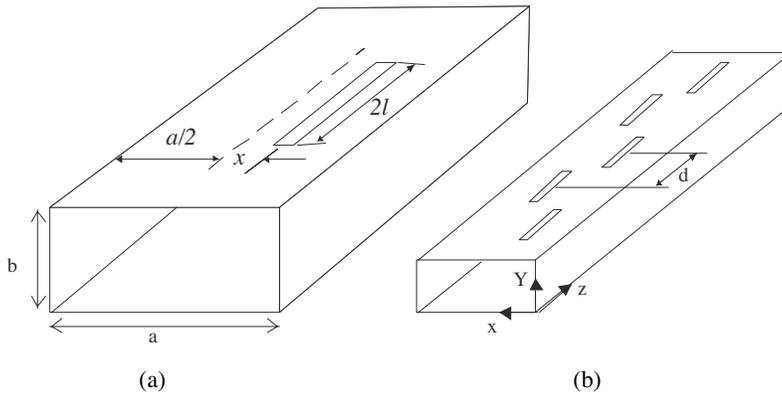
Elliott's design procedure for the slot arrays, introduces two approaches. One method is called the "standing wave feed" [15] in which the slots are equally spaced by half a wavelength and the waveguide is shorted at one end. By this procedure, the array pattern becomes broadsided and symmetrical. In the second method, the slots are still equally spaced, but not by a half a wavelength and the waveguide is terminated by a matched load. This is called the "travelling wave feed" [16]. The travelling wave feed has mainly two advantages; a nonbroadside main beam and a higher bandwidth compared to the standing wave feed.

As a further improvement, if we let the slot spacings to be unequal, due to the properties of nonuniformly spaced arrays, we expect to gain asymmetrical patterns with higher bandwidths.

Following a previous novel effort made on the design of slot arrays by the Method of Least Squares (MLS) [17], we will extend the Elliott's design theory to nonuniformly spaced longitudinal slots and use the MLS to develop an optimum design procedure. In this method an error function is constructed suitably counting for the design goals, namely impedance matching and array pattern synthesis.

## 2. THEORY

An offset narrow longitudinal slot on the broad wall of rectangular waveguide and the corresponding linear array consisting of  $N$  slots is shown in Fig. 1. The Elliott's design procedure for longitudinal slots



**Figure 1.** (a) A longitudinal slot module. (b) A linear array of  $N$  slots.

rests on the following equations [15, Chap. 8]:

$$\frac{Y_n^A}{G_0} = K_1 f_n \sin(kl_n) \frac{V_n^s}{V_n} \quad (1)$$

$$\frac{Y_n^A}{G_0} = \frac{K_2 f_n^2}{Z_n^a} \quad (2)$$

$$K_1 = -j \left[ \frac{8(a/b)}{\pi^2 \eta G_0 (\beta/k)} \right]^{1/2}, \quad K_2 = \frac{292(a/b)}{0.61\pi(\beta/k)} \quad (3)$$

$$f_n = \frac{\cos(\beta l_n) - \cos(kl_n)}{\sin(kl_n)} \sin\left(\frac{\pi x_n}{a}\right) \quad (4)$$

where  $Y_n^A/G_0$  is the normalized active admittance of the  $n$ 'th slot (with respect to  $G_0$ , the equivalent transmission line characteristic admittance of TE<sub>10</sub>),  $V_n$  is the mode voltage of the  $n$ 'th slot (in the equivalent transmission line model),  $V_n^s$  is the maximum voltage at the centre of  $n$ th slot,  $a$  and  $b$  are the internal guide dimensions,  $k$  and  $\beta$  are the propagation constants of the air and the dominant mode TE<sub>10</sub> in the waveguide, respectively and  $Z_n^a$  is the active impedance of the  $n$ 'th equivalent dipole.

Equation (1) shows that the mode voltage and slot voltage are in phase (or out of phase) if  $Y_n^A/G_0$  is pure real (The function  $f_n$  is pure real, but can be positive or negative, since  $f_n(-x_n, l_n) = -f_n(x_n, l_n)$  as inspection of Eq. (4) reveals). For the  $\lambda_g/2$  spacing of slots (standing wave feed),  $V_n$  is common to all elements in a waveguide, except for an alternation in sign, which is normally compensated for by an alternation in the direction of slot offsets. Specifying the desired pattern (so that  $V_n$ s are known) and the desired admittance level (so that  $Y_n^A/G_0$  is constrained), Eqs. (1) and (2) can be solved simultaneously to obtain the design parameters (slot offsets and lengths). Considering the traveling wave feed, the mode voltages  $V_n$  are no longer equal in magnitude and so we can not account for and compensate them in the design equations as for standing wave feed. Consequently, they should be calculated using the transmission line model of the guide. Similar to the approach used in [16] for uniformly spaced slots, we consider the equivalent circuit of Fig. 2 for the nonuniformly spaced slot array, to obtain the corresponding design equations. The slot spacings are assumed to be  $d_1$  to  $d_{N-1}$ . A matched load  $G_0$  is placed beyond the slot farthest from the feed end. For notational convenience let us take the origin of the  $z$  axis at the cross section of the  $N$ th slot with  $z$  increasing to the right in Fig. 2. Then for any length  $d_n$  of the transmission line we can write:

$$V_{in} = V_{out} \cos \beta d_n + j I_{out} Z_0 \sin \beta d_n \quad (5)$$

$$I_{in} = I_{out} \cos \beta d_n + j V_{out} G_0 \sin \beta d_n \quad (6)$$

In which  $(V_{in}, I_{in})$  is measured at a cross section  $d_n$  units of length to the left of  $(V_{out}, I_{out})$ . The total admittance seen at the cross section of slot 1 is:

$$Y_1 = Y_1^A + G_0 \quad (7)$$

Applying Eqs. (5)–(6) for slot 1, we find that:

$$I_{out} = I_1 = V_{out} Y_1 = V_1 Y_1 \quad (8)$$

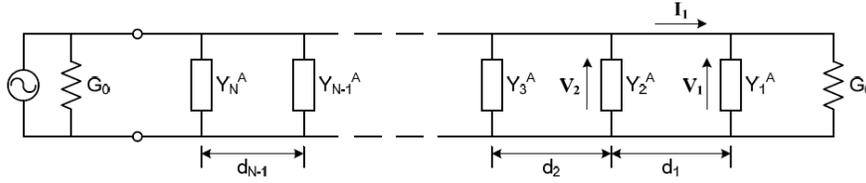
$$V_{in} = V_2 = V_1 \left( \cos \beta d_1 + j \frac{Y_1}{G_0} \sin \beta d_1 \right) \quad (9)$$

We can generalize the above equations for all the slots:

$$V_n = V_{n-1} \left( \cos \beta d_{n-1} + j \frac{Y_{n-1}}{G_0} \sin \beta d_{n-1} \right) \quad (10)$$

In which:

$$\frac{Y_{n-1}}{G_0} = \frac{Y_{n-1}^A}{G_0} + \frac{(Y_{n-2}/G_0) \cos \beta d_{n-2} + j \sin \beta d_{n-2}}{\cos \beta d_{n-2} + j (Y_{n-2}/G_0) \sin \beta d_{n-2}} \quad n > 2 \quad (11)$$



**Figure 2.** Equivalent circuit of non-uniformly spaced slot array.

Equations (1) and (10) can be combined to give:

$$\cos \beta d_{n-1} + j \frac{Y_{n-1}}{G_0} \sin \beta d_{n-1} = \frac{V_n^s}{V_{n-1}^s} \cdot \frac{f_n \sin(kl_n)}{f_{n-1} \sin(kl_{n-1})} \cdot \frac{Y_{n-1}^A/G_0}{Y_n^A/G_0} \quad (12)$$

In combination with Eq. (2), Eq. (12) completes the two final design equations.

### 2.1. Slot Arrangement

Generally, there are two common ways to arrange slots on the waveguide broad wall. The first is to place all the slots on the same

side of the center line and the second is to place them on both sides alternately. Both of these arrangements cause increasing phase due to  $\beta d_{n-1}$  (the traveling wave displacement phase) along the guide for the excitations ( $V_n^s/V_{n-1}^s$ ). But in the case of alternately spaced slots, a phase difference of  $-\pi$  is further added to the phase increase  $\beta d_{n-1}$  resulting in a more controllable pattern. Considering the latter arrangement, the array factor is written as:

$$F(\theta) = \sum_{n=1}^N \frac{V_n^s}{V_1^s} e^{jkz_n \cos \theta} = \sum_{n=1}^N \left| \frac{V_n^s}{V_1^s} \right| e^{j(z_n k \cos \theta - z_n \beta + n\pi)} \quad (13)$$

where  $z_n$  is the place of the  $n$ 'th slot and equals  $z_n = \sum_{i=1}^n d_i$ . In Eq. (13), the place of the main beam isn't necessarily equivalent to the zero phase of array factor. As a consequence the place of the main beam can't be formulated in a closed form, but we should consider it in the desired pattern.

### 3. DESIGN PROCEDURE

In the MLS design procedure, an error function is formulated according to the design goals. In the case of slot array design, we will form an error function consisting of three terms, namely one for the impedance matching, one for the Elliott's equations and the third for the pattern synthesis.

#### 3.1. Impedance Matching

Impedance matching should be achieved between the feed network and the normalized characteristic admittance ( $G_0 = 1$ ). The error function is constructed for the real and imaginary parts of  $Y_{in}$ :

$$\varepsilon_{Matching} = \varepsilon_{real} + \varepsilon_{imag} = W_1 |\operatorname{Re}(Y_{in}) - 1|^2 + W_2 |\operatorname{Im}(Y_{in})|^2 \quad (14)$$

where  $W_i$  are the weighting functions. Combining Eqs. (2) and (11) gives the input admittance (seen through the last slot, N) of the waveguide as:

$$Y_{in} = \frac{K_2 f_N^2}{Z_N^A} + \frac{(Y_{N-1}/G_0) \cos \beta d_{N-1} + j \sin \beta d_{N-1}}{\cos \beta d_{N-1} + j(Y_{N-1}/G_0) \sin \beta d_{N-1}} \quad (15)$$

### 3.2. Elliott'S Equations

In order to account for the Elliott's equations simultaneously, we will use Eqs. (2) in (12). Summing over the slots 2 to N in the form of an error function results in:

$$\varepsilon_{Elliott} = W_3 \left| \sum_{n=2}^N \left( \cos \beta d_{n-1} + j \frac{Y_{n-1}}{G_0} \sin \beta d_{n-1} - \frac{V_n^s}{V_{n-1}^s} \cdot \frac{f_{n-1} \sin(k\ell_n)}{f_n \sin(k\ell_{n-1})} \cdot \frac{Z_n^A}{Z_{n-1}^A} \right) \right|^2 \quad (16)$$

### 3.3. Pattern Synthesis

The array factor for the linear array (including the element factor due to slot) in the  $y$ - $z$  plane ( $\varphi = \pi/2$ ) is:

$$F(\theta) = \sum_{n=1}^N \left| \frac{V_n^s}{V_1^s} \right| g_n(\theta) e^{j(z_n k \cos \theta - z_n \beta + n\pi)} \quad (17)$$

The element factor of each slot is derived by assuming an equivalent dipole of length  $l$ :

$$g(\theta) = \frac{\cos(kl \cos \theta) - \cos(kl)}{\sin \theta} \quad (18)$$

As a typical approach, we will define the desired pattern by specifying the desired side lobe levels. This is done by setting an upper and lower limit for the side lobes at specific angles, so that the pattern stays within these limits. Consequently, the error function for the pattern synthesis is:

$$\varepsilon_{Synthesis} = \sum_{k=1}^K W_k \left( \left| h_k^U - F(\theta_k) \right|^2 + \left| h_k^L - F(\theta_k) \right|^2 \right) \quad (19)$$

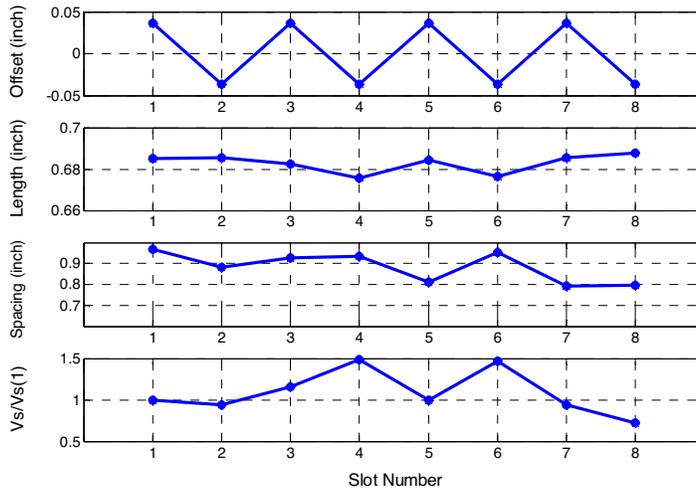
where  $F(\theta)$  is given in Eq. (17),  $h_k^U$  and  $h_k^L$  are the upper and lower limits of SLL of the desired pattern, respectively, and  $k$  denotes a point (among  $K$  discrete points  $k = 1, 2, \dots, K$ ) for the pattern amplitude of various zenith angles  $\theta_k$  between 0 and 180°.

The final error function is:

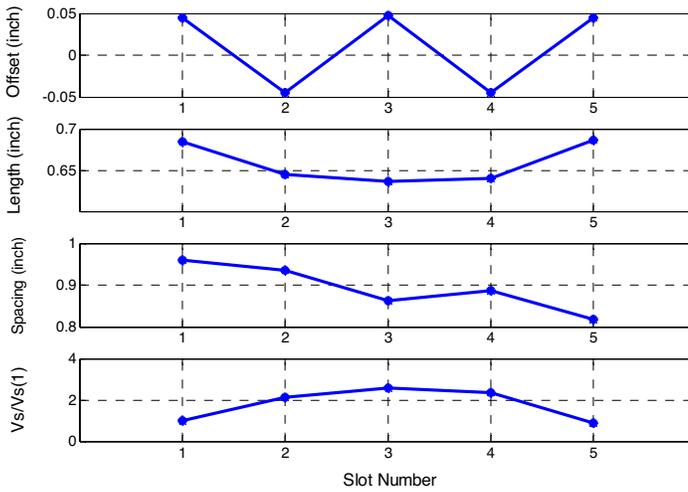
$$\varepsilon_{Total} = \varepsilon_{Matching} + \varepsilon_{Elliott} + \varepsilon_{Synthesis} \quad (20)$$

One can now design a linear array by first specifying the number of slots (N) and the desired pattern characteristics (such as beam width

and SLL) and then minimizing the error function (20) under the slot geometry constraints. As a result, the values of slot lengths ( $2l_n$ ), offsets ( $x_n$ ), spacings ( $d_n$ ) and the corresponding excitation voltages ( $V_n^s$ ) are determined, as the optimization parameters.

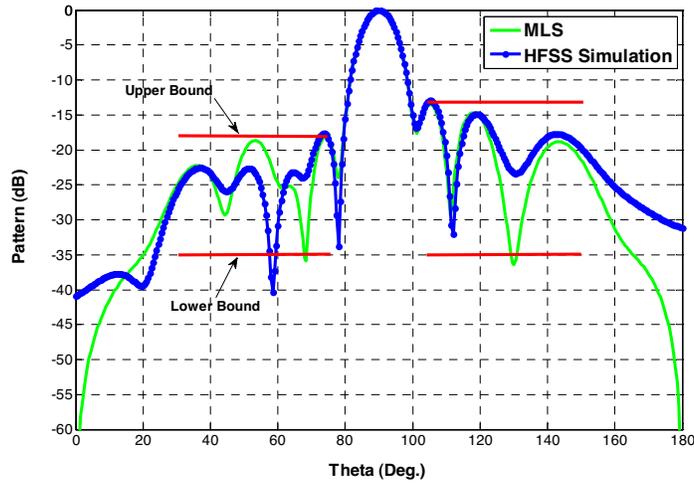


(a)

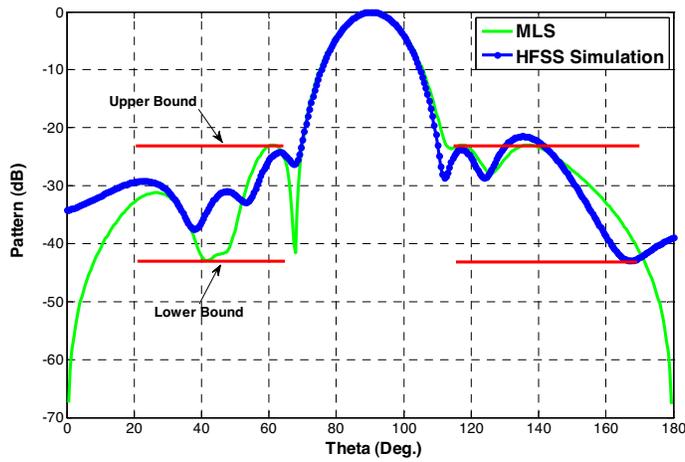


(b)

**Figure 3.** MLS Results for slots offset, length, spacing and excitation, (a) 8 slots array, (b) 5 slots array.



(a)



(b)

**Figure 4.** (a) 8 slots array with asymmetrical pattern, (b) 5 slots array with symmetrical pattern.

For the results coming up, the minimization of the error function has been done by the hybrid method of Genetic Algorithm (GA) and Conjugate Gradient (CG). Utilization of the GA & CG in a hybrid form, results in a more accurate answer at a faster rate.

#### 4. RESULTS

The design procedure described in this paper is applied to two examples. The first one is an array of 8 slots, on the broad wall of a standard WR90 waveguide so as to have a broadside asymmetrical pattern, with the upper limit of  $-18$  dB for the side-lobes on the left of the main beam and  $-13$  dB for the right ones. The lower limit is set to  $-35$  dB. The design frequency is 9.375 GHz. The wall thickness and slot width are assumed to be 0.001 inches and 0.03 inches, respectively.

The second example is an array of 5 slots, on the broad wall of the same waveguide so as to have a broadside symmetrical pattern, with the SLL upper limit of  $-23$  dB and lower limit of  $-43$  dB.

The MLS design results including slot offsets, lengths, spacings and excitation voltages are shown in Fig. 3. It can be seen from Fig. 3 that the optimization result values are asymmetrical for the asymmetrical pattern of example 1 and symmetrical for the symmetrical pattern of example 2, as it is expected from the array synthesis theory. The patterns obtained by eq. (17), using the results of Fig. 3, is compared with those obtained from simulating the same results in HFSS software, in Fig. 4.

As it can be seen from the results, MLS design pattern matches very well with the HFSS simulation pattern for the two examples. The main beams are completely broad sided and the side lobes lie within the specified limits, as desired. The HFSS simulation input VSWR results are 1.03 and 1.06, at the specified frequency, for examples 1 and 2 respectively and show a very good input match.

#### 5. CONCLUSIONS

An effective MLS method is presented for the design of nonuniformly spaced longitudinal slot arrays on the broad wall of rectangular waveguides. The theory developed by Elliott for the travelling-wave-fed slot arrays is extended to nonuniform arrays. An error function is then constructed accordingly for the impedance matching at the input and array pattern synthesis and then minimized using the hybrid method of Genetic Algorithm & Conjugate Gradient. This design method is advantageous by the fact that it combines the determination of slot parameters and impedance matching with the array pattern synthesis (including the element factor and the mutual coupling) in the form of a computer automated procedure so as to increase the design speed and accuracy. Two examples of symmetrical and asymmetrical patterns were presented, showing very good agreement between the MLS results and HFSS simulations. The procedure can also be extended to the

design of other common slot array configurations such as transverse or centre inclined slots on the broad wall.

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