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LDMOS MODELING AND HIGH EFFICIENCY POWER AMPLIFIER DESIGN USING PSO ALGORITHM

Mohammad Jahanbakht* **and Mohammad T. Aghmyoni**

Department of Electronic Engineering, Shahr-e-Qods Branch, Islamic Azad University, Tehran, Iran

Abstract—A simple and nonlinear LDMOS transistor model with multi-bias consideration has been proposed. Elements of the model are optimizes using particle swarm optimization (PSO) algorithm to fit the measured RF specifications of a typical transistor. The developed model is used then to design a high efficiency power amplifier with 55% power added efficiency (PAE) at 33 dBm output power with 12 dB power gain. This amplifier has a novel topology with optimized BALUN and microstrip matching network which makes it unconditionally stable and extensively linear over UHF frequency range of 100 MHz to 1 GHz with 163% fractional bandwidth. This power amplifier is fabricated and realized with 12-V supply voltage. A good agreement between simulated and measured values observed, indicating high accuracy of either the model and the amplifier design approach.

1. INTRODUCTION

Laterally diffused MOSFET (LDMOS) transistors are widely used as high power transistor in many recent wireless infrastructures and applications such as base stations, radio navigation, and broadcasting [1] and that is all because of their high output power with a corresponding drain to source breakdown voltage, compared to other devices such as GaAs. Gathering these behaviors together, makes these devices large compared to their operating wavelength, even at the lower frequencies. Modeling of these distributed devices therefore is a real challenge. A good and precise LDMOS model has to consider the followings:

A. Distributed architecture of the transistor.

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* Corresponding author: Mohammad Jahanbakht (mjahanbakht@yahoo.com).

B. Multi bias points of the circuit.

C. Nonlinear RF performance over the frequency bandwidth.

This accurate LDMOS model may use then to design a linear and high efficient amplifier. LDMOS devices always suffer from relatively poor efficiency due to their high power consumption. This disadvantage could be overcame using some compensating techniques like,

A. Automatic and adaptive biasing [2].

B. Tuned or optimized matching networks [3], [This Work].

C. Hybrid classes like AB or Doherty [4, 5].

D. Switch-mode amplification (envelope tracking) [6].

E. Multi-staging of the ordinary classes [1].

F. Parallel amplifiers (digitally controlled) [7].

All of these methods somehow compensate the large input capacitance and the knee effect of the transistors; and between them, the 1st and the 6th methods can be realized automatically using controller units.

In the following sections a new distributed and nonlinear LDMOS transistor model with multi-bias consideration will be introduced. A power amplifier with novel topology will also been proposed based on the earlier model. Both transistor model and power amplifier will optimize to achieve a design with high efficiency, broad bandwidth, and linear performance. Details of the optimization algorithm will be described as well.

2. NONLINEAR LDMOS TRANSISTOR MODELING

Available transistor models are normally introduced for class-A operations and their accuracy in modern high efficient circuits are

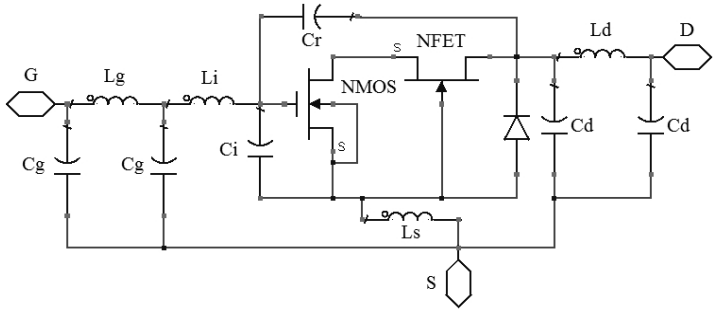

Figure 1. Proposed RF LDMOS transistor model.

compromised [8]. Hereby, a new and simple LDMOS transistor model is proposed in Figure 1.

NMOS and NFET are standard channel-N MOSFET and JFET blocks with threshold voltages of 3 V and −5.45 V respectively. Lg and Ls are gate and source bond wire inductances, respectively. Cg and Cd are gate-source and drain-source capacitances and Cr is the gate-drain feedback capacitance.

Li is the major inductance through the signal path which prepares the input RF and DC signals. This inductance has been connected to ground via the Ci and Ls. Ld is placed to pass the output RF signal and also to deliver the required drain DC biasing. A diode has also been placed to limit the V_{DS} (drain bias voltage) to positive values.

3. PARAMETER EXTRACTION USING PSO

PSO is a population based search algorithm which ensures non trapping on any local minima. Unlike genetic algorithm and other heuristic algorithms, PSO has the flexibility to control the balance between the global and local exploration of the search space. This unique feature of PSO overcomes the premature convergence problem and enhances the search capability [9]. This optimization algorithm is used here to find the appropriate values of the LDMOS transistor model.

3.1. Term Assigning

Before we proceed with the algorithm declaration, some term explanations has to be done:

A. *circuit elements (x)*: the circuit elements are Cg, Lg, Ci, Li, and ... which are considered as optimization variables and directly involve in the optimization process.

B. *particle*: a combination set of circuit elements with specific numerical values are known as one single particle (agent). Any two different particles consist of exactly the same circuit elements with different element values.
- *particle position* (p_i): this term is assigned to circuit element values in the particle.

$$p_i = \{x_i\} = \{Cg_i, Lg_i, Ci_i, Li_i, \text{ and } \ldots\} \tag{1}$$

- *particle movement vector* (r_i): this vector presents the particle position in the next step, relative to its current position. So, the particle position at the very next step would be:

$$p_i^{t+1} = p_i^t + r_i^{t+1} \tag{2}$$

C. *swarm*: the total number of particles used to optimize a problem is a constant number (n_p). The collection of all these particles is called swarm.

$$swarm = \{p_i | \, i = 1, 2, \ldots, n_p\} \tag{3}$$

D. *solution*: in every step of optimization, we will have p_i^t and r_i^t for every particle in the swarm. These two datasets together are called a solution. Solution changes dynamically as the optimization process goes on.
- *solution space*: circuit element values (particle position) in every solution could change between two min and max limits.

$$x_i \in [x_{\min}, \; x_{\max}]$$

This authorized search area is called solution space.

E. *simulated S-parameters* (S_i): using the latest solution for every particle, one may calculate the S-parameters of Figure 1 as a function of frequency. In this paper, S-parameters are calculated from the Z-matrix transformation.

F. *objective function (f)*: this function defines a criteria to evaluate particles. $f(p_i)$ is a real positive number which indicates how much a particular particle (p_i) is close to the one we are looking for. This function is also suitable to compare two or more particles together.

$$f(p_i) = \sum_{all\ frequencies} |S_i - S_{measured}|^2, \quad 0 \leq f(p_i) < \infty \tag{4}$$

G. *personal best* ($pBest_i$) *and social best (sBest)*: as the optimization process goes on, the particle position changes according to its movement vector in Equation (2). Therefore, $f(p_i^{t+1})$ is different from $f(p_i^t)$ and $pBest_i$ is the best personal experience of a single particle for its own records (its best solution), so far. On the other hand, $sBest$ is the best p_i between all particles throughout the entire optimization steps (the best value of any particle).

3.2. Algorithm

The model in Figure 1 is optimized using PSO algorithm to meet the RF specifications of a special LDMOS product of the SEMELAB® Company, named D2219UK. The optimized values are shown in Table 1.

These values are calculated by a simple repetitive procedure. The algorithm steps are as follows:

Table 1. Optimized LDMOS transistor values for D2219UK.

Parameter	Lg	Ld	Ls	Li	Cg	Cd	Ci	Cr
Value $[10^{-12}]$	70	160	400	1000	0.37	0.8	9.7	0.25

A. Initialize the total number of particles (n_p), the weight constants (C_0, C_1, and C_2), and the stop criteria (ε)

$$n_{\mathrm{p}} = 50, \quad \varepsilon = 1 \times 10^{-4}, \quad C_0 = 1, \quad C_1 = 3, \quad \text{and } C_2 = 1$$

It worth to mention that,

$$C_1 + C_2 = 4 \quad \text{and} \quad 0 \leq C_0 \leq 1.2$$

B. Initialize the particle positions (circuit element values) in every 50 particles (p_i) as they uniformly distribute over the solution space. The particle movement vectors (r_i) are set to zero at first.

C. Apply the objective function to all of the particles to extract initial $pBest_i$ and $sBest$.

D. Calculate the movement vector (r_i) for every particle,

$$r_i^{t+1} = C_0 * r_i^t + rand * C_1 * (pBest_i - p_i) + rand * C_2 * (gBest - p_i) \quad (5)$$

rand is a random variable between 0 and 1 which regenerates every time. This movement vector has 3 sentences. The first sentence is called inertia which makes the particle move in the same old direction with the same old movement vector. The second sentence is called conservative personal influence which makes the particle return to the previously self-discovered best position. The last sentence is called social influence which makes the particle follow the best neighbors direction. C_0 is weight of inertia, C_1 is weight of personal information, and C_2 is weight of social information. Therefore, for initial steps of the search process, large personal weight to enhance the global exploration is used. While for the last steps, the social weight increases for better local exploration.

E. Larger r_i^{t+1} means instability. So the movement vector in step D has to be limited to $r_{\max}$

$$r_i^{t+1} \leq r_{\max} = k \frac{x_{\max} - x_{\min}}{2}, \quad 0.1 \leq k \leq 1 \quad (6)$$

F. Update $pBest_{\mathrm{i}}$ and $sBest$ values by applying the objective function.

G. As long as the $sBest$ shrinks to zero, C_2 must grow toward 3 and consequently C_1 should decrease to 1.

H. While $f(sBest) > \varepsilon$, go to step D.

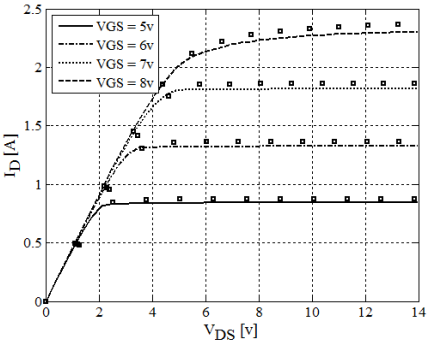

Figure 2. Measured (squares) and simulated (lines) I-V curves of the optimized model.

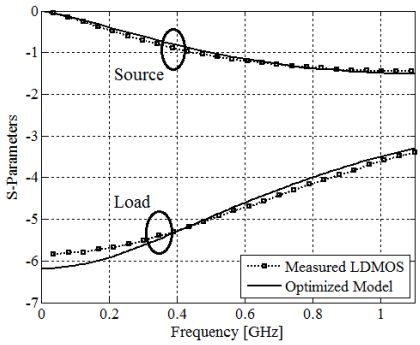

Figure 3. Measured and simulated source (S_{11}) and load (S_{22}) scattering-parameters of the optimized D2219UK LDMOS transistor under certain bias conditions.

3.3. Model Verification

To check the performance of the PSO algorithm in modeling of the transistor (in Table 1), two approaches are taken simultaneously. At first, the I-V curve of the LDMOS transistor model has been compared with measurement in Figure 2. This comparison is made under four different gate-source voltages. The model is shown to have a reasonable performance for either linear or large-signal input.

At the second approach, simulated scattering-parameters of an individually biased D2219UK transistor is compared with measurement in Figure 3. Drain and gate are biased on 12 V and 3.55 V respectively. This figure clearly proofs the accuracy of the model and allows the authors to proceed with the amplifier design approach using the extracted model.

4. HIGH EFFICIENCY POWER AMPLIFIER DESIGN

4.1. Topology and Stability

One of the major problems in the design of power amplifiers at lower frequencies is the lack of high-Q inductors needed for the matching networks [10]. By using the precise LDMOS model in Figure 1, a power amplifier with novel topology has been proposed in Figure 4(a) which uses merged microstrip and BALUN matching networks. This circuit has the overall size of 3×4 cm.

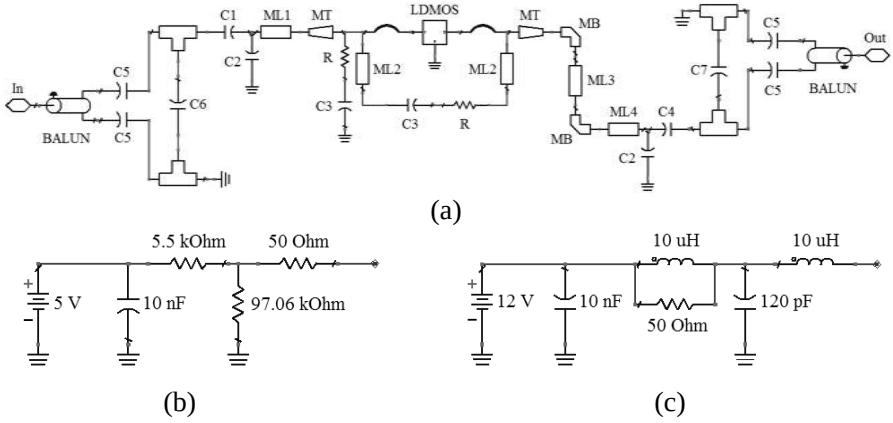

Figure 4. (a) Topology of the proposed amplifier, and its (b) gate, and (c) drain bias network.

Table 2. Optimized power amplifier elements for the maximum linear PAE.

Parameter	C_1 [pF]	C_2 [pF]	C_3 [nF]	C_4 [pF]	C_5 [nF]	C_6 [pF]	C_7 [pF]	R [Ω]	ML_1 Width/Length [mm]	ML_2	ML_3	ML_4
Value	71	5.5	100	45.5	10	15	33	255	3/19	2/9	3/6.5	3/3.5

Table 3. Input and output BALUN specifications.

Parameter	Z_0 [Ω]	$\in_{r_{eff}}$	μ_r (Surrounding Sleeve)	Input BALUN Line Length [mm]	Input BALUN L (per Unit Length) [nH]	Output BALUN Line Length [mm]	Output BALUN L (per Unit Length) [nH]
Value	25	2	125	50	200	100	300

The required gate and drain DC bias network for LDMOS power amplifier are experimentally presented in Figures 4(b) and 4(c) respectively. These high impedance biasing networks are connected through RF chock to obstruct high frequency signal pass.

This amplifier is mounted on RO4003 Rogers^{TM} substrate with $\varepsilon_r = 3.38$ and $h = 60$ mil. Circuit elements and microstrip transmission line dimensions are optimized using Agilent ADS® to gain as much efficiency as possible throughout the desired UHF frequency range with maximum achievable linearity. Optimum values of either circuit elements and matching BALUNs are presented in Tables 2 and 3.

Stability of the circuit in Figure 4(a) is guaranteed by grounded R and C_3 in input at lower frequencies and also by serial R and C_3 in feedback route at higher frequencies. On the other hand, optimized microstrip network and input/output BALUNs are used here to create a perfect match. Stability factors of the designed amplifier are plotted in Figure 5. The K factor is more than 1 and $|\Delta|$ is less than 1 through the entire frequency range, which means unconditional stability. The best performance is obtained at 800 MHz.

4.2. Power Spectrum and Amplification

Power spectrum of the proposed amplifier is shown in Figure 6. Based on this figure, the operational frequency range of the amplifier is from 100 MHz to 1 GHz which covers the entire UHF with 163% fractional bandwidth.

According to Figure 6, ripples in the power spectrum are less than 1 dBm at the entire frequency range which verifies linear performance of design. The simulation in this figure is compared with measurement which not only validates the power amplifier design approach, but also the behavior of LDMOS model in previous section.

4.3. Power Added Efficiency

Efficiency is defined as the ratio of output RF power to its relevant input DC power. This means, how much of the power source is usefully applied to the amplifier's output [11]. The optimized PAE is plotted in Figure 7. As can be seen in this figure, the efficiency is more than 55%

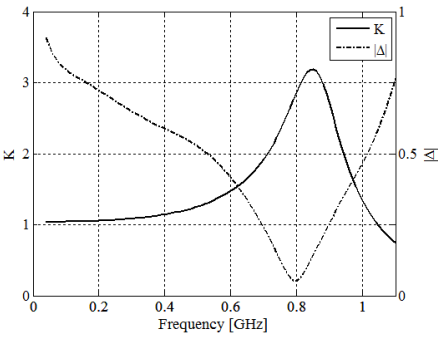

Figure 5. Stability factors of the optimized power amplifier.

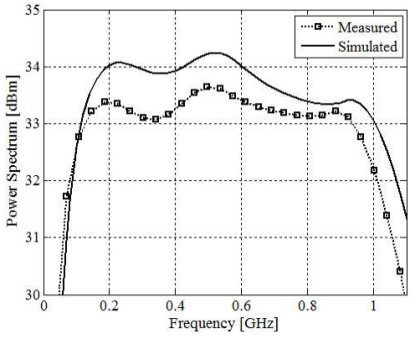

Figure 6. Power spectrum of the optimized linear power amplifier.

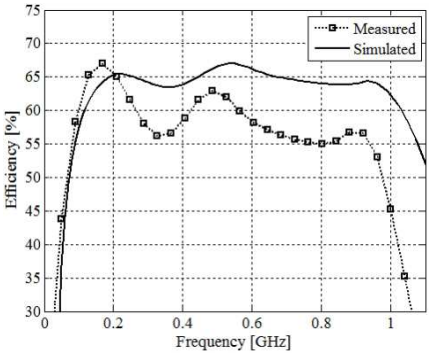

Figure 7. Measured and simulated PAE of the power amplifier.

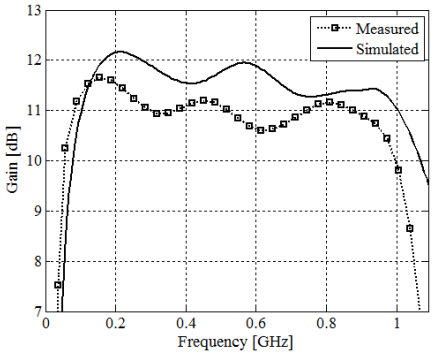

Figure 8. Measured and simulated power gain of the amplifier.

Table 4. Performance comparison of high efficient UHF amplifiers.

Ref. No.	Active Device	Technique	PAE (%)	P_{out} [dBm]	Max Frequency [MHz]
[1]	LDMOS	Multi Staging	49	23	900
[4]	LDMOS	Hybrid Classes	80	10	1000
[5]	GaAs	Hybrid Classes	50	24	800
[7]	CMOS	Parallel Amplification	43	24	1000
This Work	LDMOS	Optimized Matching Network	55	33	1000

at the entire operating frequency range. The simulation is compared with the measurement which shows a good agreement between them.

Operating gain of the amplifier is plotted in Figure 8. Measured and simulated curves are compared together which indicate a good agreement between them. Thereby a 11–12 dB power gain is achieved. Proposed power amplifier properties and specifications are compared with other UHF articles in Table 4.

5. CONCLUSION

A new methodology is developed for high power RF LDMOS transistor modeling over broad frequency range. In this method, the PSO

algorithm is used to optimize the elements of the nonlinear model. The proposed model is suitable for diverse transistor simulation approaches with any desired DC biasing.

The developed model is used then to design a power amplifier with combined microstrip and BALUN matching network. This novel UHF amplifier topology is optimized once again to achieve the broadest possible linear respond with high efficiency performance. Thereby an amplifier with 55% PAE at 33 dBm output power with minimum possible response ripples and 12 dB power gain is obtained. This amplifier is shown to be unconditionally stable over 100 MHz to 1 GHz with 163% fractional bandwidth. The measured plots not only validate the amplifier performance, but also the accuracy of the LDMOS transistor model.

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