CHARACTERIZATION OF COMPACT V-BAND GaAs CMRC FILTER USING SLOW WAVE CPW TRANSMIS-SION LINES TECHNOLOGY

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Abstract—This work presents a compact, high performance GaAs V-band bandpass filter (BPF) using a slow-wave coplanar waveguide transmission line (S-CPW TLine) and a CMRC (compact microstrip resonant cell). The slow-wave CPW Tlines have potential for the use in miniaturized low loss compact passive devices in the millimeter-wave frequency band. Owing to strong slow-wave effect, the longitudinal length of the S-CPW is shorter than that of a classical microstrip based on the same technology. The S-CPW TLines in the designed filter were realized with a reconfigurable defected ground structure (DGS). Adding the conventional inductively coupled resonator CMRC BPF allows the resonator to be miniaturized by the exploitation of the transversal dimensions of the CPW, while maintaining its performance as measured by insertion and return losses. However, the DGS cell allows reconfiguration of the structure from a low-band to a high-band BPF. The design of the filters with the DGS using filters that are designed for V-band applications is explained.

1. INTRODUCTION

In recent years, high data-rate wireless communication technologies that operate in millimeter wave frequency bands, such as for use in V-band wireless personal area networks (WPAN), have been in high demand for dense local communications, including wireless LANs. For example, future high-speed telecommunications and video streaming

Received 13 July 2012, Accepted 6 September 2012, Scheduled 13 September 2012

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will operate at approximately 60 GHz; automotive radars operate around 77 GHz; RF imaging uses 94 GHz, 140 GHz, and higher frequencies. Therefore, the development of high-frequency TLines for the use in passive circuits, such as those in power dividers, baluns, matching networks, phase shifters and filters, is of particular interest. In all of these passive devices, the filters must perform excellently and allow testing of the advanced technologies on which they are based and must satisfy the insertion loss and on-chip area requirements.

The slow-wave structure, which is frequently realized using alternatively loaded inductors and capacitors on a regular transmission line, is commonly used to achieve highly integrated microwave circuits. It has received much attention in the community of microwave researchers owing to its flexibility and versatility in the development of miniaturized components by many fabrication processes. Considerable interest has recently been shown in the development of highperformance microwave components using slow-wave structures, including electromagnetic bandgap (EBG) structures [1,2], and defective ground structures (DGS) [3–5], because of their interesting properties of miniature size, suppression of surface waves and arbitrary stopbands. Figure 1 shows a recently proposed one-dimensional (1D) compact microstrip resonance cell (CMRC) [6-8]. It was designed to minimize the size and slow-wave characteristics, which can be exploited to reject unwanted frequencies and reduce the dimensions of the structure. This work proposes three one-dimensional (1-D) V-band bandpass filters with a DGS structure in which various technologies are combined with CMRC filters. Both filters are centered at around the V-band and designed within the 100 µm-thick substrate to ensure compatibility with the GaAs 0.15-um process. A simulation based on a full wave electromagnetic (EM) solver is performed, and on-wafer measurements that are made in a microwave probe station are carried out [10].

Slow-wave structures can be categorized into two main groups. Many slow-wave structures, realized with a cascade of several simple unit cells are periodic structures [4–8], in which the unit cell is an infinitesimal line section with a small electrical length, which can be approximated by a lumped L-section with a per-unit-length inductance and a per-unit-length capacitance, if the losses can be ignored. This method is straightforward and intuitive, as the slow-wave structure shares the same circuit model as its uniform counterpart. However, the periodicity only allows a 1-D arrangement except for the complementary conducting strips [7, 8], restricting miniaturization. Slow-wave structures can also be developed by working directly on the equivalent-circuit model of a uniform transmission line with a designated electrical length [12]. In this approach, quasi-lumped elements can be substituted directly into the π -, T-, or L-equivalent model of the uniform line, and no periodicity is required.

This paper is organized as follows. First, in Section 2, the DGS S-CPW TLines are optimized and characterized up to 90 GHz. Their performance is compared with measurements made of microstrips based on the same GaAs technology, and benchmarking is carried out with previously published TLines. Section 3 presents the controlling mechanism of the DGS S-CPW TLines. Finally, Section 4 designs and characterizes DGS S-CPW CMRC filters.

2. INTERCONNECTION DEFECTED GROUND STRUCTURE (DGS) S-CPW TLINES

All devices presented in this paper were manufactured using $0.15 \,\mu\text{m}$ GaAs technology from WIN Semiconductor Company. The GaAs technology consists of a thin SiN layer deposited on a 100 μ m-thick GaAs bulk substrate, as shown in Fig. 1(a). The GaAs layer has a loss tangent of 0.001 and a dielectric constant of 12.9. The multilayer is formed by the following steps: first, a 1- μ m-thick layer is deposited, and then a 2- μ m-thick layer is deposited. One of the two metal layers is on the top of layer *l* and the other one between the two SiN layers. The choice of technology used in the filter design depends on the desired selectivity. Fig. 1(b) shows the S-CPW topology, which consists of a classical CPW TLine loaded by DGS. In this study, metal-1 is utilized as a filter. Fig. 1 shows the DGS S-CPW topology composed of a



Figure 1. (a) Stack of the $0.15 \,\mu\text{m}$ InGaAs technology from WIN semiconductor company. (b) Three-dimensional view of the S-CPW topology.

classical CPW TLine on which a ground patterned metallic shield (metal-1) is loaded. The gap G between the CPW and the ground patterned metallic shield strips is then adjusted to reach the targeted characteristic impedances.

Figures 1(b) and 4 show the circuit layout and equivalentcircuit model of the proposed S-CPW by DGS, respectively. For a conventional CPW, grounded microstrip TLines on GaAs typically exhibit a quality factor in V-band applications of the order of $5 \sim 15$, which is not sufficient for filter and TLine design. Since slow-wave TLine has been shown to provide much higher Q values [2], this approach is taken. Fig. 1(b) shows the structure of the slow-wave TLines utilized in this work. The slotted bottom metallic shields were patterned with 130 µm-long (L) metal stripes that were separated by slots with widths of 10 µm (SS = SL). The width of the signal line metal was 37 µm (W); the distance between the signal line metal and the metallic ground was 5 µm (G); the length of the signal line was 450 µm (L-TLine); the ground plane was 250 µm (Wg). The resistivity of every metal layer was $0.02 \Omega/square$, and the insulator layer was GaAs.

The electromagnetic (EM) simulation software ADS Momentum was utilized to optimize the DGS. The EM simulation of DGS S-CPW TLs is fairly complex, but it can be performed successfully. Figs. 2(a) and (b) compare the standard (Std.) CPW TLs and DGS S-CPW TLs. Fig. 3 presents the simulated performance of the TL, and high Q values were obtained.

Four sets of dimensions of the slotted unit with the DGS S-CPW TLines structure, as shown in Figs. 4(a)-(d), are proposed. To measure



Figure 2. (a) Structure of standard (Std.) CPW TLs. (b) DGS S-CPW TLs.



Figure 3. Simulated quality factor.



Figure 4. (a)–(d) structures of four different slots shaped unit DGS S-CPW TLines.

the S-parameter of the interconnection line, all the lines with length $450 \,\mu\text{m}$ for the four test structures are designed. Figs. 4(a) shows the standard CPW test structure, and Figs. 4(b), (c), (d) show the structures with three, five and seven defective ground slots. The test structure consists of a CPW interconnection line that lies on top of the inter-metal dielectric, as shown in Fig. 1.

To avoid the need for complex EM simulations of DGS S-CPW TLs, a simple analytic model, which accurately predicts DGS S-



Figure 5. DGS S-CPW TLines model.

CPW TLs properties, was developed. The model exploits the well established models of grounded and standard CPWs. Fig. 5 shows the Z element (L, R and C) of the slowwave TL model. A slowwave (large propagation constant) can be achieved by increasing C and L in the TL.

The lumped circuit parameters must be extracted to analyze the DGS unit. The equivalent impedance equation of the single resonant model may be expressed as

$$C_x = \frac{1}{C_1} + 4C_{sub.} \tag{1}$$

$$Z \approx \left(\frac{1}{j\omega_o C_x} + j\omega_o L_1 + R_1\right) \tag{2}$$

The resonant frequency of the parallel circuit is defined as

$$\omega_o = \frac{1}{\sqrt{C_x L_1}} \tag{3}$$

The insertion loss is given by

$$S_{21} = \frac{2Z_o}{2Z_o + Z} = \frac{2Z_o}{2Z_o + \frac{1}{1/R_1 + 1/j\omega L_1 + j\omega C_x}}$$
(4)

The 3 dB cut-off angular frequency, ω_c , can be determined by

$$S_{21} = \frac{2Z_o}{2Z_o^2 + \left(\frac{\omega_c/C_x}{\omega^2 - \omega_c^2}\right)} = \frac{1}{\sqrt{2}}$$
(5)

(2) into (4), the capacitance is obtained as

$$C_x = \frac{\omega_c}{2Z_o(\omega_o^2 - \omega_c^2)} \tag{6}$$

Parameters	Parameters value			
Slot, $SL = SS$ (µm)	10			
Signal width, W (µm)	37			
Metallic ground, G (µm)	5			
Patterned length, L (µm)	130			
Resonant frequency, ω_o (GHz)	60			
Inductance, L (nH)	0.006			
Capacitance, C (pF)	1.24			
Resistance, R_1 ($k\Omega$)	1.09			

Table 1. Parameters extracted from equivalent circuit.

$$C_1 = \frac{2Z_o \left(\omega_o^2 - \omega_c^2\right)}{\omega_c - 4C_{sub} \cdot \left[2Z_o \left(\omega_o^2 - \omega_c^2\right)\right]} \tag{7}$$

The inductance can be determined by

$$L_1 = \frac{1}{\omega_o^2 C_x} = \frac{1}{4\pi^2 f_o^2 C_x}$$
(8)

Therefore, the resistance R of the circuit can be obtained form resonant frequency ω respectively

$$S_{21}|_{\omega=\omega_o} = \left|\frac{2Z_o}{2Z_o + 2Z_s}\right| = \frac{2Z_o}{2Z_o + R_1}$$
(9)

$$R = 2Z_o \frac{1 - S_{21}|_{\omega = \omega_o}}{S_{21}|_{\omega = \omega_o}}$$
(10)

This model can predict the slow-wave TLs with slotted ground shield over a relatively wider frequency range from DC to 90 GHz, as shown in Fig. 1(a). The results of the circuit simulation agree closely with those of the EM simulation, as shown in Fig. 6. Table 1 presents the resistances, capacitances and inductances that are determined from the resonant frequencies of the slow-wave TLs with the slotted ground shield.

3. DEFECTIVE GROUND STRUCTURE (DGS) S-CPW TLINES MEASUREMENT RESULTS

The DGS S-CPW TLines were measured up to 110 GHz with targeted characteristic impedances from 35 to 66Ω . For comparison, measurements of a classical CPW TLine are realized. Table 2 presents the geometrical dimensions and the electrical properties at 60 GHz. The characteristic impedance Z_o , effective relative permittivity ε_{reff} ,





Figure 6. EM simulated data and circuit simulation data.

Figure 7. Measured characteristic impedances for DGS S-CPW and Std. CPW TLines.

Table 2. Physical characteristics and 60-GHz electrical properties for DGS S-CPW.

	S-CPW parameters						Electrical					
Parameters							performance					
							at ou GHz					
	W	G	Slots	SS	SL	L.	Wa	TLine	z			α
			51005				W g	length	Ľ.	Q	ε_{eff}	(dB/
	(μm)	(μm)	by	$ (\mu m)$	$ (\mu m)$	$ (\mu m) $	$ (\mu m) $	($ (\Omega) $	–	-55	· · · · ·
								(μm)				[mm)
Std. CPW	37	5					250	450	28	27	15	0.51
TLine	51	5	-	-	-	-	200	450	20	21	4.0	0.01
DGS S-CPW1	37	5	3	10	10	130	250	450	43	33	6.2	0.39
DGS S-CPW2	37	5	5	10	10	130	250	450	51	36	6.8	0.41
DGS S-CPW3	37	5	7	10	10	130	250	450	55	38	7.3	0.43

and attenuation constant α were extracted with the method proposed by [9]. The quality factor Q was then computed using

$$Q = \frac{\beta}{2\alpha} \tag{11}$$

where α and β are the attenuation and phase constant per unit length, respectively.

Finally, the slow-wave factor was calculated according to

slow-wave factor =
$$\lambda_0 / \lambda_g = \beta / \kappa_0 = \beta c / \omega = \sqrt{\frac{\varepsilon_{reff.(S-CPW)}}{\varepsilon_{reff.(CPW)}}}$$
 (12)

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Accordingly, this parameter represents the reduction in physical length achieved by using a DGS S-CPW TLine from the length of a classical CPW TLine with the same electrical length. Fig. 7 shows the measured characteristic impedances. From Fig. 8, the DGS S-CPWs structures successfully enhanced the effective dielectric constant ε_{eff} thus reduced the corresponding frequency of the quarterwavelength from 70 GHz to 68, 62 and 57 GHz. The DGS S-CPW TLines are electrically much longer than the Std. CPW TLine because they exhibit a strong slow-wave effect, as determined by the effective relative permittivity values shown in Fig. 9. The high effective relative permittivity values of the S-CPW (between 6.2 and 7.3) in Fig. 10 yields slow-wave factors of 1.1 to 1.26 compared with CPW TLines. By the transmission line theory [17], the propagation constant of a line without loss is $\beta = \omega_0 \sqrt{LC}$, where ω_0 is the angular frequency, and C and L are the distributed shunt capacitance and series inductance per unit length, respectively. The high relative effective permittivity of the S-CPW transmission line was responsible for a strong slowwave effect and large size reduction. A lower dielectric thickness Hcorrespondeds to a higher equivalent capacitance and slow-wave factor. Fig. 11 plots the measured attenuation constant of the DGS S-CPW and Std. CPW TLine. The DGS S-CPW1, DGS S-CPW2, DGS S-CPW3 and Std. CPW TLines can be properly compared because they exhibit the same characteristic impedance. Therefore, the measured attenuation constants are of the same order of magnitude for both topologies, at approximately 0.5 dB/mm at 60 GHz. As the attenuation



7.4 7.2 7.0 Relative effective permittivity 6.8 6.6 6.4 6.2 6.0 5.8 5.6 Std CPW S-CPW1 5.4 5.2 5.0 S-CPW2 4.8 4.6 30 40 50 60 70 Frequency (GHz)

Figure 8. Measurement phase results of DGS S-CPW and Std. CPW TLines.

Figure 9. Measurement results of the effective relative permittivities for four DGS S-CPWs and a Srd. TLine.



Figure 10. Measurement results of the slow-wave factor for four DGS S-CPWs and a Std. TLine.



Figure 11. Measured attenuation constant for DGS S-CPW and microstrip TLines.





Figure 12. Measurement results of the quality factors for four DGS S-CPWs and Std. CPW TLines.

Figure 13. Measurement results of the stop band for four DGS-S-CPWs and Std. CPW TLine.

constants of TLines with the same characteristic impedance are similar, the quality factor for DGS S-CPWs is higher, as shown in Fig. 12. An equivalent lumped circuit is introduced and utilized to model the DGS cell. The transmission zeroes for stop band rejection are then designed and determined by cascading the DGS cells. Sharp selectivity and deep attenuation levels are obtained on the stop band for the transmission zero, shown in Fig. 13. The chip photographs of 450 μ m-long CPW in Fig. 14 show DGS S-CPW1 DGS, S-CPW2, DGS S-CPW3 and Std. CPW TLines.



Figure 14. The chip photographs of $450 \,\mu$ m-length CPW include of S-CPW1, S-CPW2, S-CPW3 and Std. CPW TLines.

4. DESIGN OF S-CPW CMRC FILTERS

To further demonstrate the size reduction that can be realized using the proposed S-CPW structure, three V-band CMRC filters with and without the proposed slow-wave structure were designed and According to transmission line theory, for the CMRC, fabricated. the propagation constant of a line without loss is $\beta = \omega_0 \sqrt{LC}$ where ω_0 is the angular frequency, and C and L are the distributed shunt capacitance and series inductance per unit length, respectively. Slowwaves (large propagation constant) can be achieved by increasing Cand L in the transmission line. If the values of C and L are increased not continuously but periodically, then the transmission line may form a CMRC structure, an L-C equivalent circuit, as shown in Fig. 15, in which the inductances L_0 and L_1 correspond to the transverse and longitudinal narrow strips, respectively. The capacitance is C_0 capacitance of the triangular patch C_1 , which is the gap capacitance between the triangular patch and the microstrip line [10].



Figure 15. L-C equivalent circuit for CMRC.



Figure 16. L-C equivalent circuit for S-CPW CMRC BPF.

Figure 16 shows the filter layout and equivalent-circuit model of the proposed S-CPW. For brevity, an S-CPW with a CMRC unit cell, consisting of three cascaded quasi-lumped elements, is considered. Increasing the line capacitance and inductance in a slowwave transmission line can further reduce the size of the circuit. By adjusting the increments in the inductance and capacitance in the structure, resonance can be induced to improve performance. Therefore, three CMRC BPFs with and without the S-CPW TLine structure are presented. The filter cell is primarily a section of CPW-TLine from which some metallic parts have been removed. Increasing the width (W_2) of narrow connecting lines increases the series inductance. In contrast, increasing the gaps (G_t) between the lines increases the shunt capacitance. The length of the CPW-TLine section (L) and the gap width (SS, SL) in the etched pattern can be varied to generate different slow-wave effects at different frequencies. Comparisons of the structures in Figs. 17(a), 17(b) and 17(c) clearly show that the three ground structures exhibit slow-wave effects, which increase not only the series inductance and shunt capacitance, but also the resonant point of the shunt resonant components.

With a fixed width of DGS in the ground gaps and the CPW TLine of the perforation, a more effective slow-wave CMRC BPF is shown in Fig. 17(a), half of the DGS structure, which acts as a slow-wave CMRC BPF, shown in Fig. 17(b), and a standard CPW CMRC BPF without the DGS structure shown in Fig. 17(c). In these three cases, the ground plane is a layer of the metal (M1). For measurement purposes, the probe pad placed on the top layer of metal can be configured with a



Figure 17. Structure of three different circuits for S-CPW CMRC BPF.

Ground-Signal-Ground (G, S, G) probe and connected to the ground plane using via holes. The slow-wave has mmW applications in MMIC technology and can be used to fabricate the DGS TLins structure with CMRC and gaps of the order of micrometers.

The S-CPW CMRC filter circuit parameters in Figs. 17(a), (b) and (c) are $W_f = 133 \,\mu\text{m}$, $W_l = 105 \,\mu\text{m}$, $W_p = 50 \,\mu\text{m}$, $W_d = 56 \,\mu\text{m}$, $W_g = 36 \,\mu\text{m}$, $W_1 = 37 \,\mu\text{m}$, $W_2 = 28 \,\mu\text{m}$, $L_p = 93 \,\mu\text{m}$, $L_1 = 130 \,\mu\text{m}$, $L_2 = 655 \,\mu\text{m}$, $L_3 = 330 \,\mu\text{m}$, $L_4 = 152 \,\mu\text{m}$, $L_5 = 143 \,\mu\text{m}$, $SS = 10 \,\mu\text{m}$, $SL = 10 \,\mu\text{m}$ and $G_t = 5 \,\mu\text{m}$. The width and DGS gaps of the cells are identical to those of a $50 \,\Omega$ S-CPW TLine on the same substrate. Fig. 18(a) plots the measured frequency response S_{21} of the different S-CPWs, and Fig. 18(b) plots S_{11} .

The measured minimum transmission loss of the filter in Fig. 18(a)

Table 3. Performance of designed filters and gives a comparison with other recently reported mm-wave filter designs.

			-		,	,	
Process	Size	Frequency	Bandwidth	Return	Insertion	Stopband	
11000000	0120	of 3 dB		Loss	Loss	rejection	
Si-BCB	$7.5\mathrm{mm}$	63 GHz	4%	-18dB	_13dB	NA	
SI DOD	$\times 3.4\mathrm{mm}$	00 0112	170	IGUD	1.0 UD	11.11.	
CMOS	$0.72\mathrm{mm}$	62 GHz	14%	-10 dB	-5.9 dB	$72\mathrm{GHz}@$	
CINOD	$\times 0.48\mathrm{mm}$	02 0112	11/0	IUUD	0.0 UD	$-28\mathrm{dB}$	
LTCC	$4.8\mathrm{mm}$	50 CHz	1%	_30 dB	_1 2 dB	NA	
L100	$\times 2\mathrm{mm}$	55 GHZ	470	-30 (1D	-1.2 uD	IN.A.	
AlaOa	$1\mathrm{mm}$	60 CHz	8 3%	$-17 \mathrm{dB}$	264B	ΝΔ	
A12O3	$\times 1\mathrm{mm}$	00 0112	0.070	-17 0D	-2.0 uD	IN.A.	
GaAs	$0.4\mathrm{mm}$	60 CHz	NΔ	≤ -10	$-3.5\mathrm{dB}$	$68\mathrm{GHz}@$	
pHEMT	$\times 0.66\mathrm{mm}$	00 0112	N.A.	$^{\rm dB}$		$-42.1\mathrm{dB}$	
Cala	0.54 mm			< 15		$64.1\mathrm{GHz}$	
DUEMT	0.54 mm	$55.2\mathrm{GHz}$	7.8%	≤ -10	$-2.7\mathrm{dB}$	0	
piitzwit				uD		$-37.8\mathrm{dB}$	
						641 CIL	
GaAs	$0.54\mathrm{mm}$	59.4 CH2	14.9%	≤ -13	21 dB	04.1 GHZ	
pHEMT	$\times 0.17\mathrm{mm}$	52.4 GHZ	14.270	$^{\mathrm{dB}}$	-5.1 uD	971 dD	
						-37.1 0D	
						CC OCIL	
GaAs	$0.54\mathrm{mm}$	50 1 CH2	1107	≤ -15	9.4P	00.8 GHZ	
pHEMT	$\times 0.17 \mathrm{mm}$	JU.1 GHZ	11/0	dB	-2 ub	42.0 JD	
						-43.2 UD	
	Process Si-BCB CMOS LTCC Al ₂ O ₃ GaAs pHEMT GaAs pHEMT GaAs pHEMT	$\begin{array}{c} \mbox{Process} & \mbox{Size} \\ \mbox{Si-BCB} & 7.5 \ mm \\ \times 3.4 \ mm \\ \mbox{Omega} & 0.72 \ mm \\ \times 0.48 \ mm \\ \times 0.48 \ mm \\ \times 0.48 \ mm \\ \times 2 \ mm \\ \mbox{Mmm} \\ \mbox{Alg} & \mbox{Mmm} \\ \mbox{Alg} & \mbox{Mmm} \\ \mbox{Alg} & \mbox{Mmm} \\ \mbox{Alg} & \mbox{Mmm} \\ \mbox{GaAs} & \mbox{O.4 \ mm} \\ \mbox{GaAs} & \mbox{O.54 \ mm} \\ \mbox{PHEMT} & \mbox{Mmm} \\ \mbox{GaAs} & \mbox{O.54 \ mm} \\ \mbox{PHEMT} \\ \mbox{GaAs} & \mbox{O.54 \ mm} \\ \mbox{Mmm} $	ProcessSizeFrequencySi-BCB $7.5 \text{ mm} \\ \times 3.4 \text{ mm}$ 63 GHz CMOS $0.72 \text{ mm} \\ \times 0.48 \text{ mm}$ 62 GHz LTCC $4.8 \text{ mm} \\ \times 2 \text{ mm}$ 59 GHz Al_2O3 $1 \text{ mm} \\ \times 1 \text{ mm}$ 60 GHz GaAs $0.4 \text{ mm} \\ \times 0.66 \text{ mm}$ 60 GHz GaAs $0.54 \text{ mm} \\ \times 0.17 \text{ mm}$ 52.2 GHz GaAs $0.54 \text{ mm} \\ \times 0.17 \text{ mm}$ 52.4 GHz GaAs $0.54 \text{ mm} \\ \times 0.17 \text{ mm}$ 50.1 GHz	ProcessSizeFrequencyBandwidth of 3 dBSi-BCB 7.5 mm $\times 3.4 \text{ mm}$ 63 GHz 4% CMOS 0.72 mm $\times 0.48 \text{ mm}$ 62 GHz 14% LTCC 4.8 mm $\times 2 \text{ mm}$ 59 GHz 4% Al_2O_3 1 mm $\times 1 \text{ mm}$ 60 GHz 8.3% GaAs 0.4 mm $\times 1 \text{ mm}$ 60 GHz $N.A.$ GaAs 0.54 mm $\times 0.17 \text{ mm}$ 55.2 GHz 7.8% GaAs 0.54 mm $\times 0.17 \text{ mm}$ 52.4 GHz 14.2% GaAs 0.54 mm $\times 0.17 \text{ mm}$ 50.1 GHz 11%	Process Size Frequency Bandwidth of 3 dB Return Loss Si-BCB 7.5 mm $\times 3.4 \text{ mm}$ 63 GHz 4% -18 dB CMOS 0.72 mm $\times 0.48 \text{ mm}$ 62 GHz 14% -10 dB LTCC 4.8 mm $\times 2 \text{ mm}$ 59 GHz 4% -30 dB Al_2O_3 1 mm $\times 1 \text{ mm}$ 60 GHz 8.3% -17 dB GaAs 0.4 mm $\times 0.66 \text{ mm}$ 60 GHz $N.A.$ ≤ -10 dB GaAs $0.54 mm\times 0.17 \text{ mm} 55.2 \text{ GHz} 7.8\% \leq -15dB$ GaAs $0.54 mm\times 0.17 \text{ mm} 52.4 \text{ GHz} 14.2\% \leq -13dB$ GaAs $0.54 mm\times 0.17 \text{ mm} 50.1 \text{ GHz} 11\% \leq -15dB$ <td>ProcessSizeFrequencyBandwidth of 3 dBReturn LossInsertion LossSi-BCB7.5 mm $\times 3.4 \text{ mm}$63 GHz4%-18 dB-1.3 dBCMOS0.72 mm $\times 0.48 \text{ mm}$62 GHz14%-10 dB-5.9 dBLTCC4.8 mm $\times 2 \text{ mm}$59 GHz4%-30 dB-1.2 dBAl_2O_31 mm $\times 1 \text{ mm}$60 GHz8.3%-17 dB-2.6 dBGaAs pHEMT0.4 mm $\times 0.66 \text{ mm}$60 GHzN.A.≤ -10 dB-3.5 dBGaAs pHEMT0.54 mm $\times 0.17 \text{ mm}$55.2 GHz14.2%≤ -15 dB-2.7 dBGaAs pHEMT0.54 mm $\times 0.17 \text{ mm}$52.4 GHz14.2%≤ -13 dB-3.1 dBGaAs pHEMT0.54 mm $\times 0.17 \text{ mm}$50.1 GHz11%≤ -15 dB-2 dB</td>	ProcessSizeFrequencyBandwidth of 3 dBReturn LossInsertion LossSi-BCB7.5 mm $\times 3.4 \text{ mm}$ 63 GHz4%-18 dB-1.3 dBCMOS0.72 mm $\times 0.48 \text{ mm}$ 62 GHz14%-10 dB-5.9 dBLTCC4.8 mm $\times 2 \text{ mm}$ 59 GHz4%-30 dB-1.2 dBAl_2O_31 mm $\times 1 \text{ mm}$ 60 GHz8.3%-17 dB-2.6 dBGaAs pHEMT0.4 mm $\times 0.66 \text{ mm}$ 60 GHzN.A. ≤ -10 dB-3.5 dBGaAs pHEMT0.54 mm $\times 0.17 \text{ mm}$ 55.2 GHz14.2% ≤ -15 dB-2.7 dBGaAs pHEMT0.54 mm $\times 0.17 \text{ mm}$ 52.4 GHz14.2% ≤ -13 dB-3.1 dBGaAs pHEMT0.54 mm $\times 0.17 \text{ mm}$ 50.1 GHz11% ≤ -15 dB-2 dB	



Figure 18. Measured S-parameters of the CMRC BPF for DGS S-CPW and Std. CPW. (a) S_{21} . (b) S_{11} .



Figure 19. Photograph of the (a) Std. CPW CMRC BPF. (b) Half DGS S-CPW CMRC BPF. (c) Full DSG S-CPW CMRC BPF.

is 2 dB at 51 GHz in the full DGS S-CPW TLine, 3.1 dB at 54 GHz in the half DGS S-CPW TLins, and 3.7 dB at 56 GHz for standard CPW TLines. A comparison of measured filter frequency responses with and without the slow-wave structure for a fixed chip size demonstrates that the presented slow-wave structure provides favorable frequency shifting and minimal extra loss. The downshift in filter frequencies from 56 GHz to 54 and 51 GHz by the filter, which are attributable to the DGS TLine series inductance and shunt capacitance, supported slow-wave effects. As shown in Fig. 19, filters with and without DGS TLines have the same size of 915 \times 407 µm. Table 3 summarizes the performance of

the designed filters and compares them with the performance of other recently reported mm-wave filter designs. The presented slow-wave structure provides favorable frequency shifting and minimal extra loss in a single design.

5. CONCLUSION

A novel slow-wave CPW Tline structure was developed and adopted to realize V-band compact CMRC BPFs on a GaAs substrate. Owing to the strong slow wave effect, the longitudinal length of the S-CPW is smaller than that of a device with a classical microstrip topology. The S-CPW TLines based compact reconfigurable DGS with an added conventional inductively coupled resonator CMRC BPF enables the resonator to be miniaturized owing to the transversal dimensions of the CPW, without compromising performance in terms of insertion and return loss values. The DGS cell enables reconfiguration of the structure from a low-band to a high-band BPF. The design of the filters with the DGS is elucidated V-band applications.

ACKNOWLEDGMENT

This work is financially supported by the National Science Council [NSC 101-2221-E-182-043-MY3], High Speed Intelligent Communication (HSIC) Research Center and Healthy Aging Research Center (HARC), Chang Gung University, Taoyuan, Taiwan.

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