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A Q-Band Frequency Synthesizer in 0.13 µm SiGe BiCMOS

Jiankang Li[1, 2, *], Yong-Zhong Xiong[2], Jin He[3], and Wen Wu[1]

Abstract—In this paper, a 42 GHz frequency synthesizer fabricated with 0.13 µm SiGe BiCMOS technology is presented, which consists of an integer-N fourth-order type-II phase locked loop (PLL) with a LC tank VCO and a frequency doubler. The core PLL has three-stage current mode logic (CML) and five stage true single phase clock (TSPC) logic in the frequency divider. Meanwhile, a novel balanced common-base structure is used in the frequency doubler design to widen the bandwidth and improve the fundamental rejection. The doubler shows a 41% fractional 3 dB bandwidths with a fundamental rejection better than 25.7 dB. The synthesizer has a maximum output power of 0 dBm with a DC power consumption of 60 mW. The worst phase noise at 100 kHz, 1 MHz and 10 MHz offset frequencies from the carrier is −71 dBc/Hz, −83 dBc/Hz and −102.4 dBc/Hz, respectively.

1. INTRODUCTION

For wireless applications, millimeter-wave (mm-wave) bands are suitable for 24/38 GHz short-range warning radar, satellite communication at 42 GHz, short-range high data rate wireless communication links in the band of 40–45 GHz and 59–64 GHz, long-range automotive radars operating at 76–78 GHz and advanced imaging systems at 94 GHz. Attributed to constantly improvement of Si-based processes, CMOS and SiGe BiCMOS technologies have become great candidates to compete with III-V technologies to implement mm-wave systems and Si based technologies also have the advantages of low power, low cost, larger manufacturing capacity as well as high integration [1].

The synthesizer is a critical component in modern electronic systems [2]. In most communication systems or radar systems, the frequency synthesizer is used to supply a stable clock or convert the transmission data up/down to the desired frequency band. With the operating frequency increased continuously, the design of the fundamental voltage control oscillator (VCO) with wide tuning range and low phase noise becomes more imperative and challenging. Due to the bandwidths of millimeter wave frequency divider and VCO are relatively narrow and difficult to match, a popular approach of constructing a higher frequency source is frequency multiplication for releasing the requirements of the VCO and divider [3]. Thus, broadband frequency doublers with high conversion gain are desired in the mm-wave systems.

In this paper, a 42 GHz frequency synthesizer composed of an integer-N charge pump PLL and a frequency doubler implemented by 0.13 µm SiGe BiCMOS technology is presented. The LC-VCO is used to improve the phase noise and reliability. Meanwhile, considering the operating frequency and power consumption, the combination of three stage current mode logic and five stage true single phase clock circuits in the frequency divider is adopted. Furthermore, in the doubler design, the balanced common-base structure is proposed for increasing the bandwidth and improving the fundamental rejection, which shows a 41% fractional 3 dB bandwidths with a fundamental rejection better than 25.7 dB. The maximum output power of the synthesizer is 0 dBm with a DC power consumption of 60 mW.

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* Corresponding author: Jiankang Li (jkli022@163.com).

[1] The Ministerial Key Laboratory of JGMT, School of Electronic and Optical Engineering, Nanjing University of Science and Technology, Nanjing 210094, China. [2] Semiconductor Device Research Laboratory (SDRL), Terahertz Research Center, CAEP, Chengdu 611731, China. [3] School of Physics and Technology, Wuhan University, Wuhan 430072, China.

2. CIRCUIT DESIGN

Figure 1 shows a block diagram of the frequency synthesizer including a 21 GHz voltage controlled oscillator (VCO), a 1/256 frequency divider (FD), a phase frequency detector (PFD), a charge pump (CP) with an on chip low pass filter (LPF), and a frequency doubler.

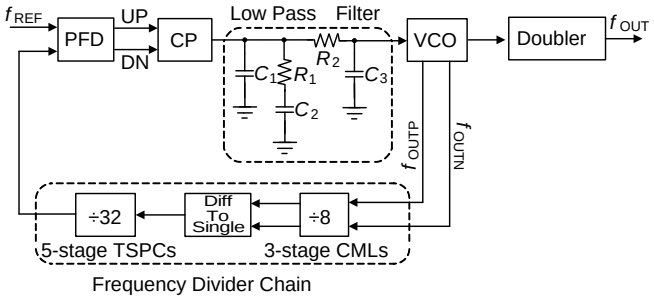


Figure 1. Architecture of the synthesizer.

2.1. Voltage Controlled Oscillator

As ring oscillator is suitable for wideband frequency synthesis but offers too limited signal purity [16] to meet the noise specifications, oscillator with high quality LC tanks is considered for offering superior phase noise performance. Figure 2 shows the schematics of the differential cross-coupled LC-VCO [4–6]. Since the g_m of CMOS and HBT devices are both large enough at the oscillator frequency of 21 GHz in 0.13 µm processes; CMOS devices have the advantages of lower saturation voltage ($V_{\rm sat}$) and better linearity over HBTs, thus NMOS is more suitable for supplying sufficient output voltage swing to drive the next stage. Although HBTs normally performs better $1/f$ noise over CMOS, 60% of phase noise at 1 MHz offset frequency from the carrier is contributed by the resistance thermal noise in this case (from simulation); the overall phase noise of CMOS VCO at 1 MHz is the same with HBT VCO. The VCO core consisted of a NMOS cross-coupled pair, a current source transistor, and an LC tank was properly designed. Moreover, a two-stage source follower is used as the output buffer.

The cross-coupled NMOS transistors M_1 and M_2 generate a negative resistance to compensate the loss of the LC tank. A tail-current in the NMOS transistor M_3 will adjust the current of the VCO core. The LC tank is formed by symmetric spiral inductors L_1 and L_2 together with NMOS varactors C_1 and C_2. To achieve a high quality factor, the inductor is shaped to be octagonal and built in the topmetal-2 layer with thickness of 3 µm and $\sim$ 10 µm away from the silicon substrate, as shown in Figure 3(a). The trace width is chosen to be 7 µm based on the tradeoff between the substrate loss and the resistive loss of metal traces. Furthermore, based on the capacitance of varactor, the space, inner diameter, and turns of the inductor are eventually optimized to be 3 µm, 50 µm, and 1.5, respectively. The performance of

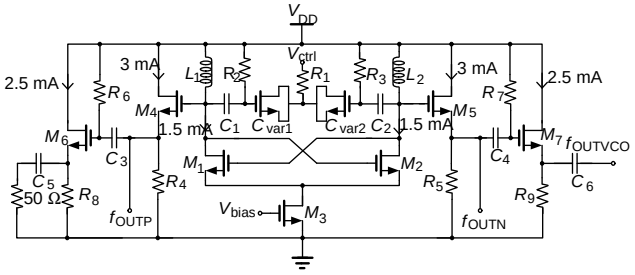


Figure 2. Schematic of the voltage controlled oscillator (VCO) and buffers ($V_{\rm DD}$: 1.5 V).

M_1	M_2		R_1	R_2	R_3
0.13 µm × 25 µm	0.13 µm × 25 µm		10 kΩ	10 kΩ	10 kΩ
M_3	M4		R_4	R_5	R_6
0.13 µm × 55 µm	0.13 µm × 20 µm		100 Ω	100 Ω	10 kΩ
M_5	M_6		R_7	R_8	R_9
0.13 µm × 20 µm	0.13 µm × 40 µm		10 kΩ	200 Ω	200 Ω
M_7	$C_{\rm var1}$		L_1	L_2	C_1
0.13 µm × 40 µm	3 µm × 40 µm		280 pH	280 pH	1 pF
$C_{\rm var2}$	C_2	C_3	C_4	C_5	C_6
3 µm × 40 µm	1 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF

Table 1. Components values of VCO.

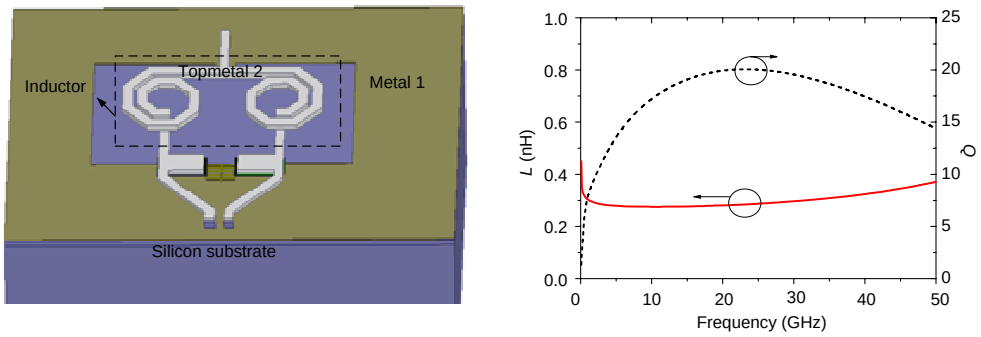


Figure 3. (a) 3-D model of VCO resonate core. (b) Simulation results of inductor.

the inductor is simulated with a 3-D simulator. The simulated inductance is 280 pH and the quality factor is around 20 at 21 GHz, as shown in Figure 3(b). As the foundry cannot provide the standard varactor model, the varactors C_{var1} and C_{var2} are realized by an NMOS device with the source and the drain connected.

Two-stage source follower is designed as the output buffer of the VCO, which features high input impedance to minimize the loading of the VCO core and low output impedance to permit the impedance matching to 50 Ω load. The differential output signals of the first stage buffer are sent to the divider chain; the single-end output signal of the second stage buffer is sent to the synthesizer output terminal, as shown in Figure 2. (The differential signals cannot be tested in our equipment condition and the performance of the single-end Si IC with more grounding pads is more reliable from PCB testing). The component parameters of the VCO are illustrated in Table 1.

2.2. Frequency Divider Chain

As the output frequency of the VCO is around 21 GHz, a static frequency divider can be used. True single phase clock (TSPC) enjoys low power consumption but it can't operate at such a high frequency. Thus, current mode logic (CML) using PMOS load is implemented in the frequency divider to achieve high speed operation with small area [7]. Figure 4(a) shows the schematic of the CML divider. In this work, PMOS transistors replace the poly silicon resistors to act as the loads since the on-chip resistors cannot be controlled precisely in processes. Note that the output of the CML divider chain must be converted to a sufficient swing signal for the subsequent TSPC dividers. The CML-to-CMOS preamplifier is used, as shown in Figure 4(c). The preamplifier can work at high frequency with low power consumption. Since the output frequency of the CML divider chain is around 2.6 GHz, the TSPC dividers are employed to reduce the power dissipation compared with CML. The 1/32 frequency divider which includes 5 divide-by-2 TSPC stages is designed. Figure 4(d) shows the schematic of the divide-by-2 TSPC divider, which mainly consists of an edge-triggered D flip-flop with only 9 transistors.

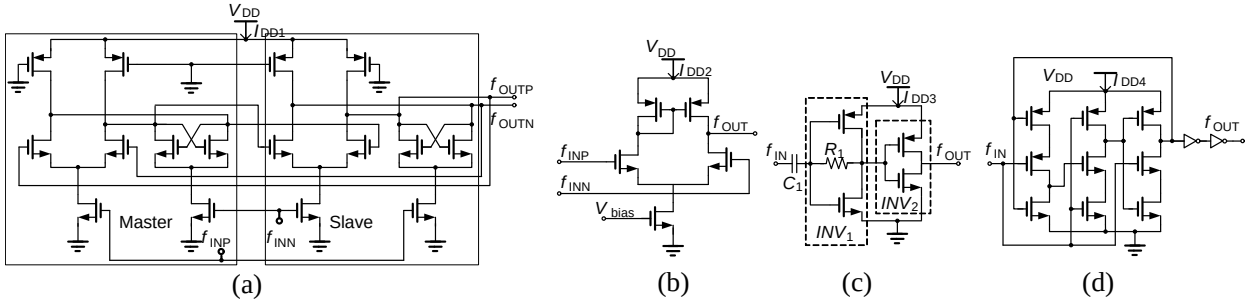


Figure 4. Simplified schematic of the frequency divider chain: (a) CML static divider, (b) differential to single, (c) CML-to-CMOS preamplifier, and (d) TSPC divider.

2.3. PFD, Charge Pump, and Loop Filter

Figure 5(a) illustrates the schematic of the PFD, which is mainly realized by TSPC dynamic D flip-flops (DFFs) [8]. The reset path in the PFD is designed to eliminate the dead-zone problem (caused by insufficient turning on time of the charge pump) effectively. In order to turn the charge pump switches on and off completely, the delay block in the PFD is designed to offer 500 ps. Furthermore, in order to compensate the delay discrepancy between the output signals of UP and DN, a transmission gate with the same delay time of the inverter is employed. The schematic of the CP [9] and LPF is shown in Figure 5(b). Switch transistors M_1 and M_2 are controlled by UP and DN signals and hence, switch the current source transistors M_3 and M_4 to pumping up and down the output voltage V_{ctrl}. The charging current is designed to be 100 µA at a V_{DD} of 1.5 V. The LPF is a third order passive filter and fully integrated on chip. In the design, with the phase margin equals to 56°, the gain of VCO (K_{vco}) is 2.3 GHz/V and the loop bandwidth is 0.5 MHz. The values of components in the LPF are calculated: $R_1 = 10\,\mathrm{k\Omega}$, $R_2 = 45.1\,\mathrm{k\Omega}$, $C_1 = 1.6\,\mathrm{pF}$, $C_3 = 1.6\,\mathrm{pF}$. All the capacitors are implemented by the vertical metal-insulator-metal (MIM) capacitors, the largest capacitor C_2 is optimized to 24.3 pF with the acceptable chip area.

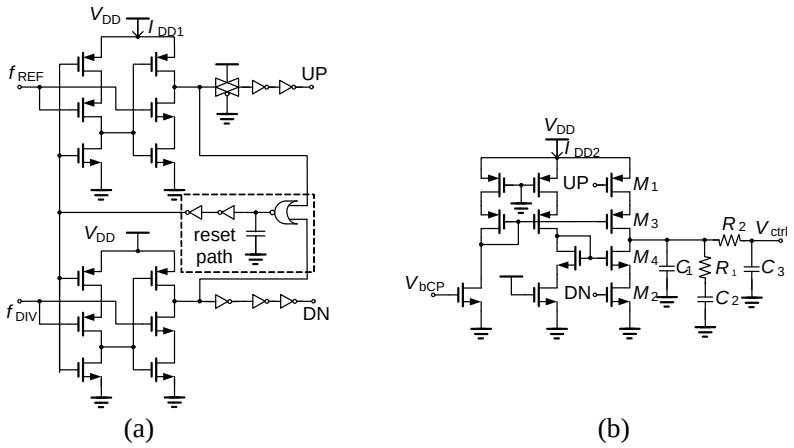


Figure 5. Simplified schematic: (a) phase frequency detector (V_{DD}: 1.5 V, I_{DD1}: 1 mA) and (b) charge pump with loop low pass filter (V_{DD}: 1.5 V, I_{DD2}: 0.3 mA).

2.4. Frequency Doubler

Figure 6 shows the schematic of the proposed frequency doubler which consists of a driver amplifier (DA), a common-base (CB) doubling core and a medium power amplifier (PA). The components values of the doubler are illustrated in Table 2. In the design, the transformer balun is deployed for signal splitting, which is also able to provide impedance matching, and the necessary dc bias for transistors Q_1, Q_2 and Q_3 in Figure 6. The 3-D simulation model of the adopted balun is provided in Figure 7(a). To achieve low insertion loss and broad-bandwidth, the two turns overlay balun is optimized on the two top thick metal layers with the width of 6 µm, the spacing of 4 µm and the inner diameter of 90 µm.

Table 2. Components values of the doubler.

Q_1	Q_2	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
$0.12\times0.48\,\mu\mathrm{m}^2\times4$	$0.12\times0.48\,\mu\mathrm{m}^2\times4$	120 fF	400 fF	170 fF	170 fF	500 fF	500 fF	500 fF	500 fF
Q_3	Q_4	C_9	L_1	L_2	L_3	L_4	L_5	L_6	L_{f1}
$0.12\times0.48\,\mu\mathrm{m}^2\times4$	$0.12\times0.48\,\mu\mathrm{m}^2\times4$	300 fF	0.72	0.19 nH	0.4 nH	0.45 nH	0.3 nH	0.25 nH	0.07 nH
Q_5	L_{f2}	R_1	R_2	R_3	R_4	R_5	R_f		
$0.12\times0.84\,\mu\mathrm{m}^2\times8$	0.07 nH	3.9 kΩ	3.9 kΩ	3.9 kΩ	3.9 kΩ	3.9 kΩ	1 kΩ		

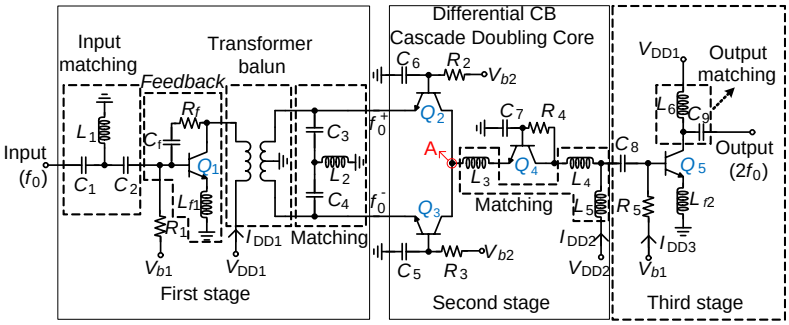


Figure 6. Schematic of the proposed balanced frequency doubler. $V_{b1} = 0.9\,\text{V}$, $V_{b2} = 0.8\,\text{V}$, $V_{\text{DD1}} = 1.6\,\text{V}$, and $V_{\text{DD2}} = 2\,\text{V}$. With input power of $-15.5\,\text{dBm}$, the simulation currents are about $I_{\text{DD1}} = 3\,\text{mA}$, $I_{\text{DD2}} = 2\,\text{mA}$, $I_{\text{DD3}} = 5.5\,\text{mA}$.

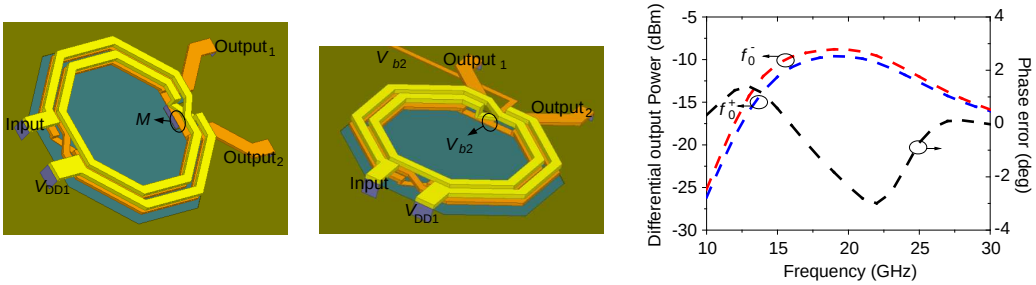


Figure 7. (a) Geometry of the balun. (b) Balun for CE configuration application. (c) Simulation results of the amplitude and phase imbalance of f_0^+ and f_0^- with the input power of $-15.5\,\text{dBm}$ at first amplifier stage.

The differential input signals are fed into the emitters of transistors, Q_2 and Q_3, where both are biased near the class-B region ($V_{b2} = 0.8\,\text{V}$) so as to generate the in phase second harmonic signal efficiently [10]. In the common emitter (CE) doubling configuration, the midpoint (M) of the balun is biased (V_{b2}) through a transmission line, as illustrated in Figure 7(b). This arrangement will introduce the phase imbalance of the differential signals, because the M node is not AC grounded. In our proposed CB doubling configuration, the node M is connected to both the DC and the AC ground, which will ensure the phase balance of the differential signals. Furthermore, the CB doubling configuration can meet the wide bandwidth requirement. C_3, C_4 and L_2 are optimized to balance the magnitude of the balun differential signals and adjust the resonate frequency of the matching network, thereby increases the gain. In Figure 7(c), the simulation results of the powers and the phase error at f_0^+ and f_0^- are presented, which indicates that the difference of the magnitude is smaller than 1.6 dB and the phase error is smaller than 2.7°. These fundamental differential signals cancel each other better and the in phase second harmonic signals enhance each other at node A, shown in Figure 6. Thus, our proposed CB structure can be easily integrated with the balun to achieve the wide bandwidth [11].

Following that, a cascade stage (Q_4) is added to amplify the $2f_0$ signal and improve the isolation between the output and input stage [12]. In the design, three inductors, L_3, L_4 and L_5, are optimized to improve the conversion gain. The simulation results of the dc power consumption and the gain of each stage for the doubler are 5 mA and 8 dB for first stage, 4 mA and 2 dB for second stage, 9 mA and 7 dB for third stage, respectively, with input power of $-15.5\,\text{dBm}$ at 21 GHz.

3. MEASUREMENT RESULTS

The frequency synthesizer were designed and fabricated in a 0.13 µm SiGe BiCMOS technology. The process involves seven metal layers with two top thick metal layers. The NMOS transistors have a

transient frequency (f_T) of around 70 GHz and an oscillate frequency ($f_{\max}$) of around 90 GHz. The bipolar transistors in the process have a f_T of around 250 GHz and a $f_{\max}$ of around 300 GHz. The die micro photograph of the chip is shown in Figure 8; the whole chip area including all the testing pads is 0.83 mm^2. The total power consumption of the frequency synthesizer is about 60 mW — 1.5 V/43 mW (PLL) and 2 V/17 mW (doubler).

Figure 9 shows a chip photograph and measured tuning characteristic and output power of the cross-coupled LC VCO versus the varactor control voltage (V_{ctrl}). The tuning range is about 2.21 GHz ($\sim$ 10.5%) from 19.9 to 22.11 GHz when the V_{ctrl} changes from 0 to 1.5 V. The linear range is about 1.15 GHz from 20.5 to 21.65 GHz with V_{ctrl} varies from 0.55 to 1.05 V. The output power is -14.1 dBm to -12.2 dBm with the tail current of the VCO core is set to 7 mA and the output buffers of the VCO consume around 14 mA of the current.

Figure 10(a) depicts the measured output power of the second harmonic signal $P_{\text{out,2nd}}$ and the fundamental signal ($P_{\text{out,1st}}$) versus the input frequency with -15.5 dBm input power. It is observed that the measured $P_{\text{out,2nd}}$ is between 1.3 and 4.3 dBm and the fundamental rejection is better than 25.7 dB with the input frequency ranging from 13.5 to 20.5 GHz. It is also noted that the measured $P_{\text{out,2nd}}$ is between -0.8 and 4.3 dBm and the fundamental rejection is better than 25 dB with the input frequency ranging from 13.1 to 21.5 GHz. Figure 10(b) demonstrates the measured input/output return losses with an input power of -15.5 dBm. Table 3 summarizes the measured performances of this work and compares them with those of other frequency doubler demonstrated previously. It is evident that the proposed balance CB doubler provides high conversion gain and high output power, with good fundamental rejection under lower dc power consumption.

The output spectrum of the 21 GHz PLL is measured with 10 MHz span and shown in Figure 11 when the synthesizer is locked [16]. It can be observed that the output frequency is from 20.56 to 21.43 GHz when the reference frequency is changed from 80.3 to 83.7 MHz, and the output power is varied from -17.5 to -16.6 dBm with about 2.5 dB lose of the cables and probes. The measured phase

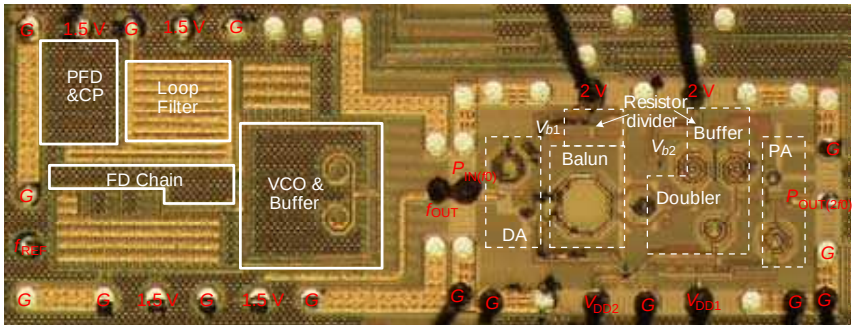
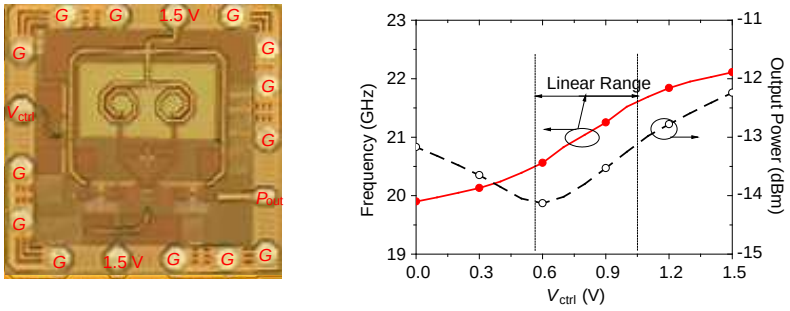


Figure 8. Chip photo of the synthesizer.



(a) (b)

Figure 9. (a) Testing chip photograph of the VCO. (b) Measured tuning characteristic and output power.

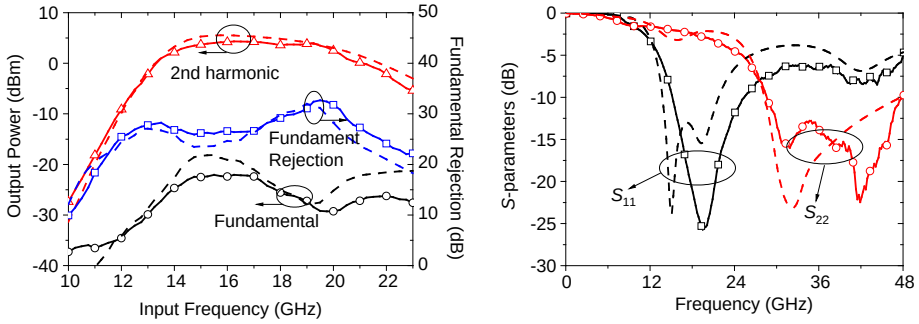


Figure 10. Measured (symbol line) and simulated (dash line) results of doubler: (a) output power and fundamental rejection, and (b) input/output return losses. With input power of −15.5 dBm, $V_{b1} = 0.9$ V, $V_{b2} = 0.8$ V, $V_{\mathrm{DD1}} = 1.6$ V, and $V_{\mathrm{DD2}} = 2$ V.

Table 3. Comparison to the previously reported frequency doubler.

	[13]	[14]	[15]	This work
Technology	0.18 µm CMOS	0.18 µm SiGe BiCMOS	0.35 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS
$P_{\mathrm{in,1st}}$ (dBm)	0	−8	−7	−15.5
F_{out} (GHz)	18–26	36–80	4–18	26.2–43
Conversion gain (dB)	−4.5–−0.5	0.83–10.2	−8–−3	14.7–19.8
P_{out} (dBm)	−4.5–−0.5	−8–1.7	−15–−10	−0.8–4.3
Power consumption (mW)	20.8	137	60	22
Fundamental rejection (dB)	30	20	23	25.7
Chip Area (mm^2)	0.28	0.272	0.77	0.34

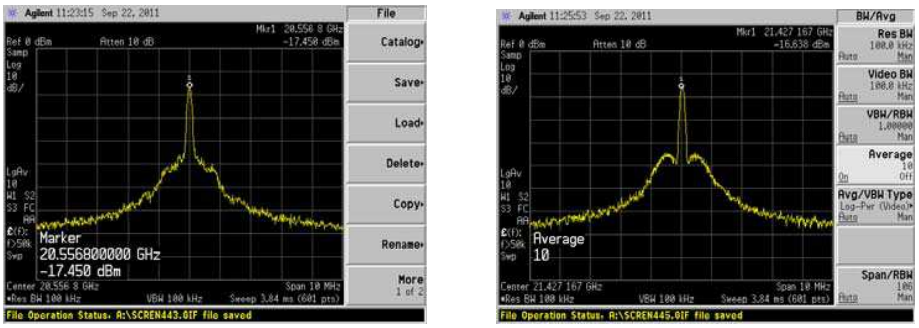
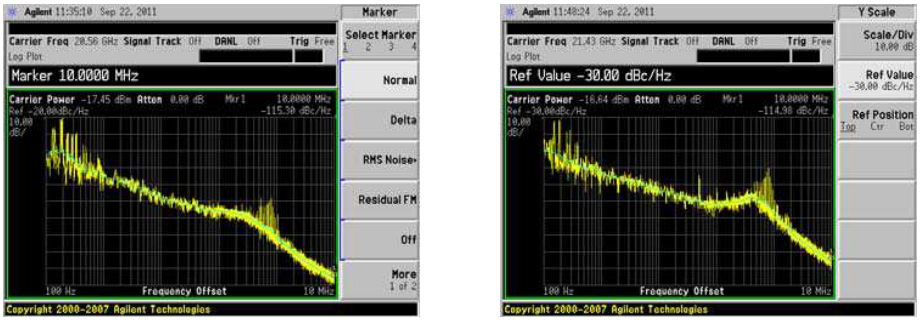


Figure 11. Measured output spectrum: (a) 20.56 GHz and (b) 21.43 GHz.

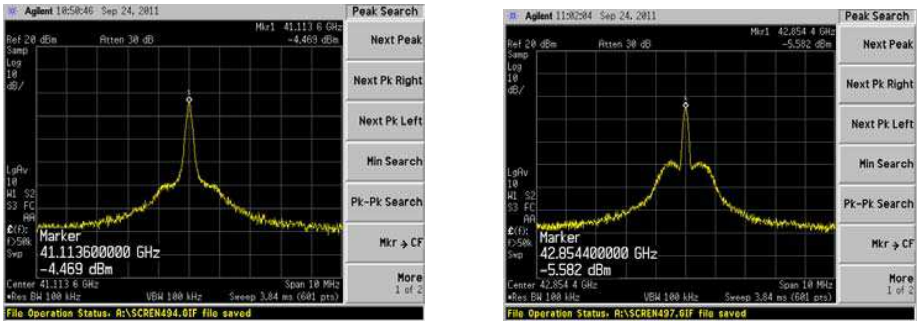
noise is shown in Figure 12. At 100 kHz, 1 MHz and 10 MHz offset frequencies from the carrier, the phase noise is −76 dBc/Hz, −93 dBc/Hz and −115.3 dBc/Hz at 20.56 GHz, −81 dBc/Hz, −89 dBc/Hz and −115 dBc/Hz at 21.43 GHz, respectively.

In order to test the performances of each block and save the total chip area, the 42 GHz synthesizer is achieved by bonding the 21 GHz PLL and the frequency doubler together. The wire bonding interconnection has 0.25 dB insertion loss and a reflection coefficient better than −25 dB in K-band [17]. The output spectrum of the synthesizer (PLL and doubler) is measured with 10 MHz span and shown



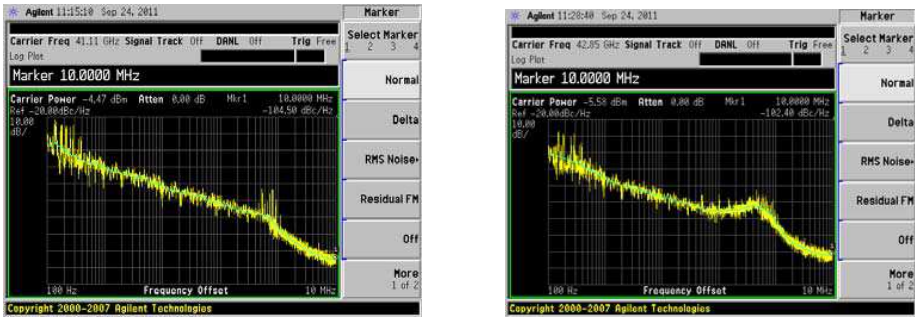
(a) (b)

Figure 12. Measured phase noise: (a) 20.56 GHz and (b) 21.43 GHz.



(a) (b)

Figure 13. Measured output spectrum: (a) 41.11 GHz and (b) 42.85 GHz.



(a) (b)

Figure 14. Measured phase noise: (a) 41.11 GHz and (b) 42.85 GHz.

in Figure 13 when the synthesizer is locked. It can be observed that the output frequency is from 41.11 to 42.85 GHz when the reference frequency is changed from 80.3 to 83.7 MHz, and the output power is varied from −4.47 to −5.58 dBm with about −4.5 dB cable and probe lose. The measured phase noise is shown in Figure 14. At 100 kHz, 1 MHz and 10 MHz offset frequencies from the carrier, the phase noise is −70 dBc/Hz, −86 dBc/Hz and −104.5 dBc/Hz at 41.11 GHz, −75 dBc/Hz, −83 dBc/Hz and −102.4 dBc/Hz at 42.85 GHz, respectively. The difference of the phase noise at ∼20 GHz and ∼40 GHz should be around 6 dB, from the measurement results, the difference is about ∼6 dB and ∼10 dB at 1 MHz and 10 MHz offset. The main reasons are the measurement error and the additional noise contributed by the frequency double. Table 4 summarizes the measured performances of this work and compares them with those of other synthesizers demonstrated previously. It demonstrates the designed PLL can provide the output power up to 0 dBm which is very useful for the millimeter application.

Table 4. Comparison to the previously reported millimeter-wave PLLs.

		[15]	[18]	[19]	[20]	This work	
Technology		0.13 µm CMOS	0.18 µm SiGe BiCMOS	90 nm CMOS	65 nm CMOS	0.13 µm SiGe BiCMOS	
Frequency (GHz)		45.9–50.5	23.8–26.95	39.1–41.6	35–41.88	20.56–21.43	41.11–42.85
Pout (dBm)		−10	−9.5	−18	N.A	−15–−14.1	−1–0
Power consumption (mW)		57	50	64	80	43	60
Divider ratio		1024	256	512–2032	640–1240	256	512
Loop bandwidth		500 kHz	1 MHz	150 kHz	200 kHz	500 kHz	500 kHz
Phase Noise (dBc/Hz)	100 kHz (offset)	−63.5[a]	−71	−72[b]	−65[b]	−81	−75
	1 MHz (offset)	−72	−93.5	−90	−97.5	−89	−83
	10 MHz (offset)	−99	−114[b]	−112[b]	−120[b]	−115	−102
Chip Area (mm^2)		0.87	0.4	1.53	1.1	0.48	0.83

[a] 50 kHz offset from the carrier.
[b] estimated form the phase noise curve.

4. CONCLUSION

A 42 GHz frequency synthesizer composed by a PLL and a frequency doubler has been designed using 0.13 µm SiGe BiCMOS technology. The proposed balance CB doubler provides high conversion gain and high output power, with good fundamental rejection under lower dc power consumption. The synthesizer has a maximum output power of 0 dBm with a DC power consumption of 60 mW. The chip size with input/output pads is 0.83 mm^2. The output frequency from 20.56 to 21.43 GHz shows the worst phase noise with −76 dBc/Hz, −89 dBc/Hz and −115 dBc/Hz at 100 kHz, 1 MHz offset and 10 MHz offset, respectively. The output frequency from 41.11 to 42.85 shows the worst phase noise with −71 dBc/Hz, −83 dBc/Hz and −102.4 dBc/Hz at 100 kHz, 1 MHz offset and 10 MHz offset, respectively.

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