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An RF Transceiver for Wireless Chip-to-Chip Communication Using a Cross-Coupled Oscillator

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Abstract—In this study, we propose a transceiver architecture for wireless chip-to-chip communication using on/off keying (OOK) modulation. The proposed transceiver is composed of an oscillator, coils, an envelope detector, and a Schmitt trigger. Given that the oscillator itself acts as an OOK modulator, the transmitter is simplified. Additionally, because the oscillating signal is coupled with the transmitter and receiver coils, the chip-to-chip communication reliability is improved compared to a pulse-type transceiver. To verify the feasibility of the proposed transceiver, we design a transceiver using a 180-nm complementary metal-oxide-semiconductor process. For a design with a 1.5-GHz oscillation frequency and 1-MHz digital input signal, we verify that the proposed transceiver successfully recovers the original digital signal.

1. INTRODUCTION

Recently, owing to active development of complementary metal-oxide-semiconductor (CMOS) processes, the integration level of integrated circuits (ICs) has significantly increased [1, 2]. Accordingly, the number of ICs that can be obtained from a single wafer has increased dramatically, and hence the unit cost of production has gradually decreased. However, semiconductor process technology is reaching its limit in terms of scaling down the CMOS transistor size, and thus the system size. Accordingly, various semiconductor industries are attempting to develop three-dimensional IC (3DIC) technologies to reduce the overall system size, such as multi-chip packaging (MCP) and through-silicon via (TSV) [3–7].

Figure 1(a) depicts a general two-dimensional IC (2DIC) with bond wires. Compared with 2DIC technology, MCP technology (shown in Fig. 1(b)) successfully results in a more compact overall system. However, as shown in Fig. 1, the bond wires in MCP technology are required to be longer than those utilized in 2DIC technology. The longer bond wires result in a higher parasitic inductance, and hence the operating speed of ICs is limited. In addition, the resonance associated with the inductances of multiple bond wires (and the parasitic capacitances of the input/output circuits of ICs) should be carefully considered for normal operation of each IC. Because of this, the number of stacked ICs in MCP technologies is generally limited to two.

TSV technology could provide one solution to help overcome the drawbacks of MCP technology. A conceptual diagram of TSV technology is presented in Fig. 2(a). In general, it is possible to implement more than four stacked ICs in TSV technologies, as shown in Fig. 2(a). Because the ICs in TSV technology are directly connected with through via holes, the parasitic elements induced by interconnection lines are reduced compared with MCP technology. However, to realize TSV technology, additional semiconductor processes are utilized for the through via holes. Moreover, the yield for the through via holes is generally lower than that for other semiconductor processes. In Fig. 2(b), general case failures for the through via hole processes are illustrated. Even if the yield of a single through

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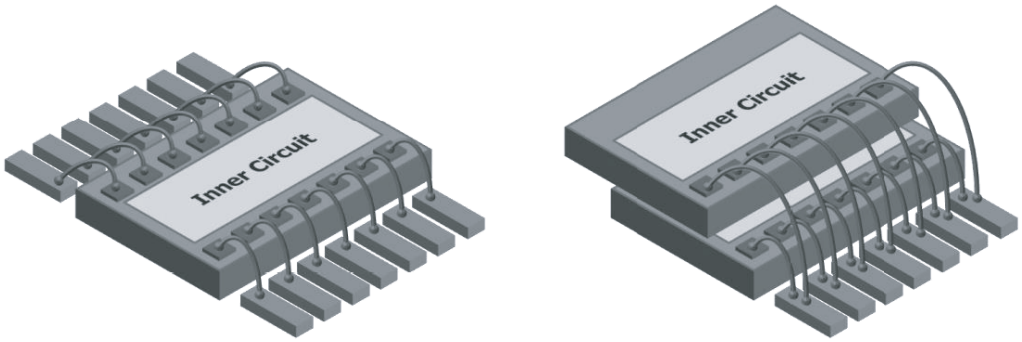
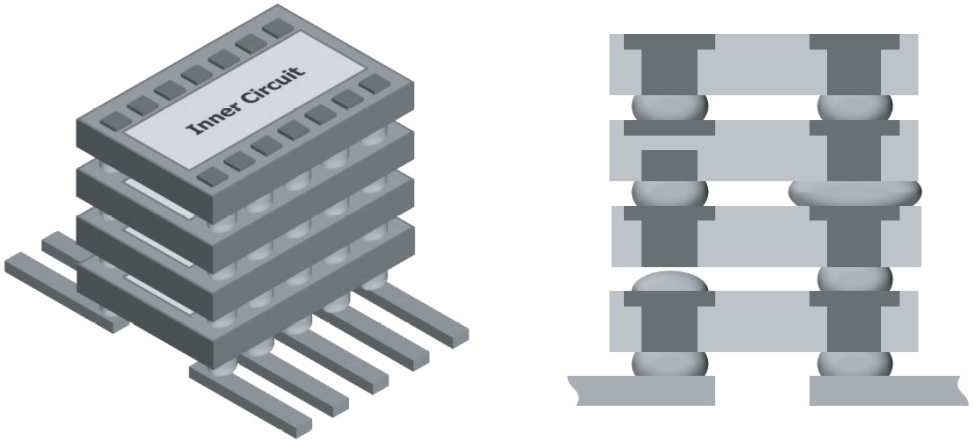


(a) (b)

Figure 1. Typical semiconductor technology: (a) 2D semiconductor and (b) MCP technologies.



(a) (b)

Figure 2. TSV technology: (a) conceptual diagram and (b) general case of failures.

via hole is 99.9%, the overall yield for the TSV technology may be decreased according to the number of pads in the 3DICs using TSV technology. For example, if the number of pads in each IC and the stacked ICs are 20 and four, respectively, then the overall yield for the TSV technology is calculated as 92%.

To enhance the overall yield after the through via hole process, all of the ICs should be checked by on-wafer test systems. However, the cost for testing should be minimized, to reduce the unit cost of the product. Moreover, as shown in Fig. 3, after on-wafer probing on a micro-bump, the resultant scratch on the micro-bump could again reduce the overall yield. To remove the scratch from the micro-bump, an additional re-balling process is required. Consequently, although TSV technology can solve the problems of MCP technology, the associated cost efficiency must be considered.

The feasibility of wireless chip-to-chip communication (WCC) to overcome the drawbacks of TSV technology has already been proven through various previous studies [8–15]. To enhance the overall yields of 3DICs, the usage of through via holes should be minimized by utilizing WCC technology. However, the complexity of typical WCC technology should be moderated for mass production. In this work, we propose a WCC method using on/off keying (OOK) modulation to moderate the complexity of a typical WCC transceiver.

2. PROPOSED HYBRID THREE-DIMENSIONAL IC TECHNOLOGY

Figure 4 illustrates the proposed hybrid 3DIC technology. The V_{DD} and ground nodes in each IC are connected by through via holes, using typical TSV technology. However, the other signals in each IC

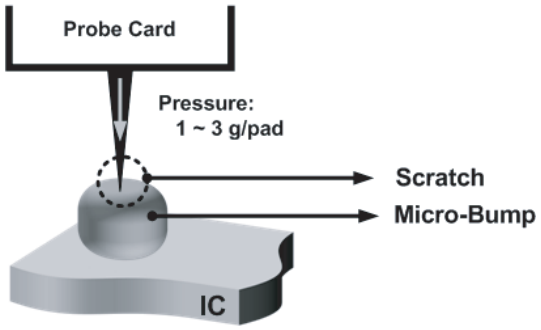


Figure 3. Conceptual diagram of on-wafer probing on a micro-bump.

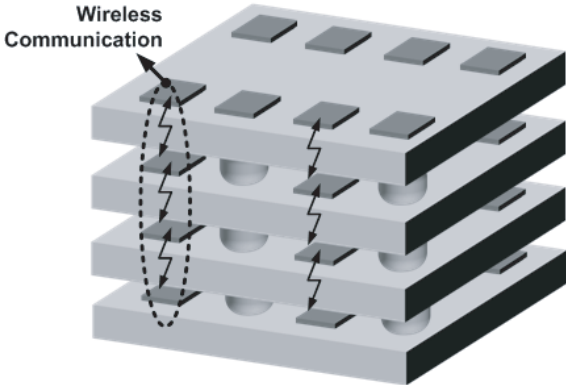


Figure 4. Conceptual diagram of wireless chip-to-chip communication.

communicate using wireless technology instead of TSV. Accordingly, the usage of through via holes can be minimized compared to typical 3DICs, which utilize TSV technology only.

Figure 5 illustrates the conceptual building blocks used in a previous study [8]. As shown in Fig. 5, the input and output voltages of the inverter-type digital transmitter are digital signals. However, given that the magnetic coupling between the transmitter and receiver coils is generated at the rising and falling edges of the output voltage of the inverter-type digital transmitter, the voltage waveform at the output of the receiver coil represents a pulse-type voltage. The voltage at the output of the receiver coil is amplified at the first amplifier stage, which consists of a typical differential amplifier. The amplified signal then enters into a latch to recover the original digital signal. Therefore, the transceiver is a pulse-type WCC transceiver.

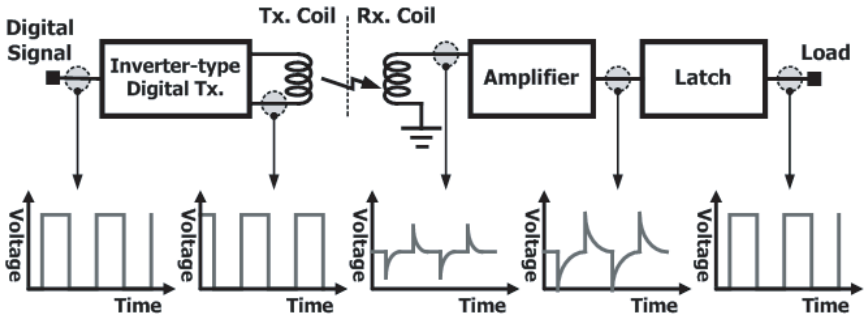


Figure 5. Block diagram of a pulse-type transceiver for WCC technology [8].

In fact, the pulse-type transceiver is designed to support WCC technology with minimal alterations to an existing digital transmitter that supports the wired communication [8]. The reason for this design strategy is to support wireless and wired communication simultaneously with a single transmitter structure. Accordingly, the pulse-type transceiver lacks sufficient optimization for WCC technology. Although a previous study on the transceiver architecture [8] verified the feasibility for WCC, there are some problems associated with the pulse-type input voltage waveform in the receiver coil. Given that the magnitude and width of a received pulse in the receiver coil are dependent on the slew-rate of the digital voltage waveform in the transmitter coil, the slew-rate should be carefully controlled in the transmitter. If the slew-rates of the transmitted voltage waveforms vary according to their signal integrity (SI) or power integrity (PI), then the pulse width and magnitude also vary, and this would affect the duty cycle of the recovered digital signal of the receiver. In the worst case, the receiver could not recover the original digital signal entering into the transmitter. These problems were reported in the previous study [8].

3. PROPOSED WCC TRANSCEIVER USING OOK MODULATION

To overcome the problems identified in the previous study [8], we propose a WCC transceiver using OOK modulation. Fig. 6 shows the conceptual building blocks of the proposed WCC transceiver. The transceiver is composed of an oscillator, coils, an envelope detector, a Schmitt trigger, and a load driver. Unlike the pulse-type transceiver, the transmitted signal is not a pulse-type signal, but rather an OOK-modulated one. Because the pulse-type WCC transceiver only uses single pulses for data transmission, reliability problems arise. However, given that the proposed transceiver uses an OOK-modulated signal for data transmission, the reliability of the proposed transceiver is superior to that of the pulse-type transceiver. The detailed schematics and roles of each of the building blocks are described as follows.

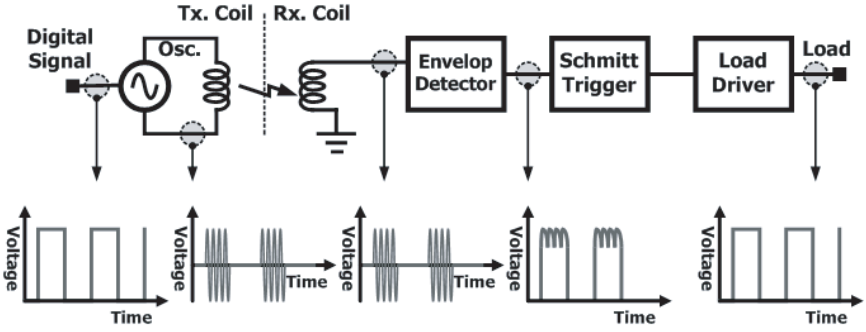


Figure 6. Block diagram of the proposed transceiver.

3.1. Oscillator as Modulator of Transmitter

The cross-coupled oscillator acts as the transmitter, while the inductor acts as the LC resonator and the coil of the transmitter. Fig. 7 presents the schematic of the proposed oscillator for the proposed transmitter. The LC tank of the oscillator determines the oscillation frequency. Unlike a typical cross-coupled oscillator, the proposed oscillator is designed using a cascade amplifier stage. The digital signal enters through the gates of the cascade transistors. The gates of the common-source transistors are cross-coupled, to obtain a positive feedback loop and thereby an oscillatory condition. If the digital signal is 'HIGH', then a feedback loop is created to generate an oscillation signal at the inductor. Conversely, if the digital signal is 'LOW', then the feedback loop is broken to generate a DC voltage at the inductor, as shown in Fig. 7. Consequently, the proposed oscillator itself acts as the OOK modulator.

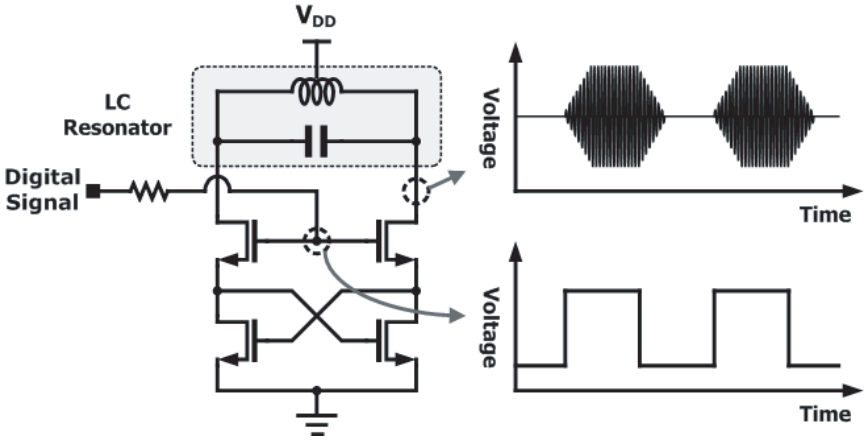


Figure 7. Proposed voltage-controlled oscillator.

In general, the output voltage of an oscillator for mobile applications should be controlled with high accuracy, to obtain a high data rate [16, 17]. Accordingly, the phase noise and harmonic components at the output signal of the oscillator should be sufficiently suppressed for mobile applications. However, the performance of the proposed transceiver is insensitive to the phase noise and harmonic components of the oscillator. As a result, the design parameters and structure of the inductor of the LC tank can be optimized to maximize the magnetic coupling between the transmitter and receiver coils. We perform optimization for the coils according to the optimization method provided in the previous work [9]. To obtain the optimized design parameters of the transmitter and receiver coils, we investigate the various coils with various radii, turn numbers, and metal widths. In this work, the selected inner radius, turn number, metal width, and space between adjacent metal lines of the coil of transmitter are 90 µm, 5, 30 µm, and 3 µm, respectively. For the receiver coil, the selected inner radius, turn number, metal width, and space between adjacent metal lines are 120 µm, 5, 30 µm, and 3 µm, respectively.

In addition, there is no requirement for a phase-locked loop for an accurate operating frequency. Consequently, the transmitter of the proposed transceiver can be simple, and the power consumption of the transmitter is minimized.

Figure 8 presents the simulated results for the oscillator. The digital input signal shown in Fig. 8(a) enters the gate of the common-gate transistor of the oscillator. As depicted in Fig. 8(b), oscillation successfully occurred when the digital input signal was 'HIGH'.

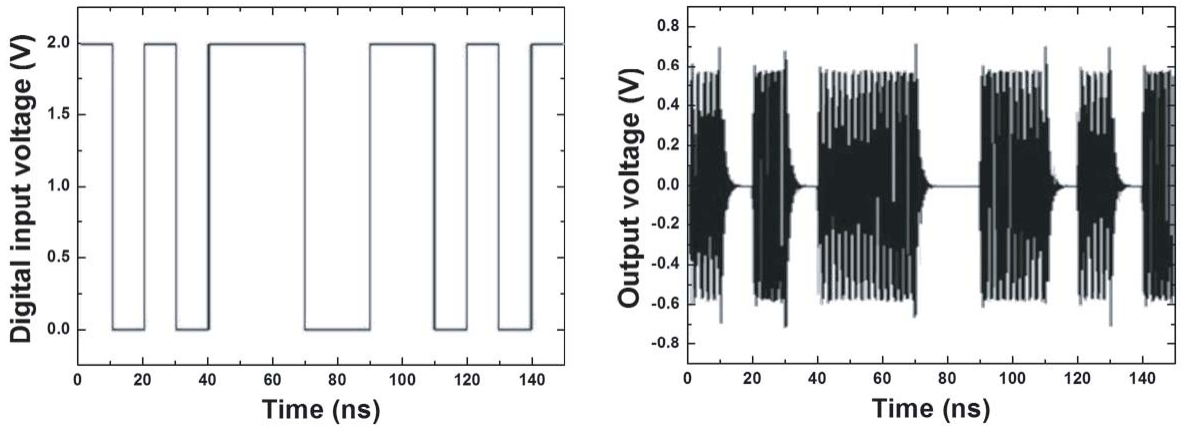


Figure 8. Simulation results: (a) digital input and (b) output voltage waveform of oscillator.

3.2. Envelope Detector

As shown in Fig. 9, a voltage multiplier is employed as the envelope detector of the proposed transceiver. Although low-pass filters, such as RC and LC networks, could be used as the envelope detector, the inductor and capacitor of such a network would require a large chip area. In addition, given that the distance between the transmitter and receiver coils is at least 50 µm (thereby making the voltage of the received signal too weak to drive the Schmitt trigger), a voltage multiplier is instead employed as the envelope detector in the proposed transceiver.

Figure 10 presents the simulated results for the envelope detector. Fig. 10(a) shows the digital input signal of the transmitter. As shown in Fig. 10(b), the output voltage of the envelope detector is in good agreement with the input signal of the transmitter.

3.3. Schmitt Trigger

The output voltage of the envelope detector acts as the input of the Schmitt trigger, which removes the noise and obtains a rectangular digital voltage waveform. In a typical Schmitt trigger, the drains of the P_C and N_C transistors are connected to the ground and V_{DD}, respectively.

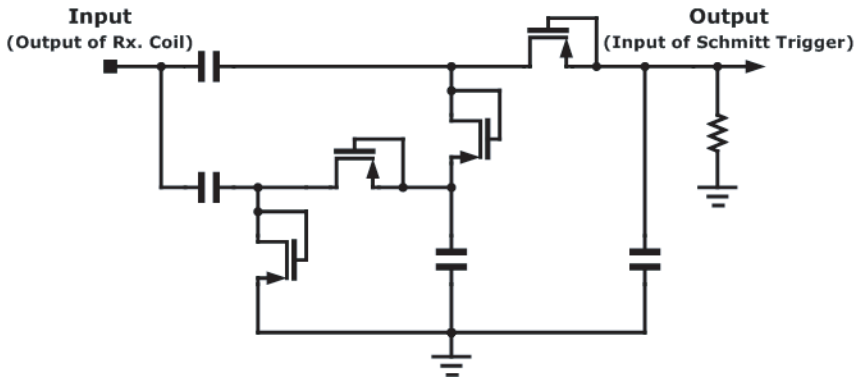


Figure 9. Designed envelope detector.

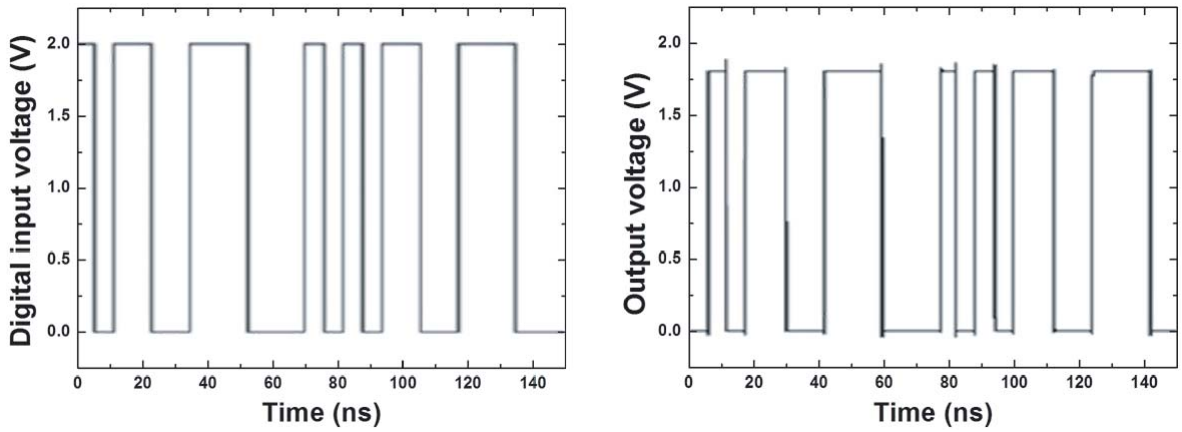


Figure 10. Simulation results: (a) digital input and (b) output voltage waveform of the envelope detector.

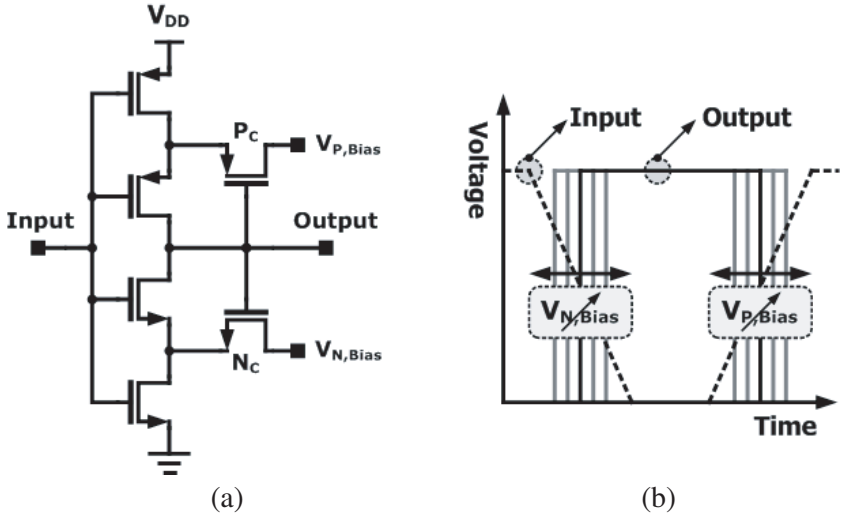
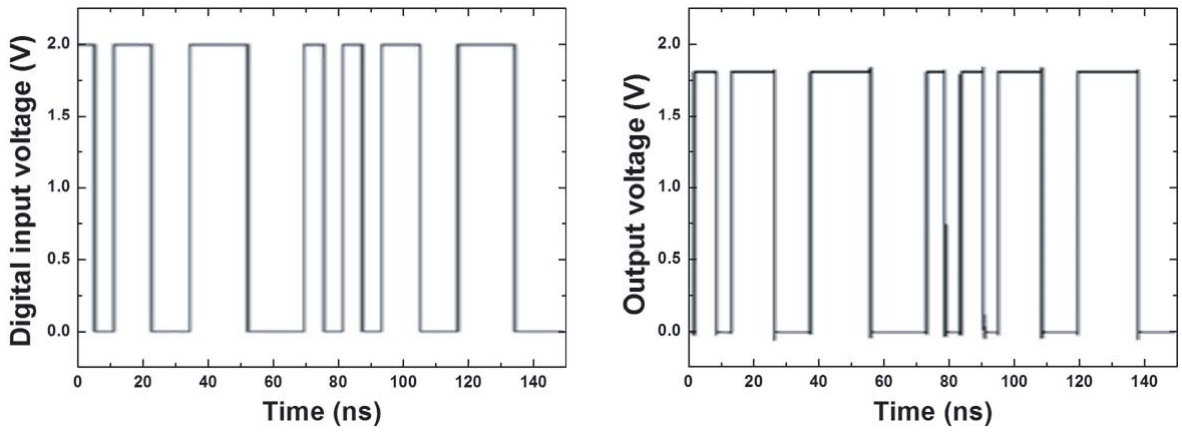


Figure 11. Proposed Schmitt trigger.



(a) (b)

Figure 12. Simulation results: (a) digital input and (b) output voltage waveform of the Schmitt trigger.

In WCC, given that the original digital signals are modulated, wirelessly transferred, and envelope detected for recovery at the end of the receiver, the duty cycle frequently differs between the original and recovered digital signals. Because of this, the transceiver must be able to correct the duty cycle of the recovered digital signal. In this work, a Schmitt trigger is utilized for duty-cycle correction. A simplified schematic of the proposed Schmitt trigger is presented in Fig. 11(a). However, in the proposed Schmitt trigger, we designed the drain voltages of P_C and N_C to be varied. If the drain voltage $V_{P,\text{Bias}}$ of P_C is varied, then the falling edge of the output signal can be controlled. Similarly, if the drain voltage $V_{N,\text{Bias}}$ of N_C is varied, then the rising edge of the output signal can be controlled, as shown in Fig. 11(b). The simulated digital input signal of the transmitter and the output signal of the Schmitt trigger are depicted in Fig. 12(a) and Fig. 12(b), respectively.

4. DESIGN OF THE PROPOSED WCC TRANSCEIVER

To verify the feasibility of the proposed transceiver for WCC using OOK modulation, we design a transceiver using a 180-nm CMOS process, which provides six metal layers. Fig. 13 presents photographs of the chips of the proposed transmitter and receiver. As shown in Fig. 13(a), the transmitter coils act as

(a) (b) (c)

Figure 13. Chip photographs: (a) transmitter, (b) coil of the receiver, and (c) receiver.

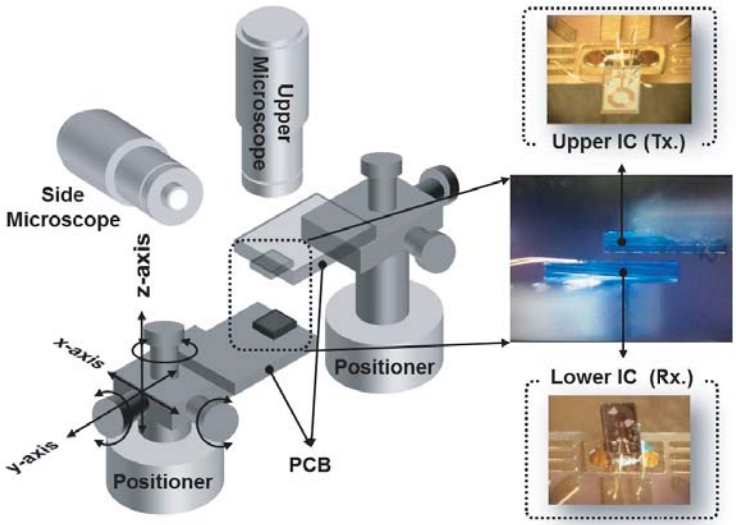


Figure 14. Measurement setup,adapted from [9].

the inductor of the LC tank of the oscillator. As shown in Fig. 13(b), the design utilizes the receiver coil only, without active circuit blocks of receivers, to measure the transmitted oscillation voltage waveform of the oscillator. The receiver shown in Fig. 13(c) includes an envelope detector, Schmitt trigger, and load drivers. The chip sizes of the transmitter, receiver coil, and receiver are 540×1040, 408×780, and $560 \times 1250\,\mu m^2$, respectively.

Figure 14 shows the measurement setup. The measurements were conducted using a face-to-face type transmitter and receiver. The distance between the transmitter and receiver ICs was controlled using the knob of the z-axis of the positioner. Using the focus of the upper microscope and the side view provided by the side microscope, the distance between the transmitter and receiver ICs was adjusted. For the majority of measurements, the distance was fixed at 0.1 mm. Using the upper microscope and knobs of the x-axis and y-axis, the alignment of the transmitter and receiver ICs was adjusted.

Figure 15 depicts the digital input voltage waveform to the transmitter oscillator, and the transferred output voltage waveform. For this measurement, the receiver is composed of only a single coil, without any active circuits, to measure the oscillation characteristics of the oscillator of the transmitter. The measured oscillation frequency is approximately 1.5 GHz, with a 2.0-V supply voltage.

As shown in Fig. 16, we measure the digital input voltage waveform to the transmitter oscillator and the transferred output voltage waveform to verify the functionality of the envelope detector. For this measurement, the receiver is composed of a coil, envelope detector, and load driver, without a Schmitt trigger, to measure the performance of the envelope detector. As shown in Fig. 16, the envelope detector successfully restores the digital input signal of the transmitter.

Figure 17 depicts the digital input voltage waveform to the transmitter oscillator and the output voltage waveform of the receiver. As shown in Fig. 17, the proposed WCC transceiver successfully recovers the original digital signal. In this work, we set the supply voltage of the receiver as 1.1 V. No partial failure cases are observed, unlike for the pulse-type transceiver [8].

As described in Section 2, the latch is essential to complete the pulse-type WCC transceiver. Given that the receiver of the pulse-type WCC transceiver utilizes the pulses transferred from the transmitter coil, the restoration performance of the original digital signal becomes highly sensitive to the bias point of the latch. Moreover, if the SI and PI characteristics are degraded, it becomes more difficult to obtain the optimum bias voltage for the latch. The sensitivity of the performance of the pulse-type WCC to the latch bias voltage results from the pulse-type signal transferred between the transmitter and receiver coils. Given that in this work the OOK-modulated oscillation signals are transferred from the transmitter to the receiver, there is no need for the latch, and therefore no sensitivity to the bias of

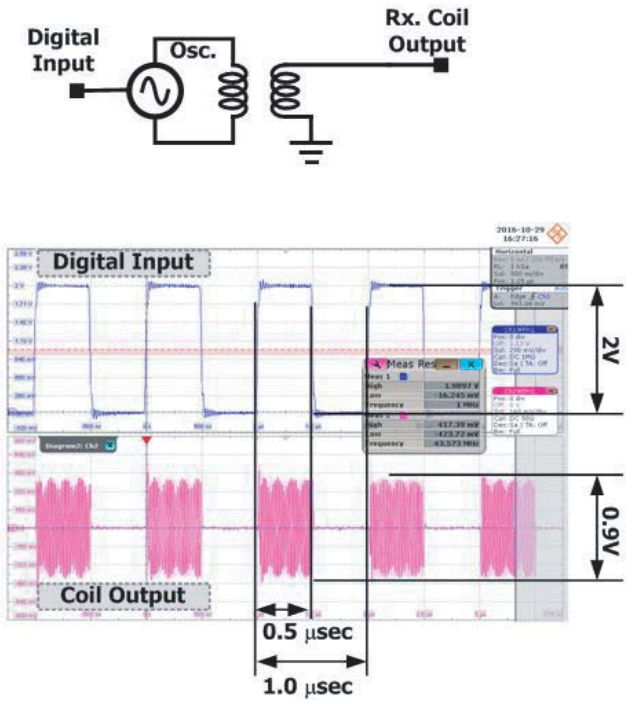


Figure 15. Digital input and measured output voltage waveform at the receiver coil.

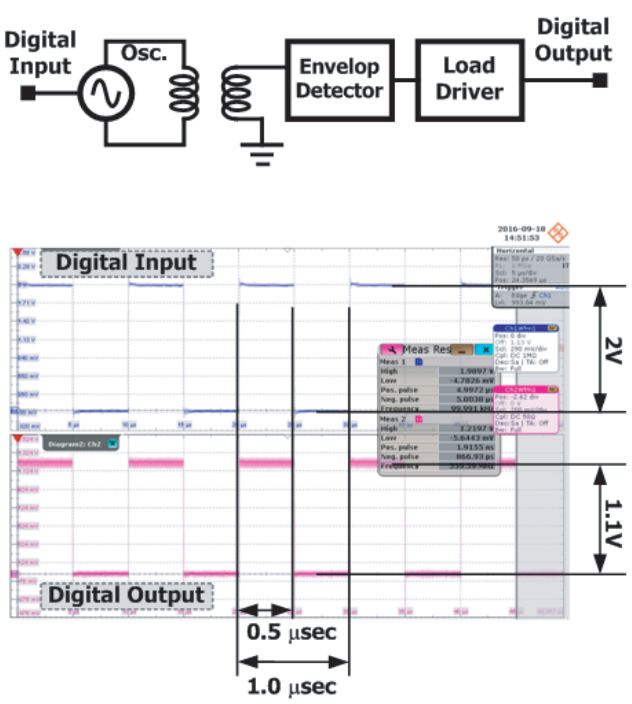


Figure 16. Digital input and measured output voltage waveform with the envelope detector of the transmitter.

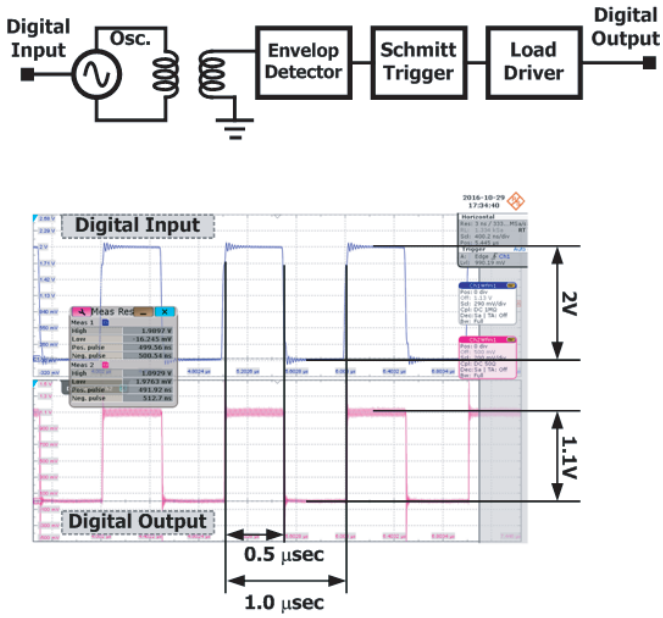


Figure 17. Digital input and measured output voltage waveform of the proposed transceiver.

latch. Consequently, we can consider that the proposed transceiver using OOK modulation is optimized for the WCC technique, while the pulse-type transceiver is designed to support wireless and wired communication simultaneously.

5. CONCLUSION

In this work, we propose a transceiver for WCC using OOK modulation. Unlike the pulse-type transceiver utilized in a previous study, the receiver utilized in this study eliminates partial failure cases and the sensitivity of the latches. To verify the feasibility of the proposed transceiver, we design a transceiver using a 180-nm CMOS process. With a 1 μs digital signal period, the proposed transceiver successfully recovers the input digital signal without any duty-cycle distortion. Therefore, the feasibility of the technology is proven experimentally.

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