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PERFORMANCE TRENDS OF ON-CHIP SPIRAL INDUCTORS FOR RFICS

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Abstract—Performance trends varying with different geometrical parameters for on-chip spiral inductors: (a) with fixed inner-dimension, (b) with outer-dimension, and (c) variation in both inner- and outer-dimensions are extensively investigated in this paper. The relationships for the inductance, Q-factor and self-resonance frequency (SRF) with various geometrical parameters, such as track width, track spacing, and turn numbers are examined on an extensive experiment basis. These performance trends can be a good guideline for practical inductor designs in RFICs.

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1. INTRODUCTION

The rapid development of modern communication systems demands a higher level integration in the design of radio frequency integrated circuits (RFICs) and monolithic microwave integrated circuits (MMICs). These designs cannot be realized satisfactorily in many cases without using the integrated spiral inductors. Thus, knowledge to realize high performance spiral inductors with desired inductance, Q-factor and self-resonance frequency (SRF) is very important. In the past a few decades, great efforts have been devoted to the modeling, optimization and design of the spiral inductors on silicon and GaAs substrates [1–19]. The approaches, such as using high resistive substrate and high conductive metal layers [1], thick dielectric layer [2] or selectively etching off substrates [3], stacking metal layers [4, 5], and even differentially driven inductors [6], have been reported. However, to the authors best knowledge, less effort has been found to systematic studies on the performance trends of inductors varying with different geometrical parameters.

In this paper, thorough studies on the performance trends of different spiral inductors: (a) with fixed inner-dimension, (b) with fixed outer-dimension, and (c) variation in both inner- and outer-dimensions for RFICs are carried out based on extensive experiments. These performance trends varying with geometrical parameters can be a good guideline for practical on-chip spiral inductor designs.

2. CHARACTERIZATION OF SPIRAL INDUCTORS

In most cases, integrated spiral inductors are used in a frequency range that is far away from its first SRF. Under this condition, single-spiral inductors can be accurately characterized [1] by a model shown in Fig. 1. In this model, L represents the spiral inductance; R_s denotes the series resistance of the spiral and varies with frequency in a complicated manner; C_p is mainly due to the overlap between the spiral and the underpass and the capacitive coupling between two adjacent spiral tracks; C_{ox1} and C_{ox2} account for the capacitive coupling between the spiral and the lossy substrate; and R_{si1}, C_{si1}, R_{si2} and C_{si2} are substrate parameters, their values mainly vary with the overall track area for a given substrate and inductive structure. For double-layer spiral inductors, our newly proposed lumped-element equivalent circuit model depicted in Fig. 2 can be very effective. In this model, L_1 and L_2 are the self-inductances of the upper and lower spirals, and M is the mutual inductance between the two spirals. C_p is the fringing capacitor between the two layers and the adjacent spiral tracks; and

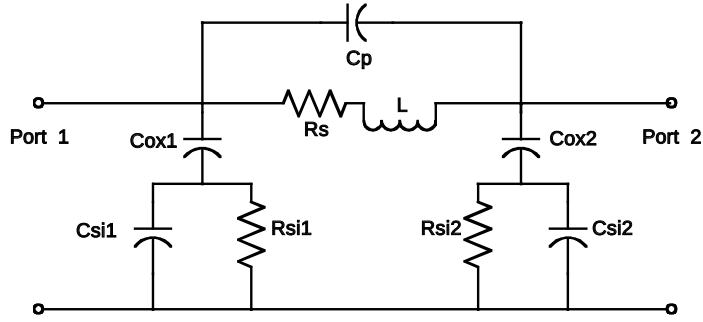

Figure 1. Lumped-element equivalent circuit model of single-layer spiral inductors on silicon substrate.

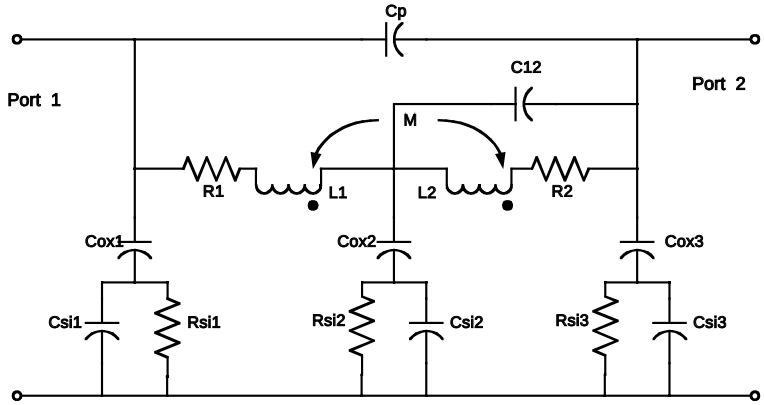

Figure 2. Lumped-element equivalent circuit model of double-layer spiral inductors on silicon substrate.

C_{12} accounts for the direct capacitive coupling between the two spiral inductors and its magnitude can be evaluated by a simple parallel plate capacitance equation $C = \varepsilon \cdot S/d$, where S and d are the overlap area and the distance between two spirals, respectively and ε is the permittivity of SiO_2 separation layer . The other elements have the same physical meaning with those in Fig. 1.

To characterize a spiral inductor, three parameters are usually employed as figure-of-merits, i.e., Q-factor, inductance, and SRF. These parameters determine the performance of a spiral inductor. Thus, they must be extracted accurately. In the following sections, some definitions and extraction methods will be explained first.

2.1. Q-Factor

There are several definitions for Q-factor. The most fundamental definition is the one proportional to the ratio of energy storage to the energy loss per cycle in the device [5, 7]. For an spiral inductor, it can be calculated by [8, 9]

$$Q_{ind} = \frac{\mathrm{Im}\left(\frac{1}{Y_{11}}\right)}{\mathrm{Re}\left(\frac{1}{Y_{11}}\right)} = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{1}$$

where Y_{11} is the input admittance converted from the measured two-port S-parameters. However, (1) has its disadvantage. For instance, Q-factor is zero from (1) at the resonance frequency, which is physically incorrect. Therefore, Yue et al. [10] resolved this problem by obtaining Q-factor from an one-port lumped-element equivalent circuit model, i.e.,

$$Q = \frac{\omega L}{R_s} \cdot \frac{R_p}{R_p + R_s\left[1 + \left(\frac{\omega L}{R_s}\right)^2\right]} \cdot \left[1 - (C_0 + C_p)\left(\frac{R_s^2}{L} + \omega^2 L\right)\right]. \tag{2}$$

In (2), the first term accounts for the magnetic energy stored and the series loss in the spiral. The second term denotes the substrate loss factor representing the energy dissipated in the semi-insulating silicon substrate. The last term is the self-resonance factor, representing the reduction in Q-factor due to the increase in the peak electric energy with increasing frequency. This equation is very useful for getting an optimized Q-factor in the design of a spiral inductor. Another definition presented in [7, 8] is to extract Q-factor by numerically adding a capacitor in parallel to measured Y_{11} of an inductor, and by computing the frequency stability factor and 3-dB bandwidth at the SRF. As (1) can be accurate up to the first SRF for spiral inductors and is easy to implement, it will be adopted in this paper.

2.2. Inductance (L) Extraction

The L value of an inductor is frequency-dependent. Physically, it decreases with frequency because of the current crowding at the edges of the conductors, which leads to a decrease in internal inductance. For a highly conductive substrate, the eddy current induced in the substrate also leads to a decrease in the overall L as a function of frequency. As the induced current is opposite to the current flowing

in the track, it will partially cancel the magnetic field generated by the inductor, thus decreasing the overall L. However, for on-chip spiral inductors, L is an increasing function of frequency. This is primarily due to the coupling capacitance, which boosts the effective L. The L value of an on-chip spiral inductor depends, therefore, on its operation frequency in practical applications. Furthermore, L is in fact an effective value as it includes the parasitic effects. Thus, different methods must be used to extract its value according to different applications. In most cases, the spiral inductor can be configured either in a "grounded" or in a "floating" form in integrated circuits. When used in a "grounded" form, it operates in one-port mode with the other port grounded. Therefore, L is determined by [9]

$$L = \frac{\mathrm{Im}\left(\frac{1}{Y_{11}}\right)}{2\pi f} \tag{3}$$

where f is the operating frequency. As (3) includes the substrate parasitic effects of C_p, R_s, C_{ox1}, C_{si1} and R_{si1}, it is widely used by researchers. When a spiral inductor is used as a two-port device, L of the spiral inductor is obtained from the mutual admittance of a two-port system by [11]

$$L = \frac{\mathrm{Im}\left(\frac{1}{Y_{21}}\right)}{2\pi f}. \tag{4}$$

Obviously, (4) ignores the parasitic effects of the substrate, resulting in a higher SRF value than that of the "grounded" case.

No matter what is the definition through which L is obtained, L values should be very close to each other at low frequencies that are far from the first SRF of the inductor. As most of the researchers did, (3) will be adopted in our studies.

2.3. SRF

At a certain frequency, resonance will occur due to the parasitic effects of the substrate and the distribution characteristic of metal tracks. After the SRF point, the inductor has a negative reactance value, thus behaves as a capacitor. Usually, the inductors are required to operate at frequencies far from its SRF. When self-resonance happens, the inductive reactance and parasitic capacitive reactance become equal. This means that the imaginary part of the one-port input impedance is equal to zero, so the frequency where $\mathrm{Im}(Z_{in})$ becomes zero is the

resonance frequency. In a two-port system, S_{11} associates with the input and output impedances by

$$S_{11} = \Gamma = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{5}$$

where $Z_0 = 50\Omega$ in our measurement system, and $\mathrm{Im}(Z_{in}) = 0$ at SRF. Thus, S_{11} is a real number. When we plot the S_{11} in a Z-Smith chart, the SRF value is at the point where the S_{11} trace crosses the horizontal axis of the Smith chart.

3. EXPERIMENTAL RESULTS AND DISCUSSIONS

3.1. Fixed Inner-Dimension of the Spiral Inductors

A set of circular spiral inductors is fabricated with standard silicon IC technology. These inductors have the same inner-dimension (r) of $30\,\mu$m but with a variation in one or more parameters of the metal track width W, track spacing S, and turn number N. The fabrication parameters are shown in Table 1.

Table 1. Fabrication parameters for inductors under test (R_{sh}: sheet resistance).

Item	Thickness (μm)	ρ ($\Omega \cdot$ cm)	ε_r	Metal	Thickness (μm)	R_{sh} (mΩ/square)
		10^{10}	4.1	M5	0.99	41
Sepration4	1.57	10^{10}	4.1	M4	0.57	76
Sepration3	1.57	10^{10}	4.1	M3	0.57	76
Sepration2	1.57	10^{10}	4.1	M2	0.57	76
Sepration1	1.57	10^{10}	4.1	M1	0.57	76
OIL	0.8	10^{10}	4.0			
Substrate	700	10^{10}	11.9			

There are five levels of metals above the oxide isolation layer (OIL), and each has a thickness of $0.57\,\mu$m and a separation of $1\,\mu$m between one another. M5 is the top metal, realizing on top of the dielectric with a relative permittivity of 4.1. M1 to M4 are embedded wholly in the dielectric. This set of inductors is fabricated with different processings. The first processing is used for inductors numbered from 1 to 15, and it uses M5. The second processing using M4 is for inductors numbered from 16 to 19. The third processing is used for inductors numbered from 20 to 23, using M3. And the fourth

processing is used for those with Nos. 24–26, which are double-layer inductors using both M5 and M4. Other geometrical parameters are shown in Table 2.

Table 2. Geometrical descriptions for the tested inductors.

No.	*N*	*W*	*S*	*No.*	*N*	*W*	*S*
1	2.5	10	2	14	6.5	10	1.5
2	3.5	10	2	15	7.5	10	1.5
3	4.5	10	2	16(M4)	2.5	10	1.5
4	5.5	10	2	17(M4)	3.5	10	1.5
5	6.5	10	2	18(M4)	4.5	10	1.5
6	7.5	10	2	19(M4)	5.5	10	1.5
7	2.5	18	2	20(M3)	2.5	10	1.5
8	3.5	18	2	21(M3)	3.5	10	1.5
9	4.5	18	2	22(M3)	4.5	10	1.5
10	2.5	10	1.5	23(M3)	5.5	10	1.5
11	3.5	10	1.5	24(M5,4)	2.25	10	1.5
12	4.5	10	1.5	25(M5,4)	3.25	10	1.5
13	5.5	10	1.5	26(M5,4)	4.25	10	1.5

According to their geometrical parameters, these inductors can be categorized into four groups. The first group consists of Nos. 1–6 corresponding to Nos. 10–15, respectively. These inductors have the same W with N increasing from 2.5 to 7.5. The S's are $2\,\mu$m and $1.5\,\mu$m, respectively. The L and Q-factor values for inductors with N ranging from 2.5 to 7.5 are extracted and shown in Figs. 3–6.

In Figs. 3–6, it is easily seen that L increases with N. However, both the maximum value of Q-factor ($Q_{\max}$) and SRF decrease with N. It is true that when N increases, the length of the metal track will increase; and this increases the total inductance, overall resistance and the parasitic capacitance. As a result, $Q_{\max}$ and SRF will decrease accordingly. Q-factor at first increases with frequency. At a certain frequencyroughly at the half value of SRF, it reaches its peak value and then rolls off to zero. This is because at low frequencies, the metal resistance R_s is nearly constant and dominates the loss, while L increases with the frequency. As a consequence, Q increases with the increasing frequency. However, when the frequency increases to a certain value (determined by its physical layout), the substrate dissipation becomes serious, the eddy current and the skin effect will also make the metal resistance an frequency-dependent value, making the loss larger than that at the lower frequency range. With these high

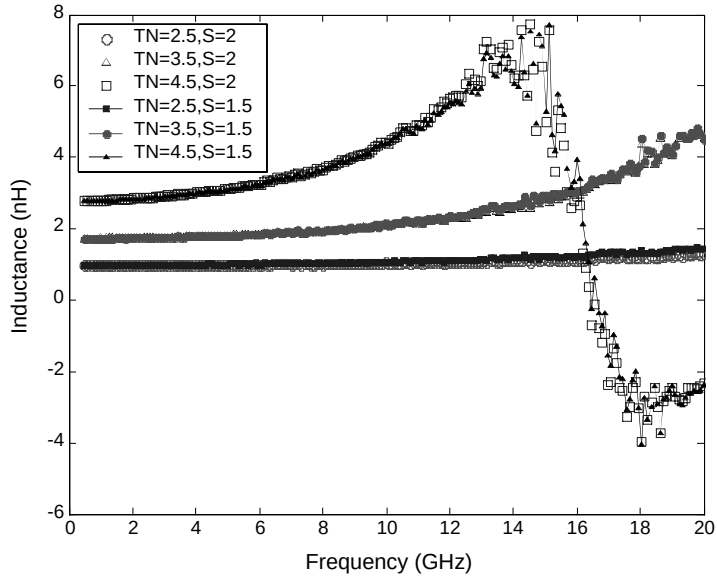

Figure 3. Inductance as a function of frequency for Nos. 1–3 and 10–12, respectively.

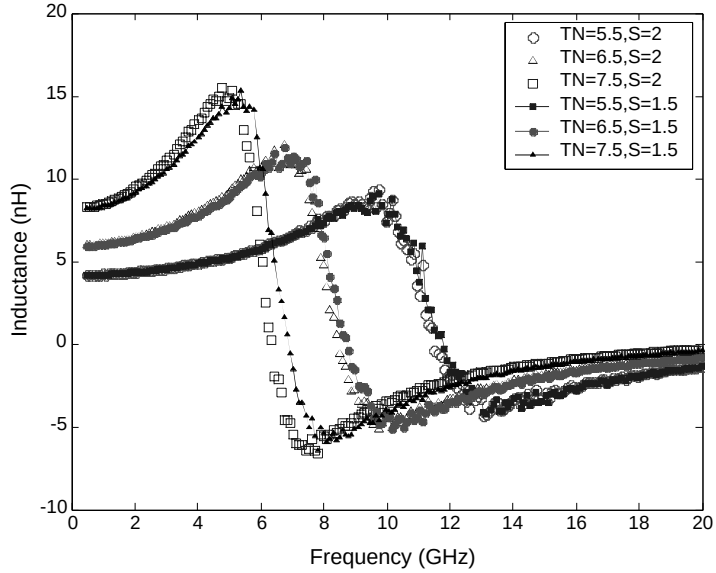

Figure 4. Inductance as a function of frequency for Nos. 4–6 and 13–15, respectively.

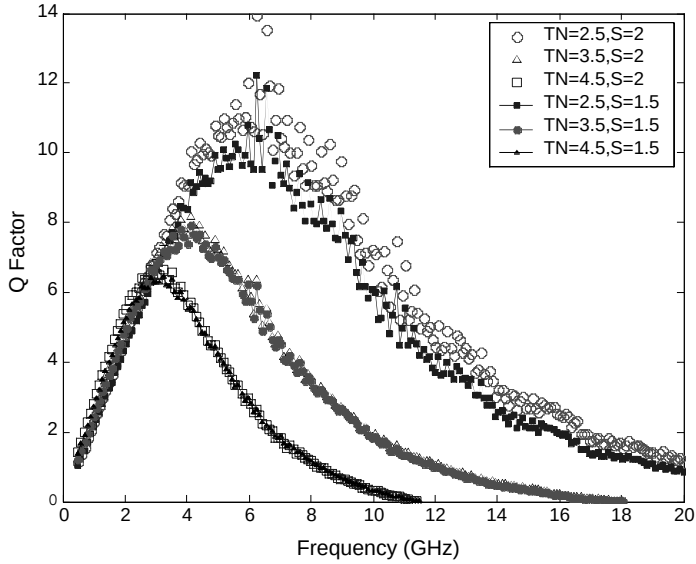

Figure 5. Q-factor as a function of frequency for Nos. –3 and 10–12, respectively.

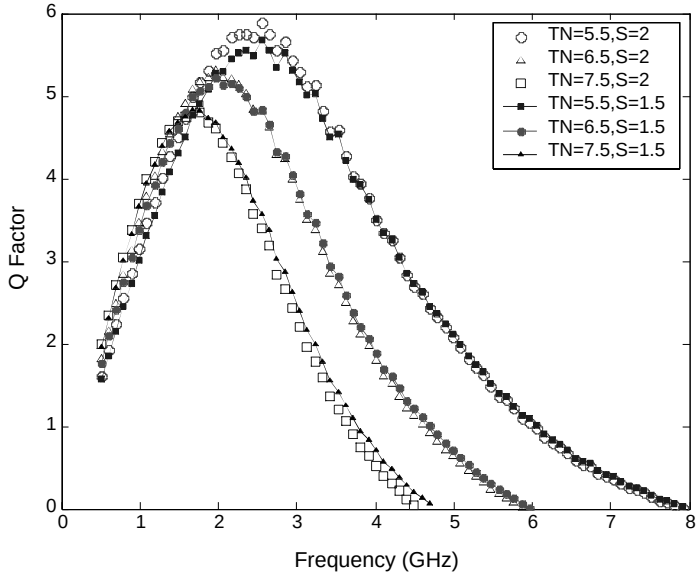

Figure 6. Q-factor as a function of frequency for Nos. 4–6 and 13–15, respectively.

frequency adverse effects, Q-factor gradually reaches its peak and then begins to roll off.

A closer examination of Figs. 3–6 also reveals some other facts. When S increases from $1.5\,\mu$m to $2\,\mu$m, L has a slight increase, which is more obvious for inductors with large N. However, SRF has a slight decrease. The change for $Q_{\max}$ is more complicated, it increases slightly first and the increase becomes less and less with N increasing. At $N = 7.5$, the two inductors have a nearly identical $Q_{\max}$ value. Physically, when S increases, the total length of the spiral increases accordingly for a given inductor with fixed r, W and N. This length increase results in a higher L, a higher series resistance and a larger occupied chip area. The increase in the occupied chip area will cause the increase in substrate loss and spiral-to-substrate parasitic capacitance. The simultaneous increase in L and substrate parasitic capacitance attributes to a lower SRF. The increase in L has the tendency to enhance Q-factor, while the increase in series resistance and substrate loss degrades Q-factor. For a small N, the enhancement of Q-factor may due to the overall effect that increases in L outweigh the increase in metal and substrate loss. For a large N, due to longer metal length and larger chip area occupation, the loss increase may dominate and lead to a lower $Q_{\max}$. Thus, from Figs. 5–6, it can be predicted that for $N > 7$, $Q_{\max}$ for inductors with $S = 1.5\,\mu$m is larger than that for inductors with $S = 2.0\,\mu$m in our case.

The second group consists of inductors Nos. 1–3 and Nos. 7–9, respectively. These inductors have an S of $2\,\mu$m while W increases from $10\,\mu$m to $18\,\mu$m. Also, L and Q-factor values are plotted as a function of frequency in Figs. 7 and 8, respectively.

It is clear that L increases with W and N. When W increases, however, the increasing magnitude of L is seen obviously only for inductors with large N. In other words, changing W has a little effect on the L value for the inductors with small N. As for the Q-factor, $Q_{\max}$ decreases with W and N. However, before $Q_{\max}$, Q-factor for the inductors with a larger W is larger than that of their narrower counterparts. This tendency is reversed after $Q_{\max}$ occurs. Just as pointed out previously, at low frequencies, the loss dominates by the constant metal resistance. The increase in W will decrease the metal resistance. That is why at low frequencies (at the point before $Q_{\max}$), Q-factor for inductors with a wider track width will be a bit higher than that of those inductors with a narrower track width. Also, at this frequency range, the effect of parasitic capacitance takes place at a lower frequency point for inductors with a larger W. As a result, $Q_{\max}$ occurs at a lower frequency point. Furthermore, SRF will also decrease with W due to the increased occupied chip area.

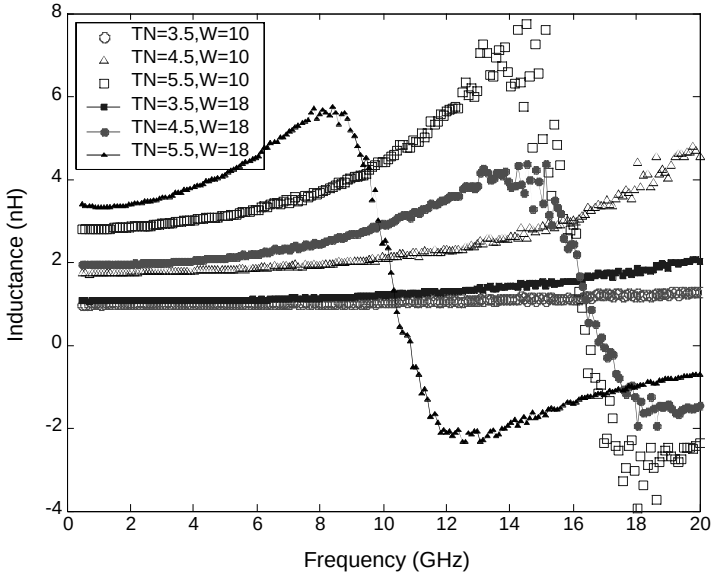

Figure 7. Inductance as a function of frequency for Nos. 1–3 and 7–9, respectively.

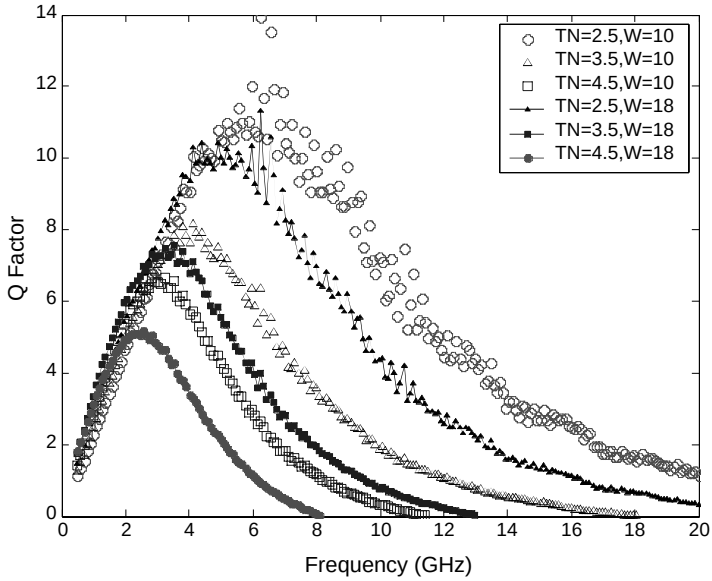

Figure 8. Q-factor as a function of frequency for Nos. 1–3 and 7–9, respectively.

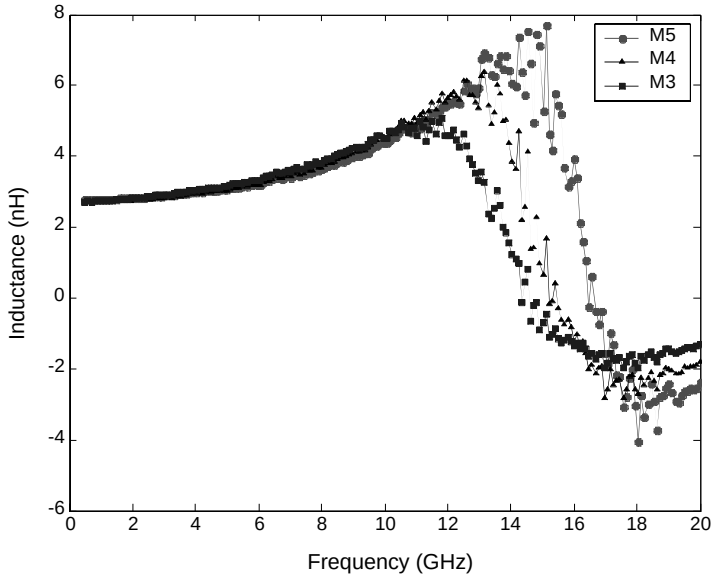

Figure 9. Inductance as a function of frequency for Nos. 12, 18, and 22 ($N = 4.5$), respectively.

The third group consists of inductors implemented with different metal layers using multi-layer interconnect technology. For those inductors with Nos. 10–13, they are implemented on M5. These with Nos. 16–19 are implemented using M4 while those with Nos. 20–23 using M3. The N value for them increases from 2.5 to 5.5 with an increase step of 1. Their L values and Q-factors for $N = 4.5$ are plotted as a function of frequency ranging from 0.5 to 20 GHz in Figs. 9 and 10, respectively.

It is obvious that using different metal layers to implement spiral inductors has little influence on L, especially at low frequencies. However, the influence on Q-factor is significant. The inductors implemented with M4 have a $Q_{\max}$ higher than that of their counterparts of the same N, implemented with M5 or M3. This is probably because of the larger loss to the air for inductors using M5 and to the substrate for the inductors using M3. However, the inductors implemented with M5 have a highest SRF, followed by those using M4, and then M3. This is self-explained as the lower the metal level used, the shorter the distance between the spiral and the substrate becomes. Thus, the substrate parasitic capacitance will be larger, resulting in a lower SRF.

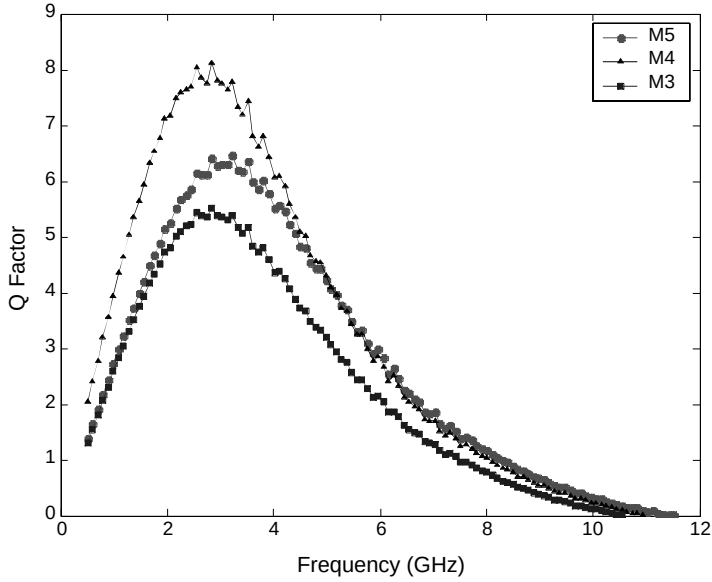

Figure 10. Q-factor as a function of frequency for Nos. 12, 18 and 22 ($N = 4.5$), respectively.

The fourth group consists of inductors Nos. 10–12 and Nos. 24–26, respectively. Nos. 10–12 are single-layer inductors, implemented with M5. Nos. 24–26 are double-layer inductors, using M5 and M4. For comparison, L and Q-factor values as a function of frequency are shown in Figs. 11 and 12, respectively.

It is easily seen that double-layer spiral inductors have a much larger L than that of the single-layer inductors, especially for large N. However, $Q_{\max}$ and SRF decreases very rapidly, resulting in a very narrow bandwidth.

3.2. Fixed Outer-Dimension of the Spiral Inductors

It is known that the polygon spirals with more than four sides have higher Q-factor than that of the square spirals with the same area, so it is advantageous to use polygon structures in inductor designs [8]. In view of this, various octagonal spiral inductors with different geometrical parameters are fabricated and tested. Their detailed descriptions for geometrical parameters are tabulated in Table 3.

Based on their geometrical parameters, these inductors can be divided into several groups. For Group 1 (G1: Nos. 1–4), W, S and r

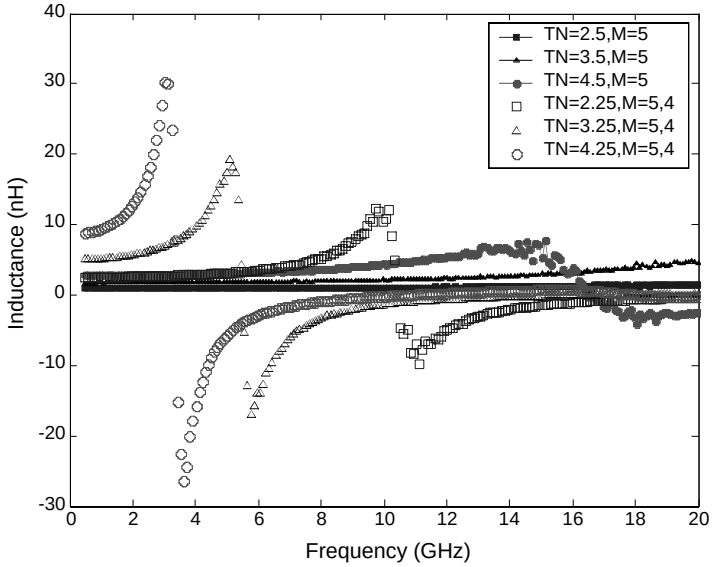

Figure 11. Inductance value as a function of frequency for Nos. 10–12 ($M5$) and Nos. 24–26 ($M = 4, 5$), respectively.

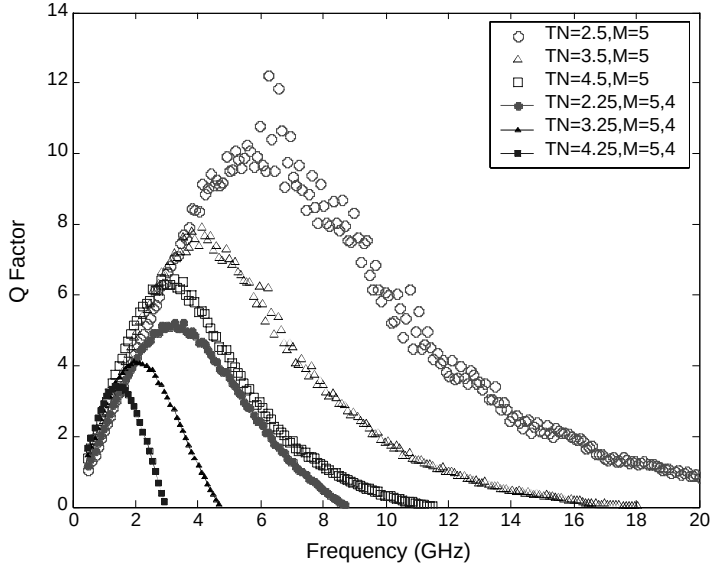

Figure 12. Q-factor as a function of frequency for Nos. 10–12 ($M5$) and Nos. 24–26 ($M = 4, 5$), respectively.

Table 3. Geometrical parameter descriptions for spiral inductors with fixed outer-dimension or variation in both outer- and inner-dimension.

Inductor	N	$W\,(\mu\mathrm{m})$	$S\,(\mu\mathrm{m})$	$D\,(\mu\mathrm{m})$	$r\,(\mu\mathrm{m})$
1	3	8	4	220	74
2	4	8	4	220	62
3	6	8	4	220	38
4	8	8	4	220	14
5	4	4	4	220	78
6	4	6	4	220	70
7	4	14	4	220	38
8	4	8	1	220	74
9	4	8	2	220	70
10	4	8	6	220	54
11	4	8	4	140	22
12	4	8	4	180	42
13	4	8	4	280	92

are fixed while $N = 3$, 4, 6 and 8, respectively. Figs. 13 and 14 depict L and Q-factor each as a function of the operating frequency. It is obvious that L increases with N, while the maximum Q-factor ($Q_{\max}$) decreases with N. Below $Q_{\max}$, Q-factors for inductors with small N are smaller than those with large N. Such a case is reversed for Q-factors above $Q_{\max}$.

The relationships between N and L, $Q_{\max}$ are plotted in Fig. 15. The smooth curves are obtained by using the least squares curve fitting technique based on the measurement results. This figure is valid for N ranging from 3 to 8. Within this range, we can design an inductor with L ranging from 3.5 to 8 nH and $Q_{\max}$ ranging from 3.8 to 7.

Fig. 16 shows SRF as a function of N for inductors in G1. Obviously, the larger N an inductor has, the lower SRF it would have. This is because both the inductance and capacitance values increase with N, and as a result SRF decreases.

For Group 2 (G2: Nos. 2, 5, 6, and 7), the inductors are fabricated with fixed $N = 4$, $S = 4\,\mu$m, and $D = 220\,\mu$m, corresponding to track width $W = 4\,\mu$m, $6\,\mu$m , $8\,\mu$m , and $14\,\mu$m, respectively. Their L values and Q-factors versus frequency are shown in Figs. 17 and 18.

It is easily seen that L decreases while Q-factor increases with

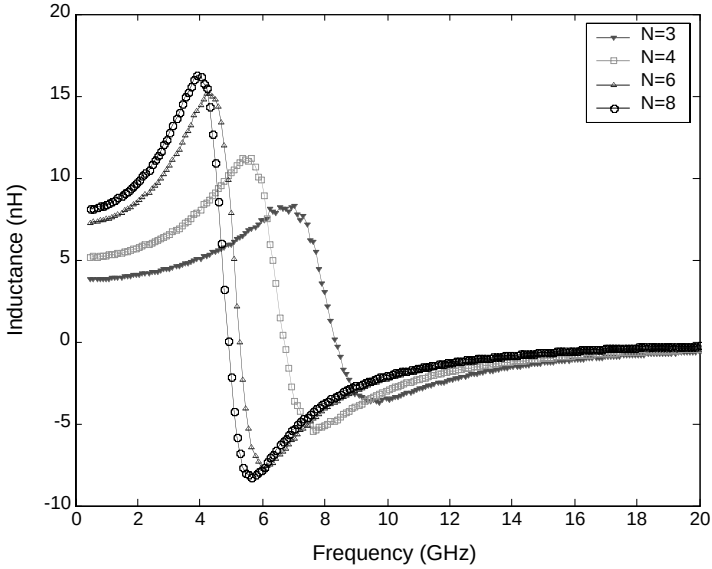

Figure 13. Inductance as a function of frequency for inductors with different N's.

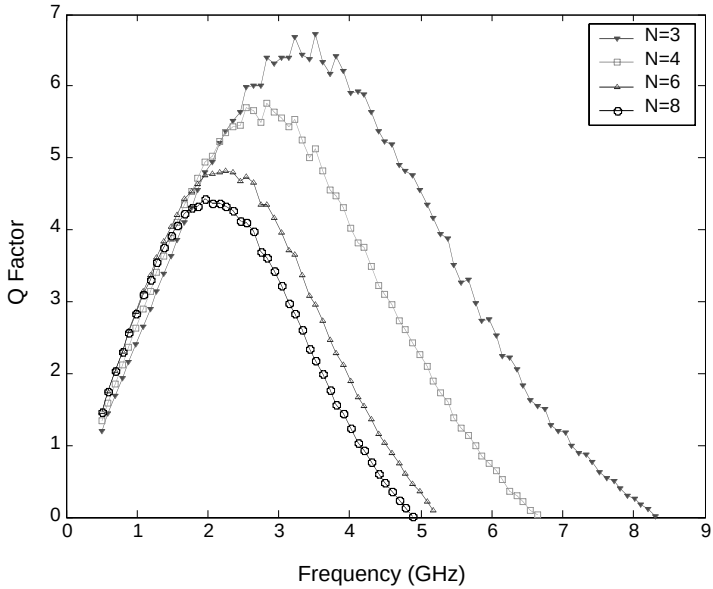

Figure 14. Q-factor as a function of frequency for inductors with different N.

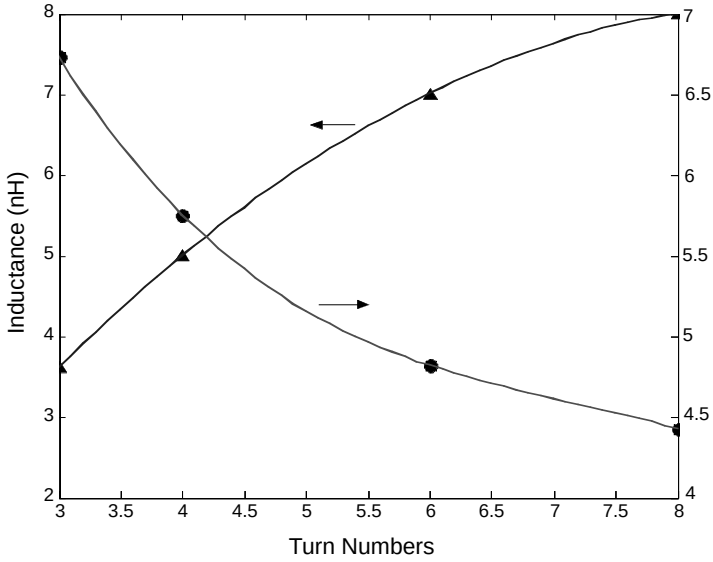

Figure 15. Inductances and $Q_{\max}$ as a function of N.

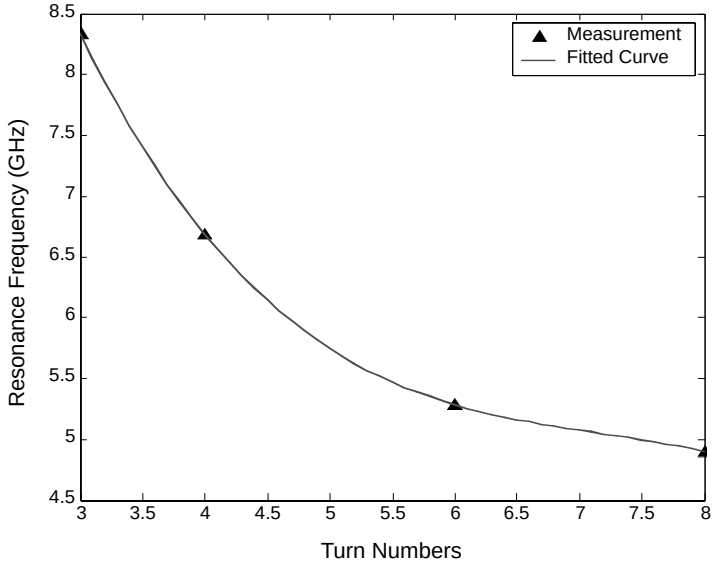

Figure 16. SRF as a function of N.

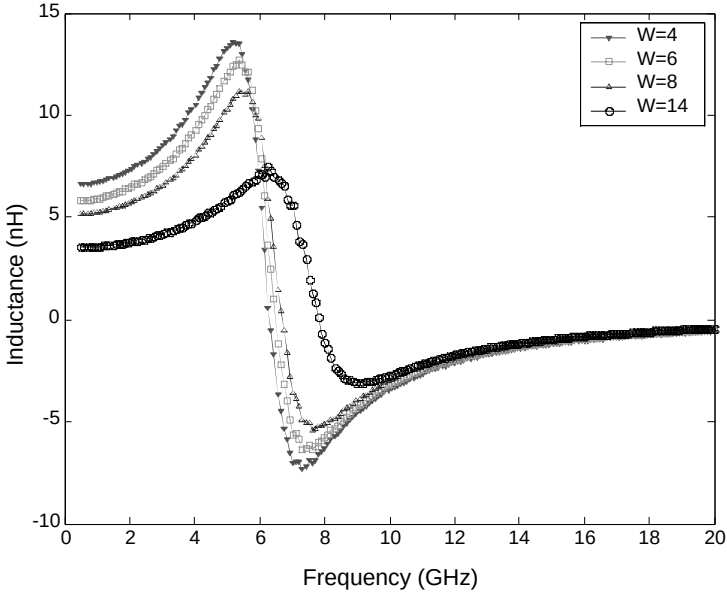

Figure 17. Inductance as a function of frequency for inductors with different W's.

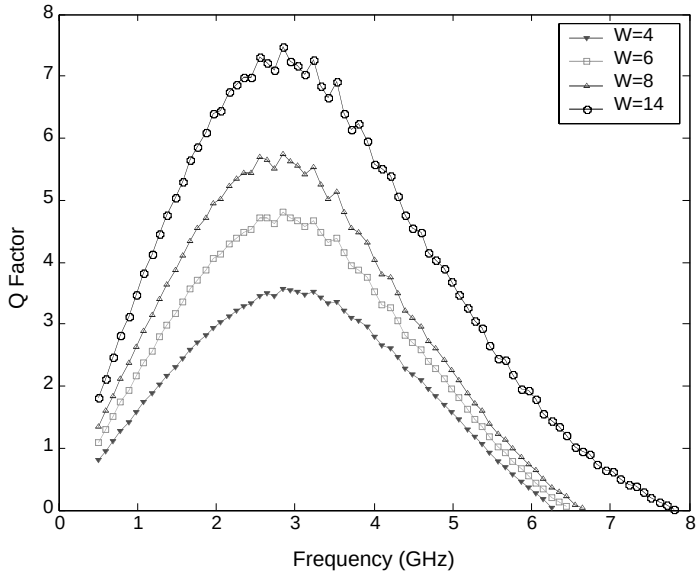

Figure 18. Q-factor as a function of frequency for inductors with different W's.

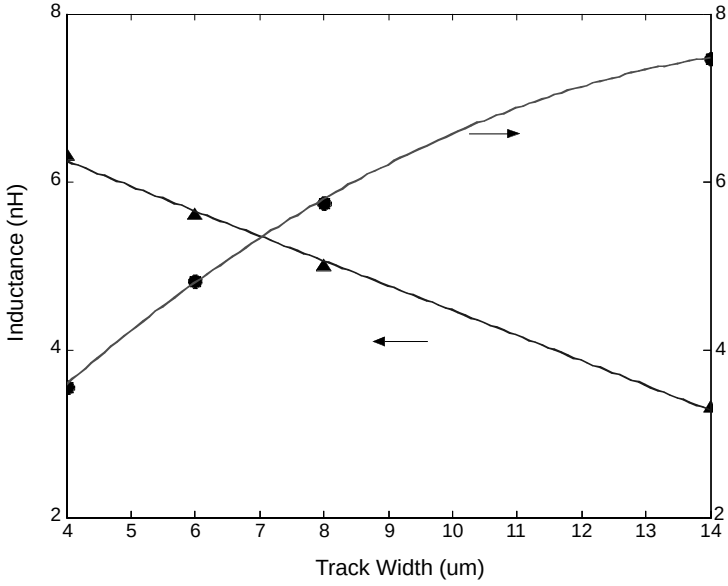

Figure 19. Inductances and $Q_{\max}$ as a function of W.

W in the whole measurement frequency range. Geometrically, when N, S, and D are all fixed, r must decrease accordingly to increase W. This decrease will cause the increase in negative mutual inductance coupling between the opposite metal tracks as the distance between them is decreased. As a result, the overall inductance will decrease. When W increases, the overall metal surface area will also increase, and in turn, the substrate capacitive coupling effects are enhanced. This is another reason that cause the overall inductance decrease. Fortunately, the increase in W will decrease the metal resistance. As a consequence, Q increases, correspondently.

Fig. 19 shows L value and Q-factor each as a function of W for those inductors in G2. It is obvious that L behaves as a decreasing linear function of W. When W is within the range from 4 to 14 μm, inductors with L ranging from 3.3 to 6.2 nH and $Q_{\max}$ from 3.8 to 7.7 can be designed for fixed $N = 4$, $S = 4\,\mu$m, and $D = 220\,\mu$m.

For inductors in group 3 (G3: Nos. 2, 8, 9, and 10), N, W and D are fixed at 4, 8 μm and 220 μm respectively, while S various from 1 μm to 6 μm ($S = 1$, 2, 4, and 6). Their L- and Q-factor-frequency curves are depicted in Figs. 21 and 22, respectively. It is seen that both L and Q-factor values decrease with S. This is easy to explain. When S increases, r decreases accordingly to maintain fixed N, W and D. This

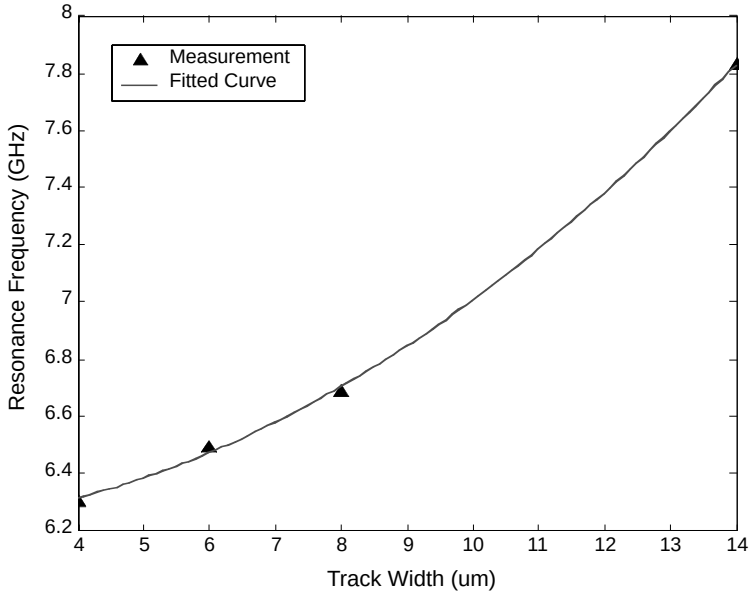

Figure 20. SRF as a function of W.

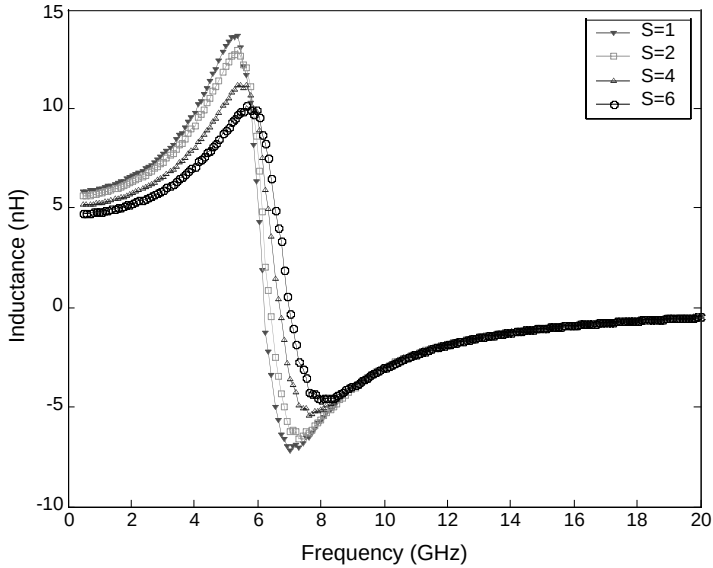

Figure 21. Inductance as a function of frequency for inductors with different S's.

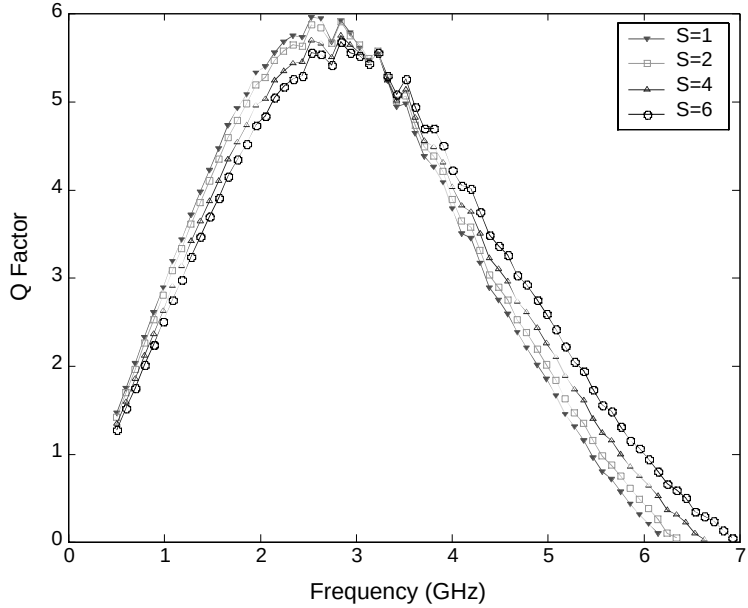

Figure 22. Q-factor as a function of frequency for inductors with different S's.

will cause a decrease in the overall L. Meanwhile, the increase in S also results in the decrease in the positive mutual inductance coupling between adjacent metal tracks and thus accounting for a slight decrease in overall L. The capacitive effect changes slightly in this case while the overall L decreases to some degree. As a result, the net energy stored in magnetic field decreases, causing the decrease in Q-factor.

Fig. 20 shows SRF as a function of W for inductors in G2, where SRF has a slight increase with increasing W. This is probably because when W increases, L decreases accordingly. Meanwhile, the parasitic capacitance increases. As the decrease in L dominates, the overall effect causes a slight increase in SRF.

The relationships between S and L, $Q_{\max}$ are plotted in Fig. 23. Both L and $Q_{\max}$ can be approximated as a linear decreasing function of S, and these results are valid for S varying from $1\,\mu$m to $6\,\mu$m.

From Fig. 24, it is seen that SRF can be approximated by a linear increasing function of S. This is due to the decrease in L while the capacitive effects maintain a relatively constant value.

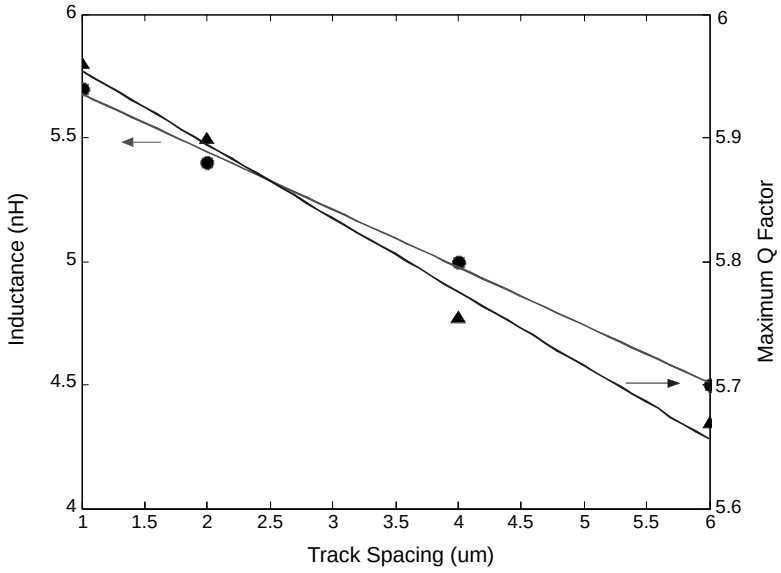

Figure 23. Inductances and $Q_{\max}$ as a function of S.

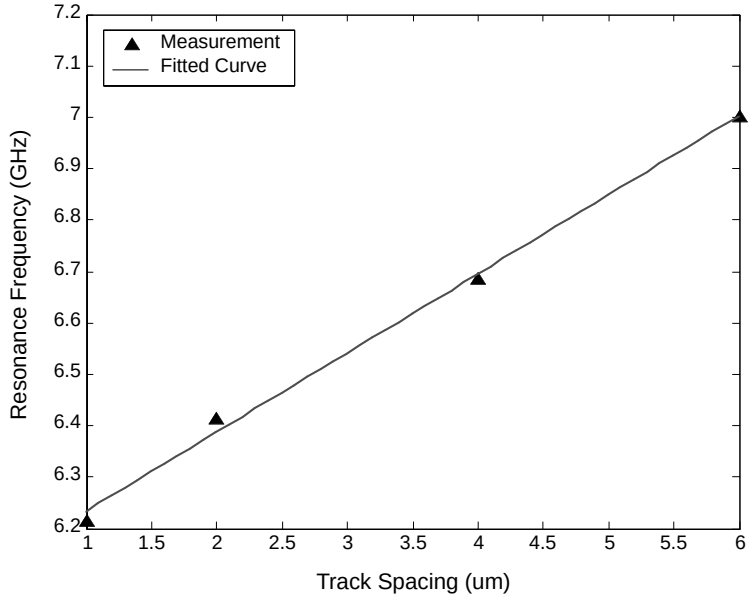

Figure 24. Self-resonant frequency as a function of S.

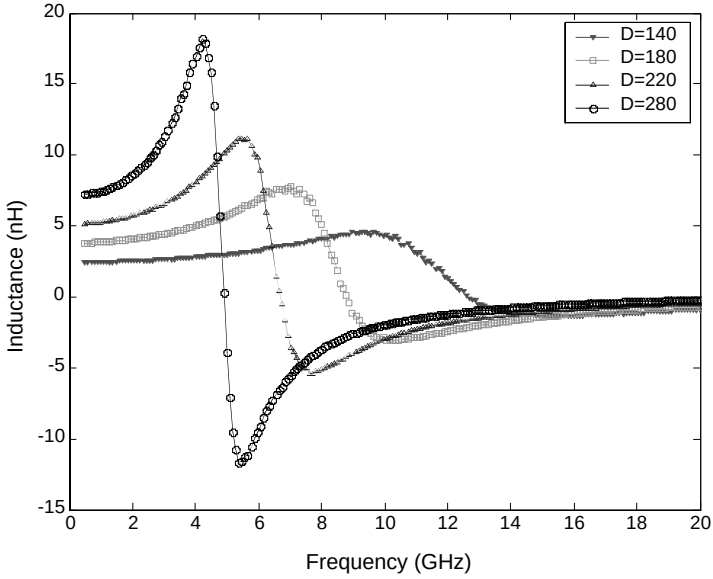

Figure 25. Inductance as a function of frequency for inductors with different D's.

3.3. Variation in both Inner- and Outer-Dimensions of the Spiral Inductors

These inductors are fabricated with fixed $N = 4$, $W = 8\,\mu$m and $S = 4\,\mu$m. The D value is $140\,\mu$m, $180\,\mu$m, $220\,\mu$m, or $280\,\mu$m, respectively (as shown in Table 1, Nos. 11, 12, 2 and 13). Figs. 25 and 26 show L and Q-factor as a function of operating frequency. It is clear that the changing trends for both L and Q-factor versus D are similar with those versus N. The likely reason is that r increases accordingly with D to keep fixed N, W, and S. As a result, the overall L increases due to the decrease in the negative mutual inductance coupling and the increase in total spiral metal length. As D increases, the overall chip area occupied by the inductor also increases accordingly. Therefore, the capacitive coupling and the substrate loss will increase. At low frequencies, the increase in L dominates. Thus, Q-factors for inductors with larger D have a larger value than that of those with smaller D. With frequency increasing, the parasitic effects for the inductors with larger D would come earlier and become dominant. This causes the decrease in Q-factor. That is the reason that both $Q_{\max}$ and Q-factors above $Q_{\max}$ for inductors with smaller D are larger than that of those with larger D.

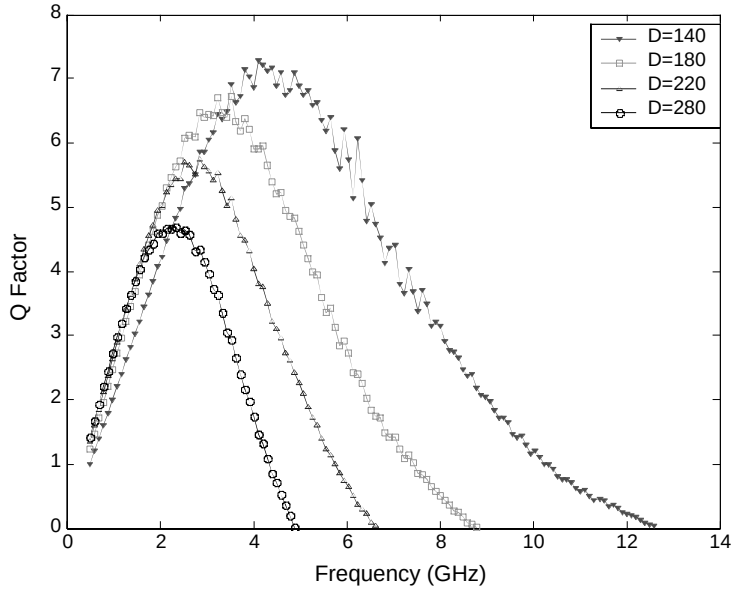

Figure 26. Q-factor as a function of frequency for inductors with different D's.

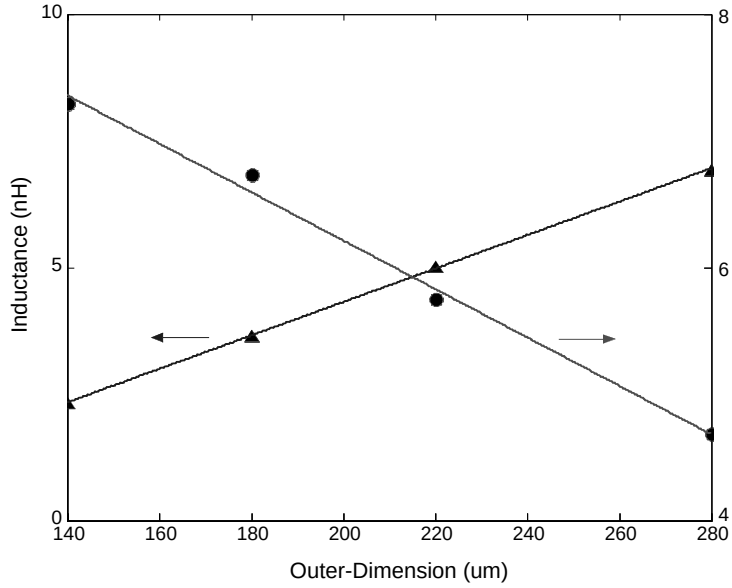

Figure 27. Inductances and Maximum Q-factors as a function of D.

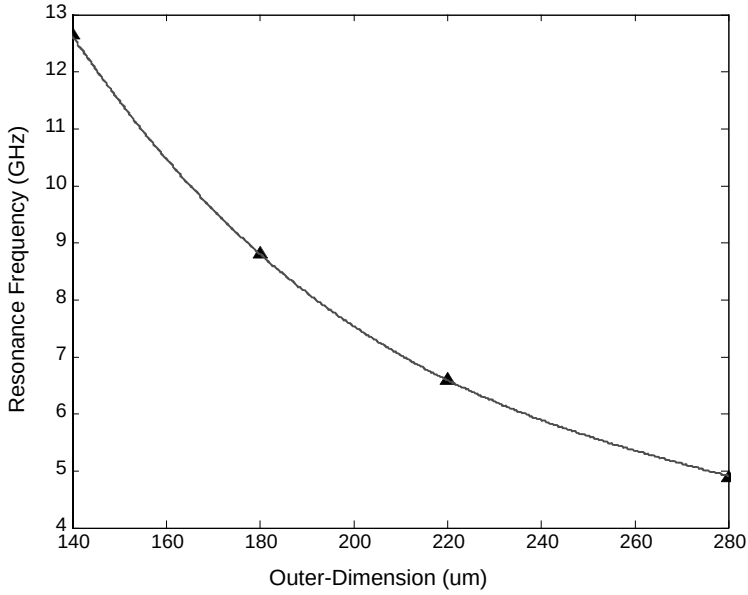

Figure 28. SRF as a function of D.

Fig. 27 shows both L and Q-factor as a function of D. In Fig. 27, L increases and $Q_{\max}$ decreases both linearly with D. These results are valid for D ranging from $140\,\mu$m to $280\,\mu$m with fixed $N = 4$, $W = 8\,\mu$m and $S = 4\,\mu$m. In addition, we can conclude from Fig. 27 that if a compromise is to be reached in these cases, then $D = 220\,\mu$m should be the most proper value for a spiral inductor, which will result in an approximate inductance value of 5 nH and a $Q_{\max}$ of 6.

Finally, Fig. 28 shows SRF versus D. Its trend is very similar to that of SRF versus N. The reason is that in both cases, the decrease in SRF is mainly due to the simultaneous increase in inductance and capacitance.

4. CONCLUSIONS

For inductors with fixed inner-dimension r, the performance trends that change with varying one or more geometrical parameters are summarized as follows: (a) increasing track width can increase inductance but cause a decrease in $Q_{\max}$ and SRF; (b) by increasing track spacing, both increased $Q_{\max}$ and L can be obtained, but SRF will decrease; (c) $Q_{\max}$ and SRF are decreasing functions of turn

numbers, while L is an increasing function of turn numbers; (d) increasing the thickness of the dielectric separation between the spiral and the substrate can also result in a higher $Q_{\max}$ and SRF, but this method has little influence on L; and (e) by using multi-layer metals, we can get a higher L at the cost of a lower $Q_{\max}$ and SRF.

For inductors with fixed outer-dimension or with simultaneously varied inner- and outer-dimensions, the performance trends that change with geometrical parameters are summarized as follows: (a) when maintaining a fixed outer-dimension, increasing track width results in a higher $Q_{\max}$ and SRF, but a decreased L; (b) with a fixed outer-dimension, both $Q_{\max}$ and L are a decreasing function of track spacing, while SRF increases with track spacing; (c) both $Q_{\max}$ and SRF are the decreasing functions of turn numbers, while L is an increasing function of turn numbers, and (d) when increasing both the inner- and outer-dimensions, e.g., increasing the area occupied by the inductor, we can get a higher L but $Q_{\max}$ degrades and SRF is also lowered. These performance trends for integrated spiral inductors, together with those presented in [1], can be used as a guideline in practical designs. However, as L, Q and SRF for a specified inductor vary as a function of frequency, we must have a trade off among these characteristics at the intended operation frequency range. For example, at low frequencies, loss is mainly due to the series ohmic metal loss, thus wider track width, thicker and higher conductivity metal should be used to get a larger $Q_{\max}$. While at high frequencies, Q-factor will be dominated by substrate loss, therefore, narrower track width or smaller outer-dimension would be better to minimize the occupied chip area, thus minimize substrate loss. In this situation, a higher resistivity substrate or a thicker oxide isolation layer between the spiral and the substrate will be also preferred to get a higher Q-factor. At low frequencies, minimizing available track spacing is preferred to maximize the magnetic coupling, but at high frequencies, proximity effects and magnetic coupling favor a larger value of track spacing [8]. Therefore, optimal geometrical and parametric parameters for a spiral inductor must be known for a specified application. And these parameters can be obtained through optimization under the guide of the performance trends presented in our papers.

REFERENCES

1. Ashby, K. B., I. A. Koullias, W. C. Finley, J. J. Bastek, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 1, 4–9, Jan. 1996.

2. Nam, C. M. and Y. S. Kwon, "High-performance planar inductor on thick oxidized porous silicon (OPS) substrate," *IEEE Microwave and Guided Wave Lett.*, Vol. 7, No. 8, 236–238, Aug. 1997.
3. Chang, J. Y. C., A. A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2 μm CMOS RF amplifier," *IEEE Electron Device Letters*, Vol. 14, No. 5, 246–248, May 1993.
4. Park, M., S. Lee, H. K. Yu, J. G. Koo, and K. S. Nam, "High Q CMOS-compatible microwave inductors using double-metal interconnection silicon technology," *IEEE Microwave and Guided Wave Lett.*, Vol. 7, No. 2, 45–47, Feb. 1997.
5. Zolfaghari, A., A. Chan, and B. Razavi, "Stacked inductors and transformers in CMOS technology," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 4, 620–628, Apr. 2001.
6. Danesh, M. and J. R. Long, "Differentially driven symmetric microstrip inductors," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 50, No. 1 , 332–341, Jan. 2002
7. Kenneth, O., "Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 8, 1249–1252, Aug. 1998.
8. Niknejad, A. M. and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF Ics," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 10, 1470–1481, Oct. 1998.
9. Koutsoyannopoulos, Y. K. and Y. Papananos, "Systematic analysis and modeling of integrated inductors and transformers in RF IC design," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 47, No. 8, 699–713, Aug. 2000.
10. Yue, C. P., C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, "A physical model for planar spiral inductors on silicon," *Proceedings of International Electron Devices Meeting*, 155–158, 1996.
11. Groves, R., K. Stein, D. Harame, and D. Jadus, "Temperature dependence of Q in spiral inductors fabricated in a silicon-germanium/BiCMOS technology," *Proceedings of Bipolar/BiCMOS Circuits and Technology Meeting*, 153–156, 1996.
12. Post, J. E., "Optimizing the design of spiral inductors on silicon," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 47, No. 1, 15–17, Jan. 2000.
13. Yin, W. Y., S. J. Pan, and L. W. Li, "Comparative characteristics

studies on on-chip single and double-level square inductors," *IEEE Trans. Magnetics*, Vol. 39, No. 3, 1778–1783, Apr. 2003.

14. Yin, W. Y., S. J. Pan, L. W. Li, Y. B. Gan, B. L. Ooi, and F. J. Lin, "Local scalable description of global characteristics of various on-chip asymmetrically octagonal inductors," *IEEE Trans. Magnetics*, Vol. 39, No. 4, 2042–2048, July 2003.
15. Pan, S. J., L. W. Li, and W. Y. Yin, "A compact lumped-element equivalent circuit model of two-layer integrated spiral inductors," *Internatfonal Journal of RF and Microwave Computer-Aided Engineering*, Vol. 13, No. 2, 148–153, 2003.
16. Pan, S. J., L. W. Li, and W. Y. Yin, "Electrical characteristics and behavioral model for spiral inductors on GaAs substrate," *Journal of Electromagnetic Waves and Application*, Vol. 16, No. 4, 443–455, 2002.
17. Yin, W. Y., S. J. Pan, L. W. Li, and Y. B. Gan, "Model description and parameter extraction of on-chip spiral inductors for MMIC's," *International Journal of RF and Microwave Computer-Aided Engineering*, acccpted for publication, Sep. 2003.
18. Yin, W. Y., S. J. Pan, and L. W. Li, "Experimental characeerization of on-chip octagonal double-helix inductors on silicon substrates," *IEE Proc-Microw. Antennas Propag.*, Vol. 150, No. 4, 265–268, 2003.
19. Yin, W. Y., S. J. Pan, L. W. Li, and Y. B. Gan, "Experimental characterization of coupling effects between two neighboring on-chip spiral inductors," *IEEE Trans. Electromagnetic Compatibility*, Vol. 45, No. 3, 557–561, 2003.

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