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A 2.3-mW 16.7-MHz ANALOG MATCHED FILTER CIRCUIT FOR DS-CDMA WIRELESS APPLICATIONS

M. A. R. Eltokhy

Electronics Technology Department
Faculty of Industrial Education
Helwan University
Egypt

H. A. K. Mansour

Electrical Department
Faculty of Engineering
Banha University
Egypt

Abstract—The matched filter (MF) is known as the fastest method for acquisition of DS-CDMA signals. Power consumption of the MF is a key issue for realizing multimedia hand-held terminals. We proposed a new Analog Matched Filter using Sample-and-Hold (S/H) circuit, which performs correlation between an input signal and a filtering coefficient employed for modulation in fully analog domain, eliminating the need to Analog-to-digital (A/D) conversion, so reduces power consumption and chip area. Simulation results reveal that the proposed circuit dissipates 2.3 mW power consumption at a chip rate of 16.7 MHz with 3.3 V power supply for 15 taps configuration. The proposed analog architecture could improve the performance of mobile terminals.

1. INTRODUCTION

For the Direct Sequence Code Division Multiple Access (DS-CDMA) system of spread spectrum communications used in the most recent cellular phones, it is important to acquire initial synchronization with transmitter soon after starting operation, and to track it at low power consumption [1, 2]. The Matched Filter is one of the devices that perform such a function. Many types of Matched Filters are studied for

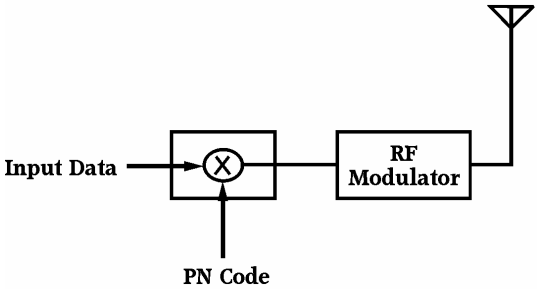

Figure 1. DS-CDMA system transmitter.

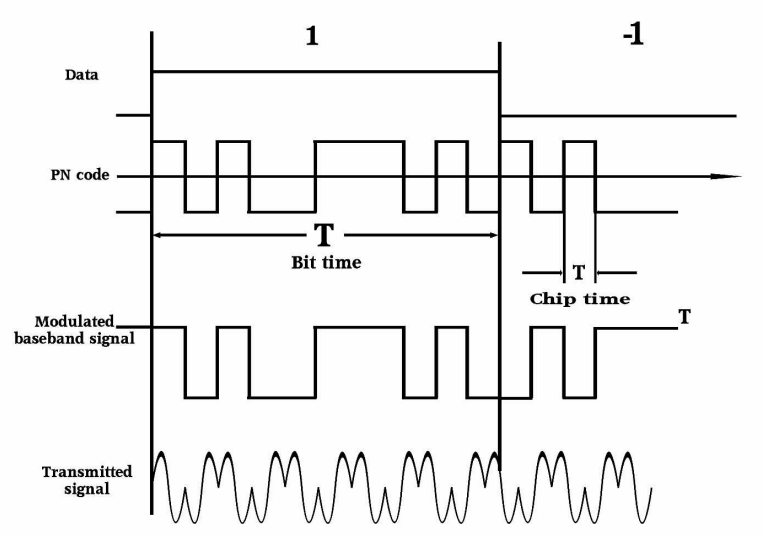

Figure 2. DS-spread spectrum modulation.

spread spectrum demodulation operating at high frequencies and/or low power consumption [3–5].

The DS-CDMA transmission section is illustrated in Fig. 1 and the signal, actually broadcast from transmitter, is shown in Fig. 2. Transmitted signal is modulated by Pseudorandom Noise (PN) code sequence with Phase Shift Keying (PSK). In order to demodulate a transmitted signal and to decode the original data correctly, a Matched Filter can be used to calculate the correlation function between a received signal and the PN code. The fundamental operation of this

Matched Filter is described by:

$$y(n) = \sum_{i=1}^{N} a_i x(n-i) \tag{1}$$

where $x(n)$ is input signal, $y(n)$ is correlation output, n is the number of taps usually 16 and 128, and a_i is the PN code. a_i is generally $a_i \in \{-1, +1\}$, which represents Binary PSK(BPSK) demodulation. Equation (1) shows that the correlation peaks when received signal is synchronized with PN code at the receiver. Using this correlation peak, the receiver acquires and tracks synchronization from which information signal is detected and decoded.

Among various methods available to perform function of Equation (1), digital-based operation is used in many cases. We proposed a new Analog Matched Filter using Sample-and-Hold (S/H) circuits. The circuit performs correlation operation in fully analog domain, eliminating the need to Analog-to-Digital conversions, so reduces power consumption and chip area.

2. FUNDAMENTAL ARCHITECTURE

2.1. Digital Matched Filter

A conventional structure of Digital Matched Filter is shown in Fig. 3. This type of Matched Filter first performs conversion of the received analog signal into digital data with a high-performance high-speed A/D converter [6–8]. Then it forwards the digital data to registers one by one in accordance with every PN code chip time. The total correlation value is computed by summing up the products between digital data held in registers, D_n, and PN code set in the other registers, a_n.

One of the major issues in the Digital Matched Filter is the fact that it requires a high-performance A/D converter, to reduce bit error rate. Thus, power consumption and chip area is increased.

2.2. Analog Matched Filter

In contrast to the conventional Digital Matched Filter, we proposed a new processing scheme as shown in Fig. 4. A received signal is processed as analog value and the data shift register is made up of S/H circuits. An appropriate analog circuit is used for operation part. The proposed structure requires only one signal line without A/D converter. Thus, chip area becomes small and the power consumption is reduced.

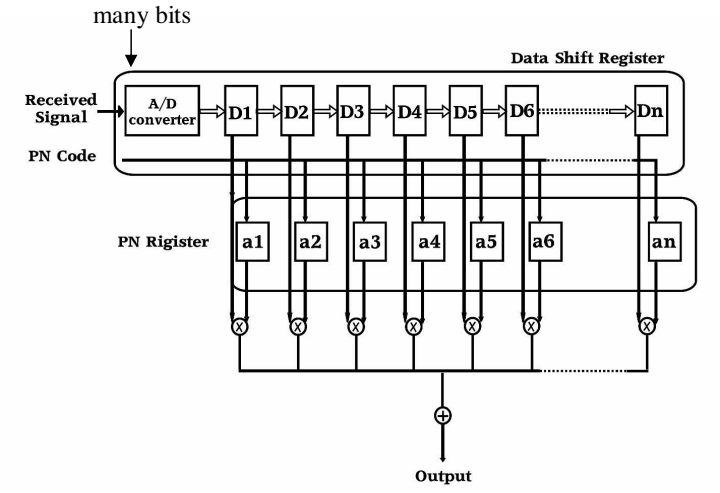

Figure 3. Conventional digital matched filter.

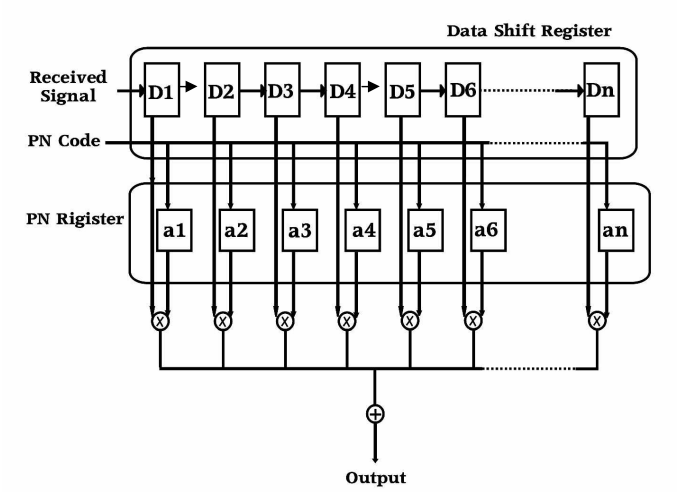

Figure 4. Proposed analog matched filter.

3. PROPOSED CIRCUIT DESIGN

Main part of an actual circuit and timing diagram are shown in Fig. 5 and Fig. 6, respectively.

In Fig. 5, the input signal applied to V_{IN} is forwarded one by one to the following stages by S/H circuits synchronizing with the clock.

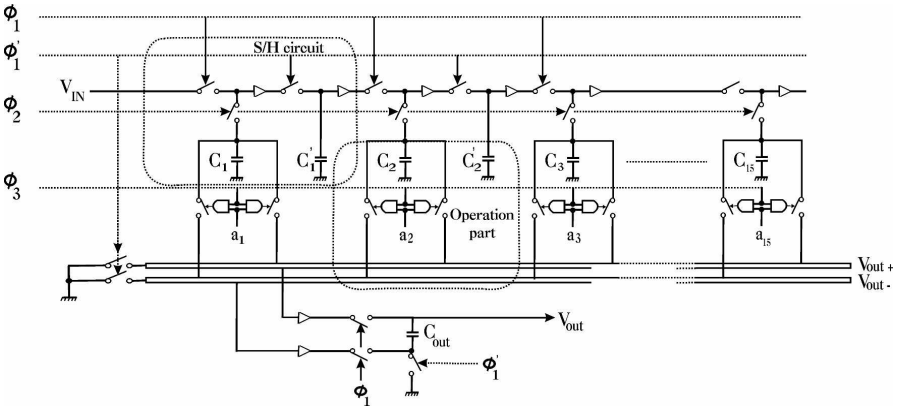

Figure 5. Operation circuit for proposed analog matched filter.

Past n chip values of the received signal are stored as charges in the hold capacitors of the S/H circuits.

The stored charges at hold capacitors are summed up separately according to the sign of the PN codes with turning on switches Φ_3. The resulting positively and negatively weighted charges are given at the V_{OUT+} node and V_{OUT-} node, respectively. Equation (2) is obtained from the charge conservation properly, assuming the initial charge of each capacitor is set to zero [4]. One can show that Equation (1) and Equation (2) are equivalent:

$$V_{OUT}(n) = \sum_{i=1}^{N} \frac{C_i}{C_{TATAL}} V_{IN}(n-i) \tag{2}$$

This equation says that the weight of each stage can be controlled with the capacitance of S/H circuits. Since the weights are either $+1$ or -1 in spread spectrum communications, all the capacitors can be designed to have the same capacitance value; $a_n = 1$ for the weight $+1$; and a_n=0 for -1.

The circuit performs Equation (2) so correlation value is output to V_{OUT} for every chip timing. Operation principle of the proposed circuit is shown in Fig. 7, and described as follows:

(1) The capacitor C_1 charged up to an input signal voltage V_{IN}. The charged stored in the hold capacitor C'_{n-1} is sampled and transferred into the capacitor C_n of the next stage, for data shifting.

(2) The charge stored in C_n is sampled and held by C'_n for preserving signal from the following destructive operation.

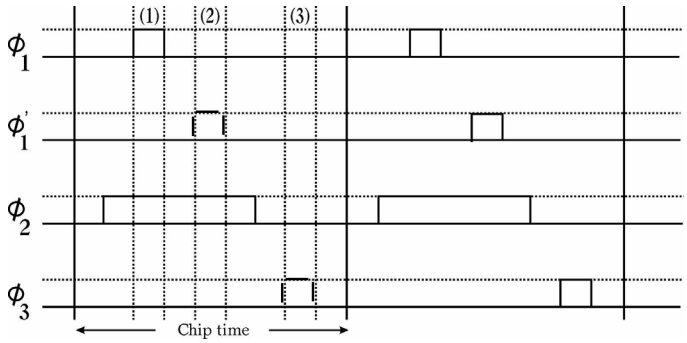

Figure 6. Switching sequence for the operation circuit.

(3) The charge stored in C_n is read out and put into either V_{OUT+} or V_{OUT-} nodes according to the sign of a_n ; V_{OUT+} for a_n=1; V_{OUT-} for a_n=0.

Correlation values are provided as V_{OUT}, after previous steps. The hold capacitor is used not only for the holding signal but also for the summing operation.

4. DESIGN CONSIDERATIONS

4.1. Parasitic Effect

The behaviour of the circuit read out V_{OUT+}, V_{OUT-} can be explained by taking into account the parasitic capacitance of the circuit. Fig. 8 depicts the equivalent circuit when parasitic capacitance is taken into account. The value of the parasitic capacitance varies depending on how the capacitor is implemented [9]. C_{jp} is introduced to model the depletion capacitance of poly silicon. As voltage coefficient of capacitors is approximately 20–200 ppmV^{-1}, the effect of C_{jp} negligible small. Top plate parasitic capacitance due to interconnect at capacitor is usually small, i.e., at the order of 1/100 of C_n. However, capacitance at the node of top plate, which is caused by junction capacitance of switching circuit, is relatively large i.e., about 20%–30% of C_n and has high voltage coefficient.

The nonlinearity of the source and drain junction capacitances associated with the transistor switches, which are voltage dependence as follow,

$$C_P = \frac{C_{P_0}}{\sqrt{1 + \frac{V_P}{\phi_0}}} \tag{3}$$

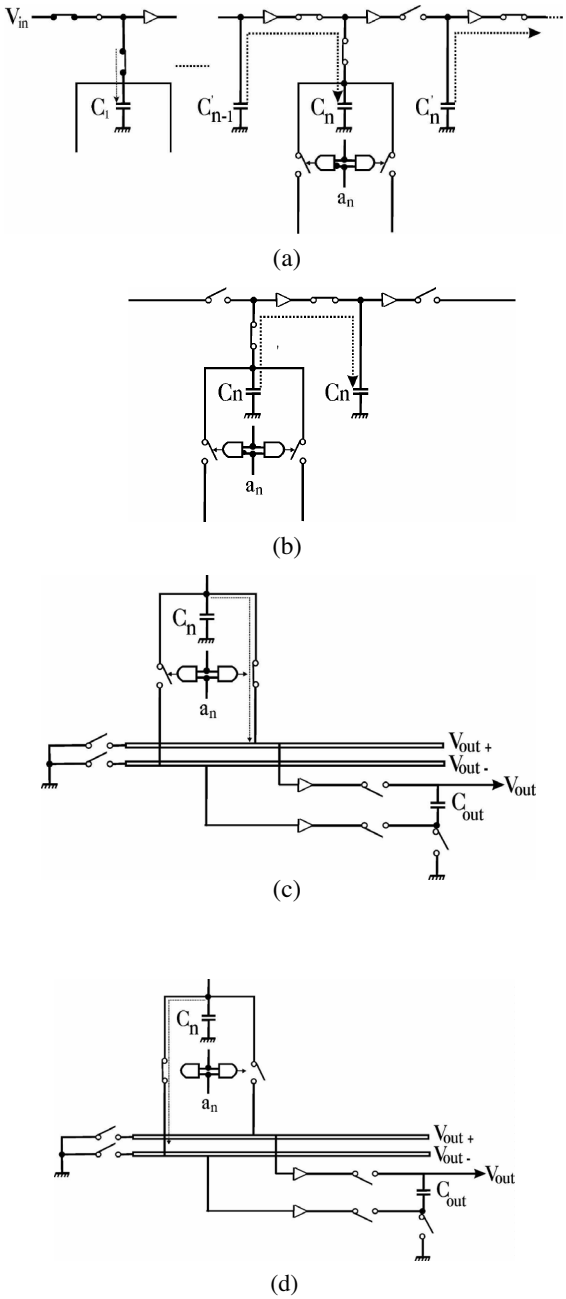

Figure 7. Principle of operation, (a) Interval (1), (b) Interval (2), (c) Interval (3) ($a_n = 1$), (d) Interval (3) ($a_n = 0$).

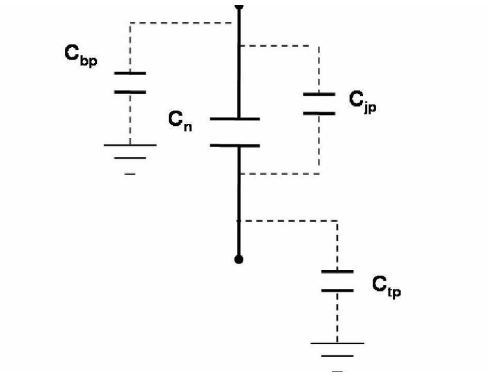

Figure 8. Sampling capacitor with parasitic capacitance shown. Parasitic capacitance exists at both to and bottom plate. Voltage dependence is also modelled with V_{jp}.

where C_{P0} is the depletion at $V_P = 0$. These capacitances can introduce errors in the sampling process that generate an extra noise component to the correlation process [10–12]. To minimize this effect, the sampling capacitor can be increased and/or the switch sizes decreased. Doing either of these increases the settling time constant ($\tau = R_{switch} \times [C_n + C_n']$), where R_{switch} is the on-resistance of the holding mode switch so there is a trade off between operating bandwidth and nonlinearity error. The switch sizes (W/L) and sampling capacitor (C_n) values are chosen to keep the charge injection error of switches (0.3 μV) are negligible small.

4.2. Noise

The CMOS analog matched filter using S/H circuit has one noise source [13]. This source is the noise power of a single sample due to sampling the thermal noise of the input switches which is given as

$$N_{thermal} = \frac{kT}{C_n} \tag{4}$$

where $k =$ Boltzman's constant and T is temperature in Kelvin. This noise voltage of 0.2 mV is very small compared to the other signals' code noise.

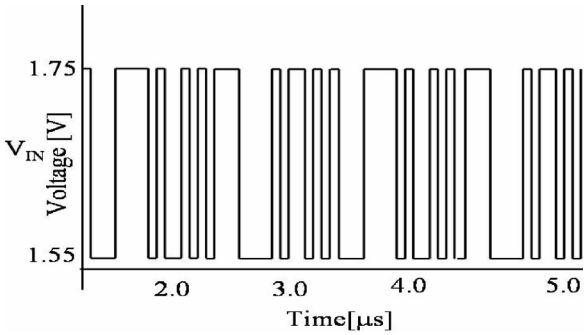

Figure 9. Input waveform.

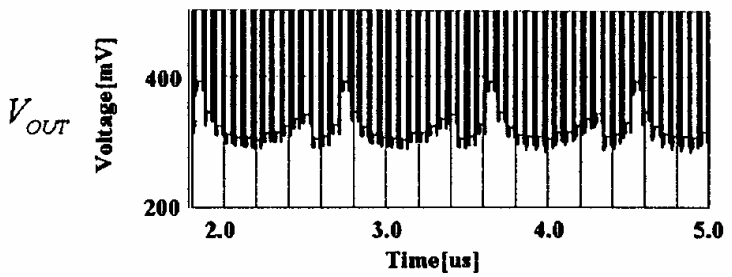

Figure 10. Output waveform.

5. SIMULATION RESULTS

HSPICE simulation proposed circuit was performed utilizing a 2poly, 3metal, 0.35 μm, CMOS process. In the simulations cascade op-amp was used for a high frequency characteristic, and a high voltage gain. The size of each capacitance was set up to 0.2 pF. With the input signal shown in Fig. 9, we can expect output has a peak when input signal and PN code are synchronized. Fig. 10 shows that a peak value is obtained every 15 chips of output signal that the proposed circuit performs the desired Matched Filter operation. Simulation example of correlation peak from analog matched during acquisition is shown in Fig. 11. The code sequence of interest is tested at each bit position along the data pattern. When every bit of the code sequence corresponds to the data pattern a perfect match occurs and a correlation peak is obtained. From the simulation example, when the desired (pre-selected) waveform is present in the data that are input to matched filter, the matched filter compress most of the energy of that waveform into a small slot of time, allowing signal detection.

We summarized the simulation result in Table 1. The Analog

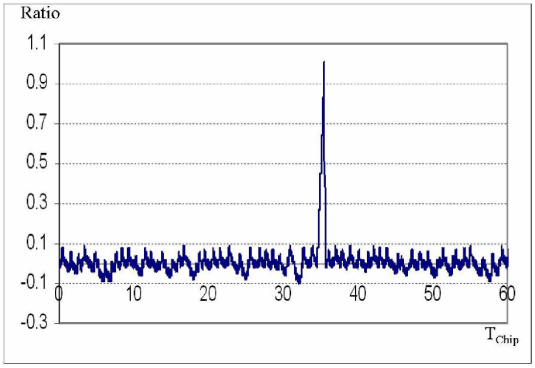

Figure 11. Example of correlation peak of analog matched filter.

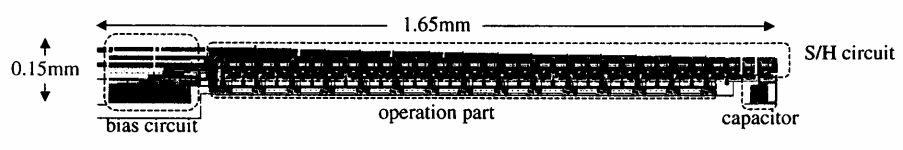

Figure 12. Analog matched filter layout.

Matched Filter circuit would achieve 2.3 mW power consumption at a chip rate of 16.7 MHz with 3.3 V power supply for 15 taps configuration.

Layout of the circuit is in Fig. 5 with 15 taps configuration, is shown in Fig. 12. the chip area was 0.25 mm^2.

Comparison with proposed Analog Matched Filter with other work is shown in Table 2. The values in the parentheses are calculated assuming the same number of taps, the same frequency, and the same power supply voltage. Accordingly to this simulation, the proposed circuit achieves a small area and low power consumption relatively. Power consumption could be reduced further with a careful optimization of cascade amplifiers.

Table 1. Simulation results.

Power supply voltage	3.3 V
PN code	Maximum length codes
The number of taps	15
Chip rate	16.7 MHz
Power consumption	2.3 mW

Table 2. Comparison with other reported matched filter circuits.

	Core area	Power	Power supply voltage	Techn -ology
Digital Architecture [5]	41.85 mm^2, 64 Tap (0.109 mm^2/Tap)	4 mW@2 MHz (0.21 μW/MHz·Tap·V^2)	5.0 V	1.2 μm
Analog Architecture [3]	85 mm^2, 128 Tap (0.664 mm^2/Tap)	225 mW@20 MHz (9.77 μW/MHz·Tap·V^2)	3.0 V	0.8 μm
Proposed Analog Matched Filter	0.25 mm^2, 15 Tap (0.017 mm^2/Tap)	2.3 mW@16.7 MHz (0.82 μW/MHz·Tap·V^2)	3.3 V	0.35 μm

6. CONCLUSION

We proposed a new Analog Matched Filter using S/H circuit. The circuit performs correlation operation in fully analog domain, eliminating A/D conversion, so reduces power consumption and chip area.

HSPICE simulation proposed circuit was performed utilizing a 2poly, 3metal, 0.35 μm, CMOS process. The simulation result shows that the proposed Analog Matched Filter would achieve 2.3 mW power consumption at chip rate of 16.7 MHz with 3.3 V power supply for 15 taps configuration. The layout of the circuit has been made with 15 taps configuration. The chip area was 0.25 mm^2. The proposed circuit achieves a small area and low power consumption relatively.

REFERENCES

1. Pickholtz, R. L., D. L. Schilling, and L. B. Milstein, "Theory of spread-spectrum communications — A tutorial," *IEEE Transaction on Communications*, Vol. 30, No. 5, 855–884, May 1982.
2. Lee, W. C., "Overview of celluler CDMA," *IEEE Transaction Vehicular Technology*, Vol. 40, No. 2, 291–302, May 1991.
3. Chen, J., G. Shou, and C. Zhou, "High-speed low-power matched filter for W-CDMA: Algorithm and VLSI-architecture," *IEICE Trans. Fundamentals*, Vol. E83-A, No. 1, 75–81, January 2000.
4. Figueroa, M., D. Hsu, and C. Diorio, "A mixed-signal approach

to high-performance low-power linear filters," *IEEE J. Solid State Circuits*, Vol. 36, No. 5, 264–270, May 2001.

5. Onodera, K. K. and P. R. Gray, "A 75-mW 128-MHz DS-CDMA base-band demodulator for high-speed wireless applications," *IEEE J. Solid State Circuits*, Vol. 33, No. 5, 753–761, May 1998.
6. Baier, A., "A low cost digital matched filter for arabitrary constant-envelope spread-spectrum wave-forms," *IEEE Transaction on Communications*, Vol. 32, 354–361, April 1984.
7. Kataoka, N., T. Kojima, M. Miyake, and T. Fujino, "Performance of soft decision digitqal matched filter in direct-sequence spread-spectrum communication systems," *IEICE Transaction*, Vol. E74, 1115–1122, May 1991.
8. Wu, J., M. Liou, H. Ma, and T. Chiueh, "A 2.6 V, 44-MHz all digital QPSK digital-sequence spread spectrum transceiver IC," *IEEE J. Solid-state Circuit*, Vol. 32, 1499–1510, October 1997.
9. Slater, D. and J. Paulos, "Low volatge coefficient capacitors for VLSI processes," *IEEE J. Solid State Circuits*, Vol. 33, No. 5, 753–761, May 1998.
10. Sheu, B. and C. Hu, "Switched-induced error voltage on a switched capacitor," *IEEE J. Solid State Circuits*, Vol. SC-19, No. 4, 519–525, 1984.
11. Wegmann, G., E. Vittoz, and F. Rahali, "Charge injection in analog MOS switches," *IEEE J. Solid State Circuits*, Vol. SC-22, No. 6, 1091–1097, 1987.
12. Shyu, J. B., G. C. Temes, and F. Krummenacher, "Random errors effects in matched MOS capacitors and current sources," *IEEE J. Solid State Circuits*, Vol. SC-19, 948–955, 1984.
13. Yoon, Y. C. and H. Leib, "Matched filtering in improper complex noise and applications to DS-CDMA," *Conference Recordings PIMRC'95*, 701–705, Toronto, Canada, Sept. 27–29, 1995.