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DESIGN OF L-BAND HIGH SPEED PULSED POWER AMPLIFIER USING LDMOS FET

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Abstract—In this paper, we design and fabricate the L-band high speed pulsed HPA using LDMOS FET. And we propose the high voltage and high speed switching circuit for LDMOS FET. The pulsed HPA using LDMOS FET is simpler than using GaAs FET because it has a high gain, high output power and single voltage supply. LDMOS FET is suitable for pulsed HPA using switching method because it has 2 $\sim$ 3 times higher maximum drain-source voltage (65 V) than operating drain-source voltage (Vds = 26 $\sim$ 28 V). As results of test, the output peak power is 100 W at 1.2 GHz, the rise/fall time of output RF pulse are 28.1 ns/26.6 ns at 2 us pulse width with 40 kHz PRF, respectively.

1. INTRODUCTION

The high power RF pulse is utilized in many applications including medical electronics, laser excitation and radars, etc. The most applicable application of RF high power pulse signal is using in radar systems. But the research of high speed RF high power pulse signal is not many compared to others [1–11]. Solid state power device is not higher output power and operating frequency, but wider bandwidth and higher reliability than vacuum tube [12]. Recently, solid-state power devices which have the output power up to hundreds W at S-band have been developed [13]. Moreover, we can obtain several kW output power by combining some devices. The pulsed power amplifier can be realized by using a modulation or a switching method.

Figure 1(a) shows the pulsed power amplifier which amplifies pulse modulated RF signal by a pulse modulator at input port. This method needs a pulse modulator and a wideband amplifier for fast switching time. Fig. 1(b) shows the pulsed amplifier which generates RF pulse

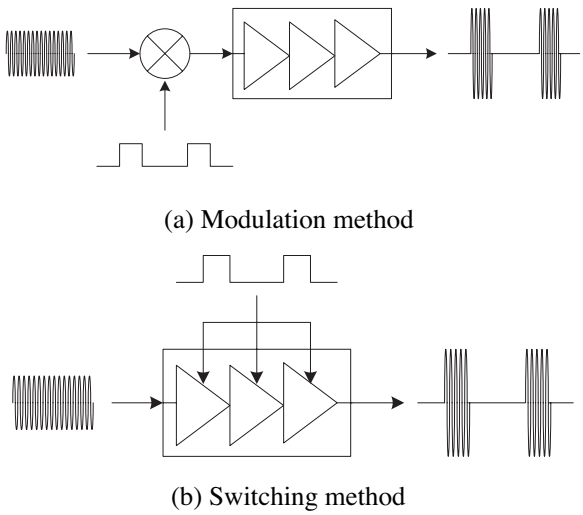


Figure 1. Pulsed power amplifier structure.

by switching the supply voltage of amplifier. This amplifier has a high efficiency and low noise floor level because of supplying bias voltage only for high level of pulse. The rise/fall time of pulsed power amplifier depends on the performance of switching circuit. But the conventional switching circuit has slower fall time than rise time and has the low driving voltage less than 20 V. In this paper, the novel switching circuit for improving the fall time and increasing the driving voltage is proposed. To conform a validity of the proposed switching circuit, we design and fabricate the LDMOS FET pulsed power amplifier which has output power of 100 W at 1.2 GHz.

2. HIGH SPEED AND HIGH VOLTAGE SWITCHING CIRCUIT

Figure 2 shows the conventional switching circuit. The output port of this circuit will be connected to a power amplifier. The operating current of switching circuit is controlled by R_Load. Q4 is p-channel power MOSFET for switching the supply voltage of power amplifier according to the input pulse. Q1 $\sim$ Q3 is a drive circuit for fast switching of Q4 by using input TTL level (5 V/0 V). It is based on a CMOS inverter circuit [14]. The rise/fall time of FET depends on charge/discharge time of the gate source capacitance (Cgs) according to the gate source voltage (Vgs). The operating current of a drive circuit is controlled by R1. The small R1 has a fast switching speed,

and then the current consumption is increased. Q4 must be selected by considering power handling capacity and drain source resistance [Rds(on)] for "on" state.

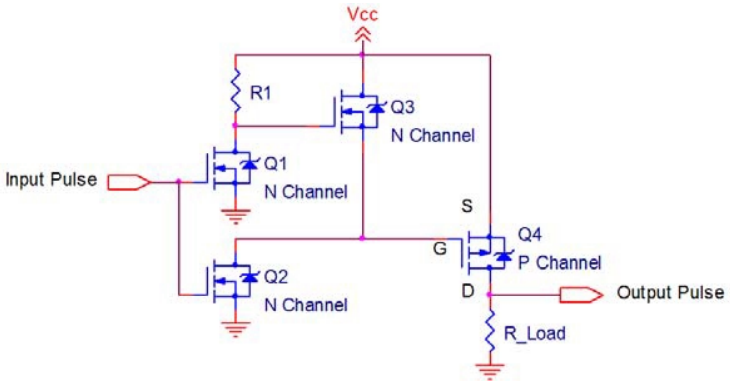


Figure 2. Conventional switching circuit.

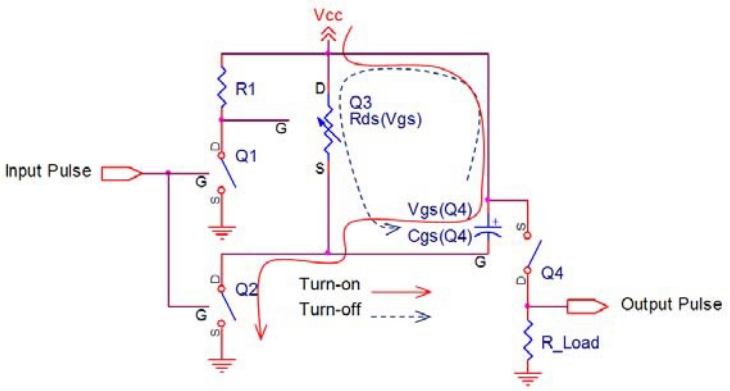


Figure 3. Operation of switching circuit.

Figure 3 shows the current flow for "on" and "off" state of the switching circuit. The Cgs(Q4) is charged along the solid current line if the switching circuit is turned on. In this case, the approximate time constant can be written as

$$\tau\_\text{charge} = \text{Rds(on, Q2)} \cdot \text{Cgs(Q4)} \tag{1}$$

where Rds(on, Q2) is "on" state drain source resistance of Q2 and Cgs(Q4) is the gate source capacitance of Q4. The time constant is very small because Rds(on, Q2) is less than several ohms. When the

switching circuit is turned off, Cgs(Q4) is discharged along the dotted line. Assuming that Q3 is the voltage controlled(Vgs) variable resistor, the approximate time constant can be written as

$$\tau\_\text{discharge} = \text{Rds(Q3)} \cdot \text{Cgs(Q4)} \tag{2}$$

where Rds(Q3) is the voltage(Vgs) controlled variable resistance of Q3. The moment the switching circuit is turned off, Rds(Q3) becomes the same as Rds(on, Q3) because Q3 is turned on by voltage difference between the Vgs(Q4) charged at Cgs(Q4) to the extent of -Vcc and the gate voltage(Vg) of Q3. The more Cgs(Q4) is discharged, the smaller Vgs of Q3 gets. Then, the discharge speed of Cgs(Q4) is getting slower because of increasing the Rds(Q3). If we can make maintaining of the Vgs(Q3) above threshold voltage while Q4 is turned off, the fall time of switching circuit can be improved because Cgs(Q4) is discharged enough before Rds(Q3) increases.

In this paper, two methods for improving the fall time are suggested. Fig. 4(a) shows the switching circuit to reduce Rds(Q3) using double supply voltages. If we supply higher voltage of drive circuit(Q1 $\sim$ Q3) than Q4's, Vgs(Q3) is increased due to the increase of Vg(Q3) resulting in the decrease of Rds(Q3). However, this method requires the extra circuit for double supply voltage. If we decrease input threshold voltage of Q3, we can increase Vgs(Q3) using single supply voltage. Because the threshold voltage of BJT with 0.6 V is smaller than FET's, the FET in Fig. 2 is replaced with BJT to decrease the input threshold voltage of Q3 as shown in Fig. 4(b). The fall time of switching circuit in Fig. 3(b) is reduced because of maintaining low Rds(Q3) while Cgs (Q4) is discharged.

But this circuit cannot be used in amplifiers with supply voltage more than 20 V because the maximum gate to source voltage(Vgs) of Q4 is $\pm$20 V. In this paper, the driving voltage of the switching circuit is increased by using a Zener diode(D1). Fig. 5 shows the high voltage switching circuit with fast fall time. The function of the Zener diode(D1) is to protect Q4. While the switching circuit is turned on, Q2 is also turned on and anode of Zener diode is shorted to ground. The gate voltage of Q4 maintains with the breakdown voltage of Zener diode. If we choose a proper Zener diode, we can control Vgs(Q4) in case of high supply voltage more than 20 V.

In this case, breakdown voltage of Zener diode can be chosen like below range

$$|\text{Vgs(th) of Q4}| < |\text{V}_{\text{BR,Zener}} - \text{Vcc}| < |\text{Maximu Vgs of Q4}| \tag{3}$$

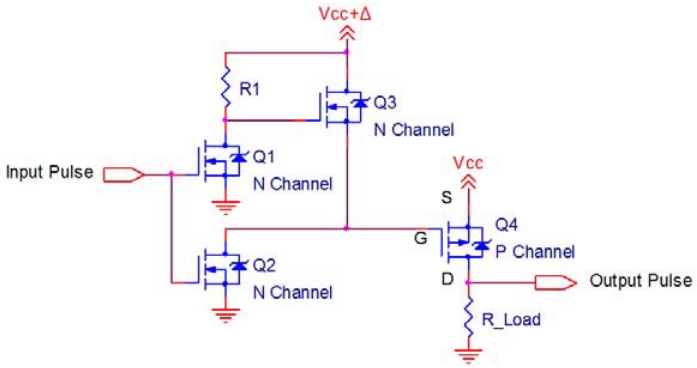
where Vgs(th) is the threshold voltage between gate and source and $\text{V}_{\text{BR,Zener}}$ is breakdown voltage of Zener diode.

3. DESIGN OF PULSED HIGH POWER AMPLIFIER

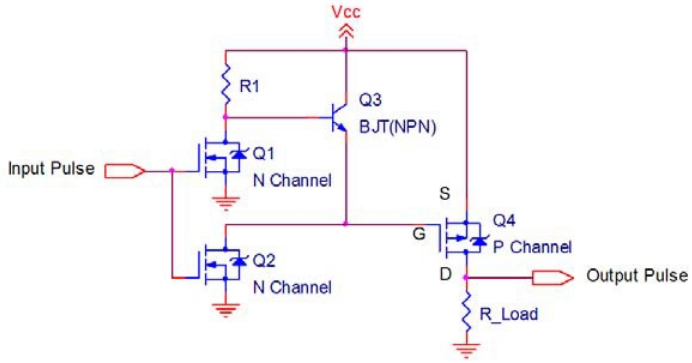
The specifications of the pulsed high power amplifier for L-band radar are summarized in Table 1.

Recently, LDMOS FET has been used in L-band high power amplifiers. It has the advantages of simple bias circuit and high maximum rating of bias voltage. So it is suitable for a pulsed high power amplifier using switching method. Fig. 6 shows a cascaded amplifier configuration to achieve the output power of 100 W at 1.2 GHz.

The devices of final stage are composed by combining two MRF9085 of Freescale® which output power has 90 W at 880 MHz. The second stage is MRF9030 of Freescale® which output power has 30 W at 945 MHz. The maximum peak power of MRF9030 is lower



(a) Double supply voltage



(b) Single supply voltage

Figure 4. Proposed high speed switching circuit.

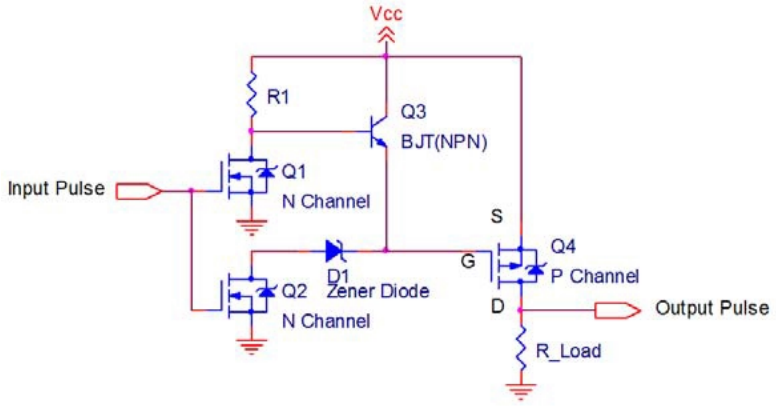


Figure 5. Proposed high speed and high voltage switching circuit.

Table 1. Specifications of THE pulsed high power amplifier.

Parameters	Specifications
Frequency	1215 ∼ 1260 MHz
RF Peak Power	100 W
Pulse Repetition Frequency	40 kHz
Pulse width	2 us, 4 us
Pulse duty	Less than 20%
Rise/fall time of RF pulse	Less than 100 ns
Supply Voltage	28 V

than maximum input power rating of final stage. The first stage of AH102 is a gain block.

To obtain a high speed RF pulse, we consider the rise/fall time of a switching device. The Q1 ∼ Q2 are IRLML2803 of International Rectifier®, Q3 is MMBT2222 of Onsemi®, Q4 is RFP30P05 of Intersil® and breakdown voltage of Zener diode is 13 V. We simulate the rise/fall time of the switching circuit by Cadence® PSPICE® simulator. Each spice model of the switching device is given by vendors. The simulated rise/fall time of each switching circuit is summarized in Table 2. We can know that the fall time of the proposed switching circuit (Q3: BJT) is faster than the conventional circuit (Q3: FET).

To minimize the switching delay time, the switching circuit is positioned close to the amplifier. And energy storage capacitance for

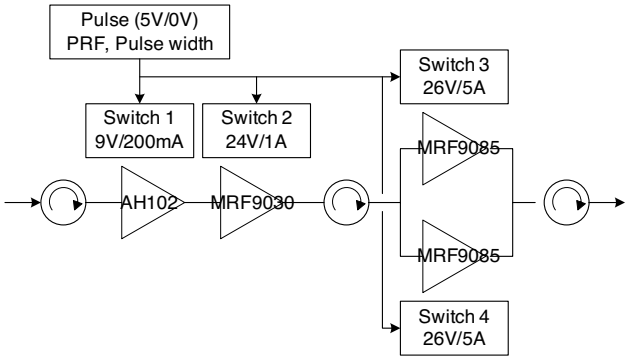


Figure 6. Configuration of pulsed power amplifier.

Table 2. Simulated rise/fall time of each switching circuit.

	MRF9030 (1 A/24 V)		MRF9085 (5 A/26 V)	
Time (ns)	Rise	Fall	Rise	Fall
Q3: FET	19.4	75.5	19.9	46.1
Q3: BJT	17.5	66.6	18.5	34.7
Improvement	+1.9	+8.9	+1.4	+11.4

pulsed power amplifier [1] is written as

$$C = \frac{I \times dt}{dV} \tag{4}$$

where I is the peak current, dt is the pulse length and dV is the pulse voltage droop. When drain voltage is changed about 0.4 V, output power of MRF9085 is reduced to 0.1 dB in simulation. To keep 0.1 dB pulse droop, storage capacitance is 62.5 us at 5 us pulse width and peak current 5 A. We use a capacitor more than 100 uF. Not to be degraded switching time, this capacitor is placed at source of p-channel power MOFET, Q4 in Fig. 5.

We can calculate switching noise by using (5) and (6), when we using switching circuit.

$$\textit{Maximum frequency of switching noise} = \frac{1}{\textit{Minimum pulse width} \times 2} \tag{5}$$

$$= \frac{\begin{array}{c}\textit{Minimum frequency of switching noise}\\ 1\end{array}}{(PRI - \textit{Minimum pulse width}) \times 2} \quad (6)$$

Where PRI is pulse repetition interval (= 1/PRF). These switching noises can be transferred from drain to gate by gate-drain capacitance of LDMOSFET. They can change gate bias voltage level. So we have to remove switching noise at gate by using bypass capacitor. In our specification, maximum frequency of noise is 250 kHz, minimum is 21.7 kHz. Because this switching noise has rectangular waveform, we also consider harmonics.

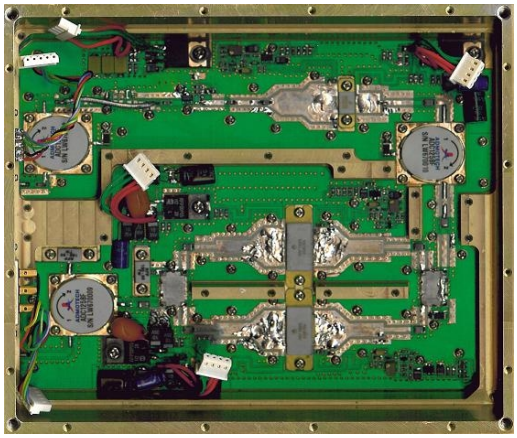
4. FABRICATION AND TEST RESULTS

To reduce the noise generated by the switching circuit, the pulsed power amplifier is fabricated by using a two layer substrate. The 1st layer is the board of amplifier and the 2nd layer is the board of switching circuits. The fabricated pulsed amplifier is shown in Fig. 7.

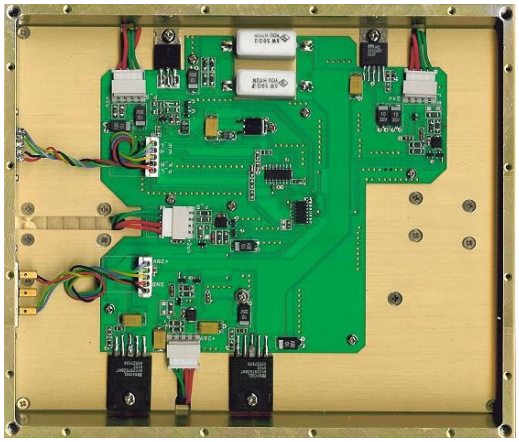
Table 3. Measured rise/fall time of each switching circuit.

	MRF9030 (1 A/24 V)		MRF9085 (5 A/26 V)	
Time (ns)	Rise	Fall	Rise	Fall
Q3: FET (conventional)	18.1	53.9	29.6	53.0
Q3: BJT (proposed)	26.2	32.9	36.3	24.9
Improvement	−8.1	+21.0	−6.7	+28.1

The measured rise/fall times of each switching circuit using R_Load are summarized in Table 3. At this time, R_Load for MRF9030 and MRF9085 is 24 Ohm and 4.7 Ohm, respectively. Compared with MRF9085, MRF9030 has much difference between the simulated and measured result. But the trends of the simulated results are similar to the test results. We think that SPICE model given by vendor is suitable for high current condition. In case of RFP30P05, we can compare simulated results to its data sheet. It is summarized in Table 4. Simulated results are very reasonable in case of high current condition like Table 4s conditions. But the less current condition, the more difference of simulations and measurements happens. From Table



(a) RF HPA layer



(b) Switching circuit layer

Figure 7. Pulsed high power amplifier (Size: $190 \times 160 \times 50$ mm).

3, we can find that the fall time of the proposed switching circuit is faster than the conventional circuit.

Table 5 is the measured rise/fall time of the pulsed high power amplifier which includes the multi-stage RF amplifiers and the switching circuits. We can know that the fall time of the pulsed high power amplifier using the proposed switching circuit is faster than the using the conventional switching circuit.

As shown in Table 4, the fall time of output pulse of pulsed high power amplifier using the proposed switching circuit is 13.7 ns faster

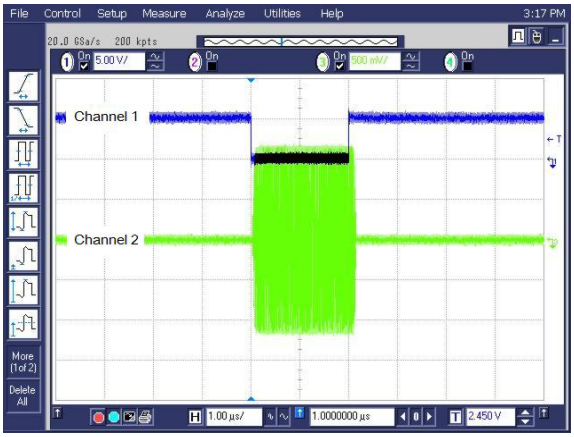
(a) Rise time

(b) Fall time

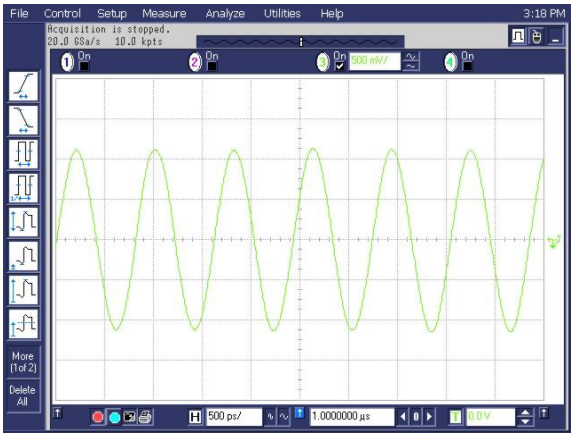
Figure 8. The output pulse of pulsed high power amplifier.

Table 4. Verification of RFP30P05.

	RFP30P05 Conditions: $V_{DD} = -25\,\text{V}$, $V_{GS} = -10\,\text{V}$ $I_D = 15\,\text{A}$, $R_G = 6.25\,\Omega$, $R_L = 1.67\,\Omega$	
	Simulated Results	Data Sheets
Rise Time(ns)	23 ns	22.5 ns
Fall Time (ns)	18 ns	18 ns



(a) 2us RF pulse waveform



(b) RF waveform in pulse

Figure 9. The output pulse waveform.

than that of using the conventional switching circuit. And the rise/fall time is almost independent according to the pulse width. The power consumption is 1.4 A/28 V at 2 us pulse width and 2.7 A/28 V at 4 us pulse width. And efficiency of the pulsed high power amplifier is about 20%.

Figure 8 shows the characteristics of 2 us RF pulse measured by the oscilloscope (54854A, Agilent Technologies). In Fig. 6, channel 1 is the input pulse and channel 2 is the output RF pulse of the pulsed high power amplifier. The delay between input and output is mainly

Table 5. Measured rise/fall time of THE pulsed high power amplifier.

Measured results of RF pulse, Pout = 100 W			
	Q3: FET (conventional)	Q3: BJT (proposed)	Improvement
	Pulsewidth = 2 us		
Rise Time (ns)	32.5	28.1	+4.4
Fall Time (ns)	40.3	26.6	+13.7
	Pulse width = 4 us		
Rise Time (ns)	32.4	28.8	+3.6
Fall Time (ns)	40.3	25.2	+15.1

caused by the inverter IC used for separating each switching circuit.

Figure 9 illustrates the 2 us RF pulse waveform and the distortionless CW waveform in the pulse.

5. CONCLUSIONS

We design a L-band high speed pulsed power amplifier using LDMOS FET. To design the pulsed power amplifier, we proposed the novel switching circuit with the fast fall time and the high switching voltage for a pulsed power amplifier. The proposed switching circuit is implemented by replacing FET of the conventional circuit with BJT and using Zener diode. Compared with a conventional switching circuit, the proposed circuit exhibits fall time reduction of more than 28.1 ns at 26 V/5 A output pulse. And the fall time of RF pulse using the proposed switching circuit is 13.7 ns faster than that of the conventional circuit. And the rise/fall time is almost independent the pulse width. As results of test, the output peak power is more than 100 W at 1.2 GHz, the rise/fall time of the output RF pulse is 28.1 ns/26.6 ns at 2 us pulse width with 40 kHz PRF and PAE is about 20% at 28 V. The proposed switching circuit seems to be applicable in the pulsed amplifier using all solid-state power device, such as LDMOS FET and GaN HEMT which is required a drain voltage more than 26 V.

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