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A GENERALIZED DESIGN PROCEDURE FOR A MICROWAVE AMPLIFIER: A TYPICAL APPLICATION EXAMPLE

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Abstract—In this work, a generalized procedure is carried out for the design of a microwave amplifier. First of all, the Performance Data Sheets (PDS) resulted from the active device characterization are used as Feasible Design Target Space (FDTS). Employing the PDS, the compatible (Noise F, Input VSWR V_i, Gain G_T) is determined over the predetermined bandwidth B between $f_{\min}$ and $f_{\max}$ operation frequencies with the source Z_S and load Z_L terminations as the design target. In the design stage, the Simplified Real Frequency Technique (SRFT) is utilized in the scattering-parameter formulation of the front- and back-end matching two-ports to provide the source and load terminations to the transistor, respectively. As an application example, a novel high technology transistor is chosen and the design targets are determined using the PDSs of the device and its front- and back-end matching two-ports are characterized by the scattering-parameters using the novel SRFT for each design target. Furthermore, the performances of the resulted amplifier circuits are analyzed and compared with the simulated results.

1. INTRODUCTION

As the electronic industry moves towards higher integration and lower cost, RF and wireless design demands increasingly more "concurrent engineering", thereby requiring IC designers to have sufficient knowledge of all related disciplines such as microwave theory, communication theory, IC design, wireless standards, multiple access, transceiver architectures, CAD tools. Due to the limited prime power, the low power and/or the low voltage, are among the main requirements for the very highly integrated low-noise amplifier

(LNA)s together with the 50 Ω noise match, a high gain along ultra-wide bandwidth (UWB). Recently, typical design works [1, 2] with SiGe heterojunction bipolar transistors are presented in the literature compatible with conventional low-cost Si CMOS [3] manufacturing for these requirements. Besides, an UWB design is presented in [4] employing LC ladder matching networks for a 3–10 GHz on-chip SiGe LNA amplifier.

Among the major problems observed in these types of studies is the lack of the "Feasible Design Target Space (FDTS)". In the other words, design process must be performed using the physical limits and/or compromise relations within the design hexagon consisting of bias voltage V_{DS}, bias current I_{DS}, noise F, gain G_T, input VSWR V_i, operation bandwidth B. This problem has not solved yet by the today's computer aided analysis and synthesis tools for RFICs, which are still in their infancy, forcing the designer to rely on experience, intuition or inefficient simulation techniques to predict the performance. It should also be noted that optimization process of the amplifier performance is highly nonlinear in terms of the descriptive parameters of the system. Certainly, within the optimization process, one can easily embed the desired performance goals without knowing the physical limits and/or compromise relations among noise (F), input VSWR (V_i) and gain (G_T) appropriately. Unfortunately this process often fails to attain the desired goals.

The physical limits and/or compromise relations within the design hexagon may be carried out in a systematic manner into the Performance Data Sheets (PDS) of the device and can be obtained in the following main stages as given in Fig. 1: (i) Firstly, a Soft-Model of the transistor which may be either Neural [5] or Support Vector model [6], is generated to determine the signal and noise behaviors within the whole operation domain of the device consisting of the configuration type (CT), the bias condition V_{DS}, I_{DS}, the operation frequency f; (ii) Secondly, noise, input VSWR, gain performance of the device is characterized point by point within the operation domain as given in the works [7, 8]; (iii) Finally, the Performance Data Sheets (PDS) can be obtained as resulted from the Gain-Bandwidth limitations [9] using the performance characterization of the active device.

Here it should be noted that the first stage of the work necessitates modeling of small-signal behavior of the transistor using nonlinear learning machines such as neural network or support vectors. In fact, nowadays these two typical nonlinear learning machines have found wide-range applications in the electromagnetic engineering. Typically, neural networks are applied to forming quasi-static modeling for

multilayer cylindrical coplanar lines [10], calculation of the impedance of air-suspended trapezoidal and rectangular shaped microshield lines [11], non uniform antenna array synthesis [12], design of the coplanar waveguides combining fuzzy systems [13], passive dipole arrays with together genetic algorithm [14]. On the other-hand, support vectors have become a strong competent method to the neural networks by the typical applications on the linear- [15] and non linear modeling [16] of mesfets; modeling of the microwave devices such as microstrip antenna based on the experimental data [17], mim capacitors [18].

The whole process is applied in a recent work [19] in details in the designof a LNA amplifier with together gradient-based method, where all the other pioneer works for the circuit-based stage are included and T-, Π-, L-types of the distributed-parameter matching networks are employed. Furthermore evolutionary algorithms such as genetic, very fast simulated reannealing and particle swarm algorithms are also utilized in [20–22] to optimize the distributed parameters of the T-, Π-, L-types of the matching networks subject to the PDS of the device.

In this work, the similar design procedure to the one in [19–22] is followed and worked out to put forward a general procedure for the design of a microwave amplifier with a different type of the modeling for the transistor terminations' data, as independent of the circuit topology. To the authors' knowledge, these are expected to contribute the following originalities into the literature: (1) The Feasible Design Target Space (FDTS) based upon the Gain-Bandwidth limitations of the employed active device [9] is used, thus the compatible (F, V_i, G_T) triplet is chosen to supply as the performance target with together its corresponding operation bandwidth B into the design process. This type of determination of the FDTS results in these advantages: (i) Input VSWR V_i is also introduced as a free variable into the design procedure; Furthermore, (ii) Stability of the device does not need to be considered as an additional target, since all the solution terminations take place within the Unconditionally Stable Working Area (USWA) of the device [7, 8]; (iii) Each component of the Compatible (F, V_i, G_T) triplet may also be chosen as a function of frequency, i.e., one of our choices is that $F_{req} = 0.46\,\mathrm{dB}$; $V_i = 1$ and $G_{T_{\max}}(f)$ which is the constrained maximum gain at each operation frequency along the operation bandwidth B as given in Fig. 6. Another frequency dependent choice may be in the form of $F_{req} = F_{\min}(f)$, $V_{i_{req}} = const.$, $G_{T_{\max}}(f)$, where $G_{T_{\max}}(f)$ is the maximum gain at each operation frequency constrained by the requirements of $F_{req} = F_{\min}(f)$ and $V_{i_{req}} = const.$ (2) The multi-objective design of the whole amplifier is finally simplified as modeling of the target Z_S, Z_L terminations' data of the required triplet for the transistor, as independent of the circuit

topology. A reflectance based real-frequency technique [23] is employed in the modeling using the L and C elements within the practical range. Furthermore, since the reference source and load impedances may be chosen as $50\,\Omega$, so there is no need for the diplexer to provide $50\,\Omega$ for source and/or load. So this will help to reduce the size for the miniaturization.

In the following sections, block diagram for the Performance Data Sheets in the Fig. 1 will be considered block by block in an order. In the later sections, the reflectance-based type of the data modeling for the terminations will briefly be given together with optimization algorithms and applications.

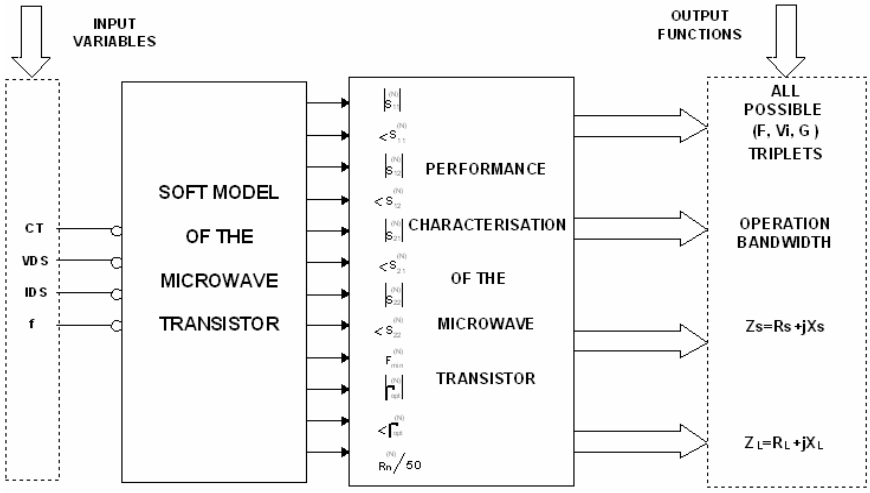


Figure 1. A block diagram for the performance data sheets.

2. PERFORMANCE DATA SHEETS OF A MICROWAVE TRANSISTOR

2.1. Potential Performance of a Microwave Transistor: Compatible (F, V_i, G_T) Triplets and (Z_S, Z_L) Terminations

A typical design problem of a basic microwave amplifier employing per se, a GaAs FET as an active device is given by Fig. 2.

Since in such a system, all the main performance components of F, V_i, G_T can be determined by the active device employed, so it has to be identified by all its possible (F, V_i, G_T) triplets and their (Z_S, Z_L) terminations of the active device.

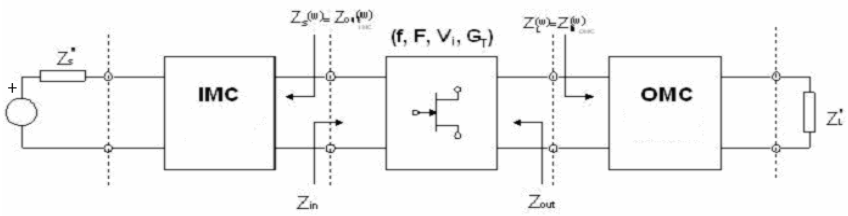


Figure 2. Microwave transistor with the matching circuits for the potential characteristics.

All the compatible (F, V_i, G_T) triplets are the simultaneous solutions of the following three nonlinear performance equations for the passive (Z_S, Z_L) terminations in the operation domain of the active device:

$$G_T = \frac{P_L}{P_{AVS}} = G\{R_S, X_S, R_L, X_L\} = \frac{4R_S R_L}{|(z_{11}+Z_S)(z_{22}+Z_L) - z_{12}z_{21}|^2} \quad (1)$$

$$F = \frac{(S/N)_i}{(S/N)_o} = F\{R_S, X_S\} = F_{\min} + \frac{R_N}{|Z_{opt}|^2}\frac{|Z_S - Z_{opt}|^2}{R_S} \quad (2)$$

$$\text{Input VSWR} = V_i = V_i\{R_S, X_S, R_L, X_L\} = \frac{1+|\rho_i|^2}{1-|\rho_i|^2}, \rho_i = \frac{Z_S - Z_i^*}{Z_S + Z_i^*} \quad (3)$$

The solution subsets $\{Z_S, Z_L/R_s > 0, R_L > 0\}$ in which we are interested, are the sets that ensure stable working of the transistor within its physical limitations, thus they have to satisfy the following inequities and/or equalities:

$$\text{Re}\{Z_i\} > 0, \ \text{Re}\{Z_o\} > 0 \quad (4)$$

$$G_{T_{\min}} \le G_T \le G_{T_{\max}}, \ V_i \ge 1, \ F \ge F_{\min} \quad (5)$$

where Z_i and Z_o are the input and output impedances of the active device two-port, respectively, which are in terms of $[z]$ parameters are,

$$Z_i = z_{11} - \frac{z_{12}z_{21}}{z_{22}+Z_L}, \quad Z_o = z_{22} - \frac{z_{12}z_{21}}{z_{11}+Z_S} \quad (6)$$

The problem of the gain limitations can be described as a mathematically constrained extremum problem, which is to find the extremum stable values of the function $G\{R_S, X_S, R_L, X_L\}$ in (1) subject to

$$\Phi_1 = F_{req} - F\{R_S, X_S\} = 0, \ \Phi_2 = V_{i_{req}} - V_i\{R_S, X_S, R_L, X_L\} = 0.$$

This constrained extremum problem and determination of the (Z_S, Z_L) terminations ensuring any G_T value between the $G_{T_{\min}} \leq G_T \leq G_{T_{\max}}$ are rigorously solved by the linear circuit and noise theory using impedance $[z]$ — or scattering $[S]$-parameter approach in [7, 8] respectively and employed to obtain the PDSs for the potential performance of the microwave transistor.

In the next subsection 'Performance Data Sheets' will be dealt to be used in the design of the front- and back-end matching circuits.

2.2. Performance Data Sheets

PDSs of a microwave transistor can be obtained from the block diagram given in Fig. 1 which consists of the two main parts: (i) The first part is "The Data-Based Soft" model of the device which needs some amount of data to be established. In this part, linear learning machines such as neural network [5], or support vector machine [6] can be employed; (ii) The second part is 'the Circuit Analyze-Based' model whose fundamentals are given in the previous subsection. So PDSs can be obtained from the interrelations among the physically realizable performance triplets and terminations over a defined operation bandwidth B, expressed as follows:

$$(F_{req}, V_{i_{req}}, G_{T_{\max}}) \Leftrightarrow \begin{array}{l} Z_{S_{\max}} = R_{S_{\max}} + jX_{S_{\max}}; \\ Z_{L_{\max}} = R_{L_{\max}} + jX_{L_{\max}} \end{array} \tag{7a}$$

$$(F_{req}, V_{i_{req}}, G_{T_{\min}}) \Leftrightarrow \begin{array}{l} Z_{S_{\min}} = R_{S_{\min}} + jX_{S_{\min}}; \\ Z_{L_{\min}} = R_{L_{\min}} + jX_{L_{\min}} \end{array} \tag{7b}$$

$$(F_{req}, V_{i_{req}}, G_{T_{req}}) \Leftrightarrow \begin{array}{l} Z_{S_{req}} = R_{S_{req}} + jX_{S_{req}}; \\ Z_{L_{req}} = R_{L_{req}} + jX_{L_{req}} \end{array} \tag{7c}$$

In the worked examples, PDSs of a high technology transistor is considered to obtain the design target space for the microwave amplifier circuits.

We can have the two alternative approaches in formation of the design target space from (7a), (7b) and (7c) to employ either (i) the compatible (F, V_i, G_T) triplets for the whole amplifier circuit or (ii) the Z_S and Z_L terminations for the input (IMC) and output (OMC) matching circuits respectively. The later will be emphasized in this paper. So the method to model the Bounded Real (BR) termination data will briefly be followed in the next section.

3. REFLECTANCE BASED REAL-FREQUENCY TECHNIQUE TO MODEL THE COMPUTED BR TERMINATION DATA

3.1. Scattering Parameter Characterization of the Matching Networks

In this work, the Reflectance Based Method is employed, whose essentials are based upon the simplified real frequency technique given in details [13], to build up the scattering parameters of the Darlington two-ports to match the given generator Γ_G and load Γ_r terminations to the required source Γ_S and load Γ_L terminations of the transistor, respectively, for the desired (F, V_i, G_T) triplets, as given in the Figs. 2–3. In our approach, the modeling problem can be defined as the generation of a realizable bounded real (BR) reflectance function which best fits the given data. Eventually, this BR reflectance is synthesized as a lossless and reciprocal "Darlington two-port" in resistive termination, yielding the desired circuit model. Obviously, the solution is not unique. The goal is, to end up with a reasonable BR reflectance function such that the resulting circuit can be built easily with least number of elements. In the course of the modeling, the termination data is examined and the corresponding BR reflectance forms are selected carefully.

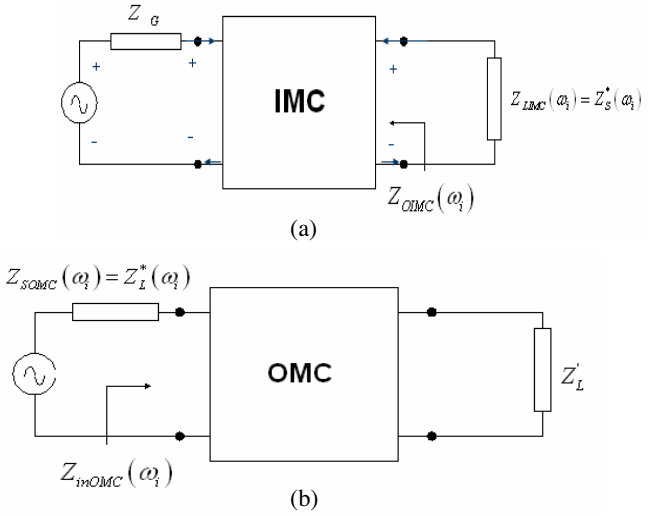


Figure 3. (a) Design of the front-end matching network. (b) Design of the back-end matching network.

Let $S(\omega_i) = S_R(\omega_i) + jS_X(\omega_i)$ or $S(\omega_i) = \rho(\omega_i)\, e^{j\phi(\omega_i)}$ be the given reflectance data such that $\rho(\omega_i) \leq 1$ over the sample frequencies ω_i defined throughout the operation bandwidth B. Let $\{S_{kl}; k, l = 1, 2\}$ designate the scattering parameters of the corresponding model which defines a lossless, reciprocal two-port, so called "Darlington two-port". For a lumped element, reciprocal, lossless two-port, the scattering parameters may be expressed in the Belevitch form as follows:

$$S_{11}(s) = \frac{h(s)}{g(s)}; S_{21}(s) = S_{12}(s) = \frac{f(s)}{g(s)}; S_{22}(s) = -\frac{f(-s)\, h(-s)}{f(s)\, g(s)} \tag{8a}$$

In (8a), $s = \sigma + j\omega$ designates conventional complex domain variable associated with lumped elements, $g(s)$ is an nth degree strictly Hurwitz polynomial with real coefficients such that

$$g(s) = g_n s^n + g_{n-1} s^{n-1} + \ldots + g_2 s^2 + g_1 s + g_0 \tag{8b}$$

Similarly, $h(s)$ is also an nth degree polynomial with free real coefficients h_i. That is,

$$h(s) = h_n s^n + h_{n-1} s^{n-1} + \ldots + h_2 s^2 + h_1 s + h_0 \tag{8c}$$

In (8a), $f(s)$ is a real polynomial which includes all the transmission zeros of the termination under consideration. Furthermore, the losslessness condition requires that $S(s)S(-s) = I$, which necessitates the following relation between the Belevitch polynomials:

$$g(s)g(-s) = h(s)h(-s) + f(s)f(-s) \tag{9a}$$

This also imposes the following degree relations:

$$\deg h \leq n, \deg f \leq n \text{ where } n = \deg g. \tag{9b}$$

Based on the above explanation, the termination reflectance data — $\Gamma_S(j\omega_i)$ or $\Gamma_L(j\omega_i)$ — must be equal to the input scattering coefficient $S_{1l}(j\omega_i)$ of the Darlington two-port to provide matching to the transistor. Losslessness condition of (9a) requires that $\rho_{21}^2(\omega_i) = 1 - \rho^2(\omega_i) \leq 1; \forall\omega_i$, where ρ is the magnitude of the $S_{ii}s$. So, once an appropriate form of $f(s)$ is selected, we can generate the full scattering parameters of the lossless and reciprocal Darlington two-port from the given numerator polynomial $h(s)$ according to the following theorem.

3.2. Main Theorem of the Reflectance — Based Modeling Problem

The scattering parameters $\{S_{kl}; k, l = 1, 2\}$ of a lumped element, reciprocal, lossless two-port can uniquely be determined from the

numerator polynomial $h(s) = h_n s^n + h_{n-1}s^{n-1} + \ldots + h_2 s^2 + h_1 s + h_0$ of the input reflection coefficient $S_{11}(s) = \frac{h(s)}{g(s)}$ for a preselected $f(s)$ such that

$$g(j\omega)g(-j\omega) = h(j\omega)h(-j\omega) + f(j\omega)f(-j\omega) \quad \forall\omega. \tag{10}$$

Proof: If $f(s)$ is preselected as stated by the theorem then, the even polynomial $G(s^2) = g(s)g(-s)$ can be constructed using (9a) in terms of $f(s)$ and $h(s)$ such that

$$G(s^2) = G_n s^{2n} + G_{n-1}s^{2(n-1)} + G_{n-2}s^{2(n-2)} + \ldots + G_1 s^2 + G_0 \tag{11}$$

Zeros of (11) can never be on the $j\omega$ axis since $g(j\omega)g(-j\omega) = h(j\omega)h(-j\omega) + f(j\omega)f(-j\omega)$ is never zero. Furthermore, these zeros present mirror image symmetry with respect to the imaginary axis $j\omega$. Hence, the strictly Hurwitz polynomial $g(s)$ is constructed on the left-half plane (LHP) zeros of (11). Thus, the scattering parameters of the lossless, reciprocal two-port are uniquely determined as in (8).

3.3. Synthesis Procedure

Based on the main theorem given above, in order to ensure the fitness of the unknown real coefficients $\{h_0, h_1, h_2, \ldots, h_{n-1}, h_n\}$ to the termination data, an objective function based on "Gain Performance" of the matching networks in Figs. 3(a) and 3(b) can be used:

$$\varepsilon = \sum_{j=1}^{N_\omega} (1 - G_T(\omega_j, h_i)), \quad i = 1, \ldots, n \tag{12}$$

where N_ω denotes the number of sampling frequencies over the operation bandwidth B and the gain $G_T(\omega_j, h_i)$ function can be expressed in terms of the impedance mismatching factor at either port of the reciprocal, lossless matching networks such as

$$G_T(\omega_j, h_i) = 1 - |\rho(\omega_j, h_i)|^2 \tag{13a}$$

and $\rho(\omega_j, h_i)$ can be given in terms of the termination data for input and output matching networks in the Figs. 3(a), 3(b), respectively, as follows:

$$\rho_{IMC} = \frac{Z_{outIMC}(\omega_j, h_i) - Z_{str}(\omega_j)}{Z_{outIMC}(\omega_j, h_i) + Z^*_{str}(\omega_j)} \tag{13b}$$

$$\rho_{OMC} = \frac{Z_{inOMC}(\omega_j, h_i) - Z_{Ltr}(\omega_j)}{Z_{inOMC}(\omega_j, h_i) + Z^*_{Ltr}(\omega_j)} \tag{13c}$$

where Z_{outIMC} and Z_{inOMC} have the well-known relations in terms of the scattering parameters of the related two-ports.

The Optimization Procedure used in this work can briefly be summarized as follows: (i) Choose a "Local Optimizer", i.e., "Nelder-Mead Simplex" or "Gradient-based Optimizer"; (ii) Start the design of the amplifier with the differential bandwidth $\Leftrightarrow$ narrowband from either the starting or stopping frequency of the operation bandwidth by initializing all the coefficients of the polynomial $h(s)$ as unities; (iii) Increase the bandwidth by passing to the next sample frequency at each step and taking the previous solution set as "the initial set" to the current design and continue this procedure till reaching to the end point of the operation bandwidth.

Thus the polynomials $h(s)$ and $g(s)$ are determined so that gains of the matching networks given the Figs. 3(a), 3(b) can be maximized, from (13b) and (13c) that ensure $Z_{outIMC} \cong Z_{Str}$, $Z_{inOMC} \cong Z_{Ltr}$ at each frequency along the operation bandwidth B. Then the bounded Scattering parameters are formed just described in (8) and the lossless and reciprocal matching circuits are synthesized using the Darlington procedure.

In the next section, the reflectance-based modeling procedure described in the above will be applied step by step to a chosen transistor NE329S01.

4. WORKED EXAMPLES

4.1. Design Target Space

NE329S01 is chosen as the transistor to design of its front- and back-end matching two-ports, whose minimum noise profile is given by Fig. 4.

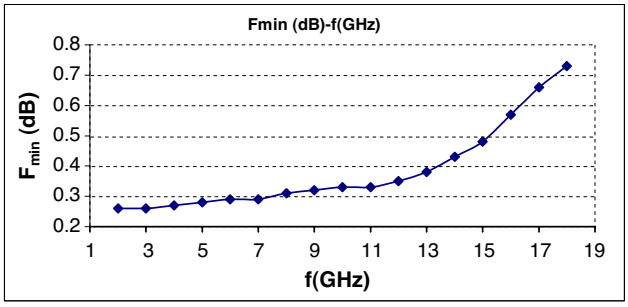


Figure 4. Minimum noise profile for the NE329S01 transistor for the bias condition $V_{CE} = 2\,\mathrm{V}$, $I_C = 10\,\mathrm{mA}$.

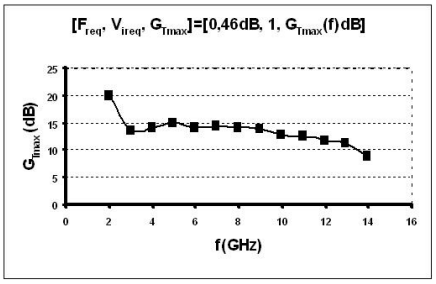
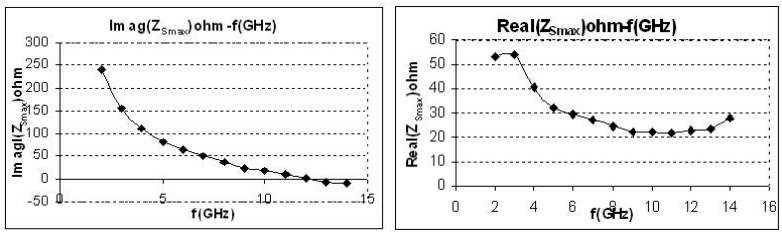
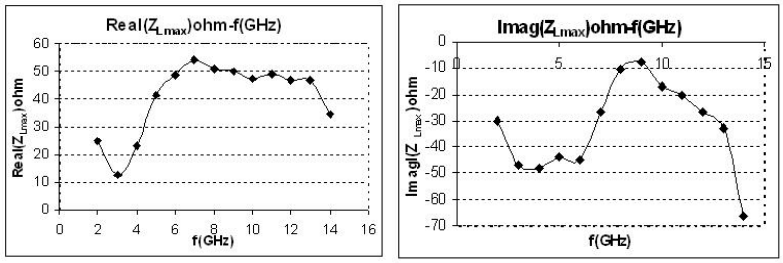


Figure 5. The [0.46 dB, 1, $G_{T_{\max}}(f)$] triplet for the NE329S01 transistor.



(a)



(b)

Figure 6. (a) The source termination functions of the [0.46 dB, 1, $G_{T_{\max}}(f)$] triplet for the NE329S01 transistor. (b) The load termination functions of the [0.46 dB, 1, $G_{T_{\max}}(f)$] triplet for the NE329S01 transistor.

The performance characterization of the NE329S01 transistor is completed, thus for the chosen bias condition $V_{DS} = 2\,\mathrm{V}$ and $I_C = 10\,\mathrm{mA}$, the maximum gain profile $G_{T_{\max}}(f)$ under the constraints of $V_{i_{req}} = 1 \Leftrightarrow$ conjugate matched input port, $F_{req} = 0.46\,\mathrm{dB}$ is obtained as given in Fig. 5 with together the corresponding source $Z_{S_{\max}}(\omega_i)$ and load $Z_{L_{\max}}(\omega_i)$ terminations in Figs. 6(a) and (b), respectively.

Two design targets are chosen to be synthesized: The constrained maximum gain profile $\Rightarrow (F_{req} = 0.46\,\text{dB}, V_{i_{req}} = 1, G_{T_{\max}}(f))$ between 4 GHz and 13 GHz and the flat gain characteristic $\Rightarrow (F_{req} = 0.46\,\text{dB}, V_{i_{req}} = 1, G_{T_{req}} = 12\,\text{dB})$ characteristics over the predetermined operation bandwidth 4–11 GHz from the characteristic of the Fig. 5, respectively. The terminations $Z_{S_{req}}(\omega_i)$, $Z_L(\omega_i)$, $i = 1, \ldots, N_\omega$ of these targets are given in Figs. 6(a), (b) and 7(a), (b) respectively.

4.2. Synthesis Procedure

Input and output matching networks of the transistor are considered independently, as defined by Figs. 3(a) and 3(b) respectively. Choosing the low-pass circuit configuration $\Leftrightarrow f(s) = 1$, the real frequency technique given in the Section 3 is applied and the gains of the reciprocal and lossless matching networks are maximized using the Nelder-Mead simplex method and the two typical examples will be given below. The other many typical examples can be found in [14].

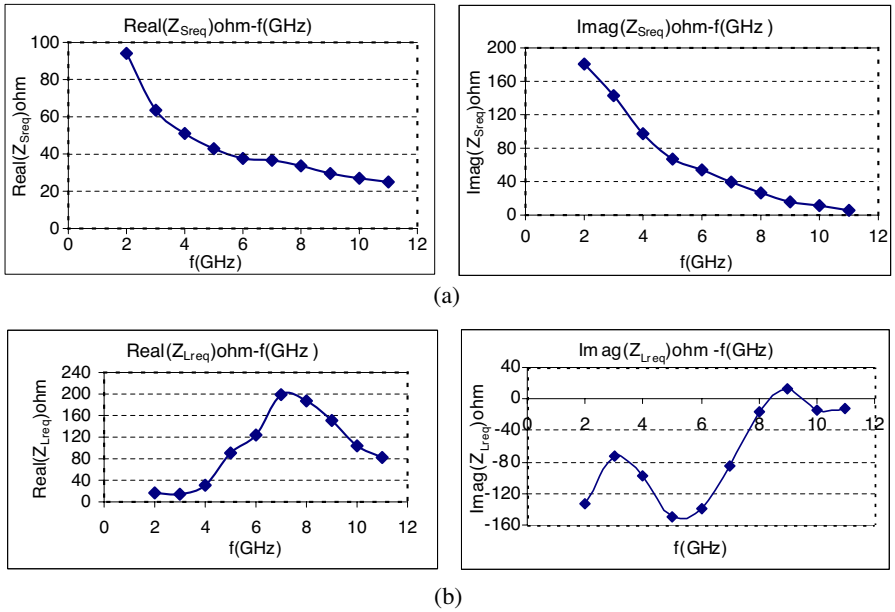
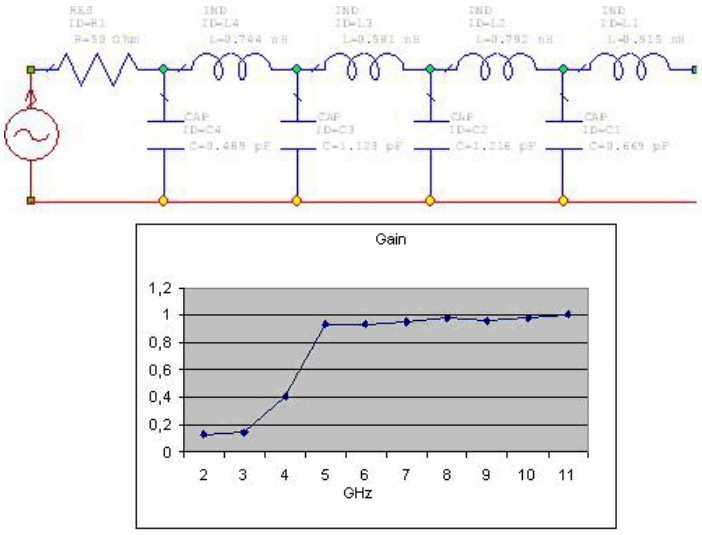
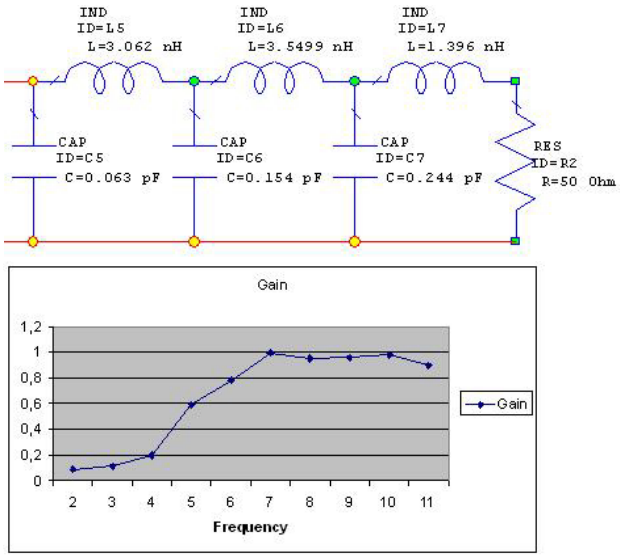


Figure 7. (a) The source termination functions of the [0.46 dB, 1, 12 dB] triplets for the NE329S01 transistor. (b) The load termination functions of the [0.46 dB, 1, 12 dB] triplets for the NE329S01 transistor.

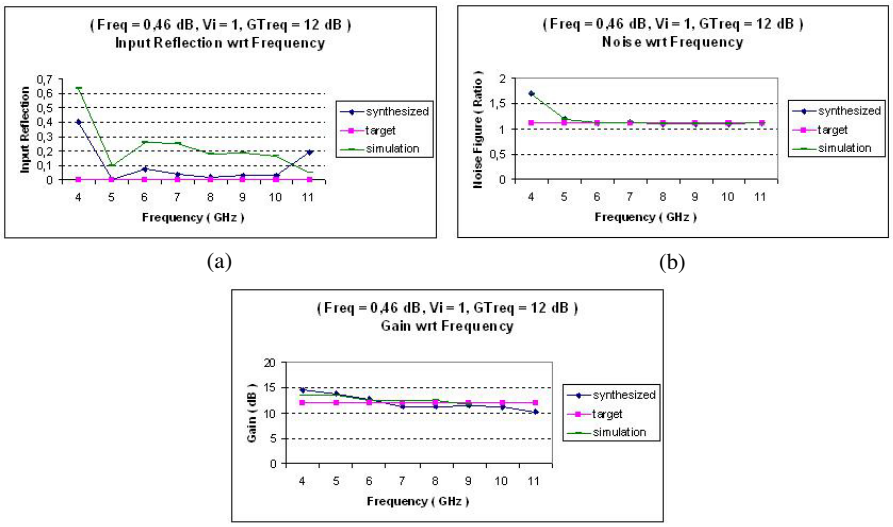


(a)



(b)

Figure 8. (a) Input matching circuit with the gain characteristic for the $[F_{req} = 0.46\,\mathrm{dB},\ V_{i_{req}} = 1,\ G_{T_{req}} = 12\,\mathrm{dB}]$ triplet $B = 4\,\mathrm{GHz},\ \ldots,\ 11\,\mathrm{GHz}$ of the NE329S01 transistor. (b) Output matching circuit with the gain characteristic for the $\left[F_{req} = 0.46\,\mathrm{dB}, V_{i_{req}} = 1, G_{\mathrm{T}_{req}} = 12\,\mathrm{dB}\right]$ triplet for $B = 4\,\mathrm{GHz},\ \ldots,$ 11 GHz of the NE329S01 transistor.



(a) (b)

(c)

Figure 9. (a) Input reflection characteristics for the matching given by the Figs. 8(a) and 8(b). (b) Noise characteristics for the matching given by the Figs. 8(a) and 8(b). (c) Gain characteristics for the matching given by the Figs. 8(a) and 8(b).

4.2.1. Matching with the Design Target of ($F_{req} = 0.46\,\mathrm{dB}$, $V_{i_{req}} = 1$, $G_{T_{req}} = 12\,\mathrm{dB}$) *over the Operation Bandwidth (*$B = 4\,\mathrm{GHz}, \ldots, 11\,\mathrm{GHz}$*)*

The Belevitch polynomials $h(s)$ and $g(s)$ are obtained for the input (front-end) and output (back-end) matching circuits and given in (14a)–(14b) and (15a)–(15b) respectively as follows:

$$\begin{aligned} h_i(s) &= -36.4417s^8 - 7.2364s^7 - 70.3068s^6 - 19.9067s^5 - 40.9470s^4 \\ &\quad -16.2905s^3 - 6.8698s^2 - 3.9457s \qquad (14a) \\ g_i(s) &= 36.4417s^8 + 50.3818s^7 + 104.4155s^6 + 98.5184s^5 \\ &\quad +91.4305s^4 + 55.6473s^3 + 25.3272s^2 + 8.1377s + 1 \qquad (14b) \\ h_o(s) &= -1.97s^6 + 7.9986s^5 - 0.7677s^4 + 12.9658s^3 \\ &\quad +1.1402s^2 + 4.7371s \qquad (15a) \\ g_o(s) &= 1.97s^6 + 10.0403s^5 + 10.1155s^4 + 17.352s^3 \\ &\quad +8.8318s^2 + 6.3328s + 1 \qquad (15b) \end{aligned}$$

Furthermore the low-pass circuit synthesizes of the corresponding

scattering parameters to the Belevitch polynomials given by (14a), (14b) and (15a), (15b) are given in Figs. 8(a) and (b) with together their gain characteristics, respectively.

The resulted input reflection, noise and gain characteristics of the amplifier are given as compared with target and simulation characteristics in the Figs. 9(a), (b), (c), respectively.

4.2.2. Matching with the Design Target ($F_{req} = 0.46\,\text{dB}, V_{i_{req}} = 1$, $G_{T_{\max}}(f)$), $B = 4$–$13\,\text{GHz}$

The Belevitch polynomials $h(s)$ and $g(s)$ are given in (16a)–(16b) and (17a)–(17b) for the input (front-end) and output (back-end) matching

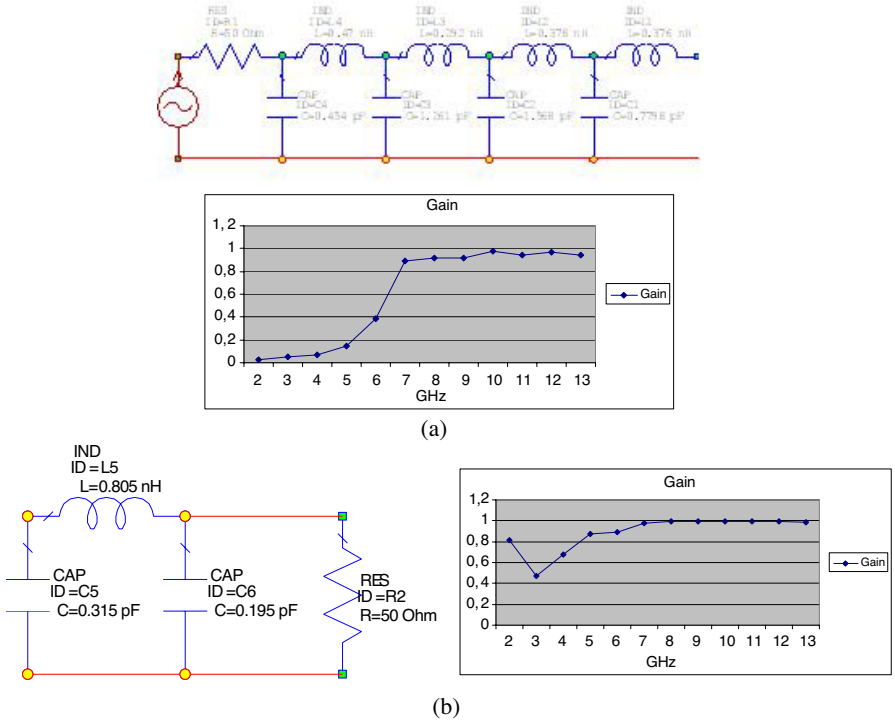


Figure 10. (a) Input matching circuit with the gain characteristic by the Gain approach for the $(F_{req} = 0.46\,\text{dB}, V_{i_{req}} = 1, G_{T_{\max}}(f))$ triplet $B = 4\,\text{GHz}, \ldots, 11\,\text{GHz}$ of the NE329S01 transistor. (b) Output matching circuit with the gain characteristic by the Gain approach for the $(F_{req} = 0.46\,\text{dB}, V_{i_{req}} = 1, G_{T_{\max}}(f))$ triplet, $B = 4\,\text{GHz}, \ldots, 11\,\text{GHz}$ of the NE329S01 transistor.

circuits, respectively as follows:

$$\begin{aligned} h_i(s) &= -24.4533s^8 - 24.7261s^7 - 43.9264s^6 - 54.2865s^5 \\ &\quad -22.8909s^4 - 3.117s^7 - 7.6003s \end{aligned} \tag{16a}$$

$$\begin{aligned} g_i(s) &= 24.4533s^8 + 49.2442s^7 + 81.0095s^6 + 102.0565s^5 \\ &\quad +78.7888s^4 + 62.1941s^3 + 23.8268s^2 + 10.2675s + 1 \end{aligned} \tag{16b}$$

$$h_0(s) = -0.843s^3 - 0.3742s^2 - 0.4142s \tag{17a}$$

$$g_0(s) = 0.843s^3 + 1.5901s^2 + 1.8308s + 1 \tag{17b}$$

The corresponding low-pass synthesizes of the input (front-end) and output (back-end) matching circuits are given in Figs. 10(a) and (b) with together their gain characteristics.

Figures 11(a), (b), (c) denote variations of the input reflection, noise and gain with respect to the frequency for the whole amplifier circuit.

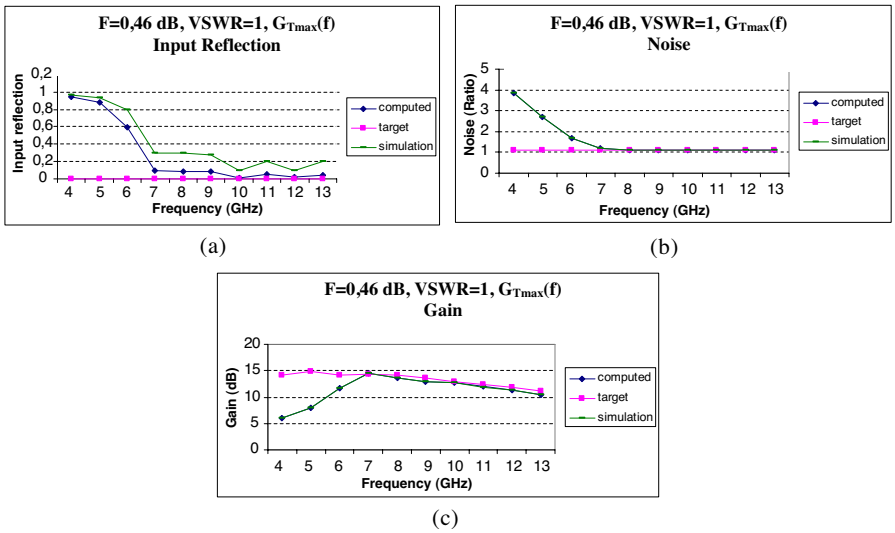


Figure 11. (a) Input reflection characteristics for the matching given by the Figs. 10(a) and 10(b). (b) Noise characteristics for the matching given by the Figs. 10(a) and 10(b). (c) Gain characteristics for the matching given by the Figs. 10(a) and 10(b).

5. CONCLUSIONS

In this work, design of a microwave amplifier is aimed at as a generalized systematic procedure in these respects: (i) Establishment of a Feasible Design Target Space (FDTS) taking into account the physical limits and/or compromise relations within the design hexagon consisting of bias voltage V_{DS}, bias current I_{DS}, noise F, gain G_T, input VSWR V_i, operation bandwidth B for the used active device; (ii) Characterization of FDTS in a convenient form to be used in Design procedure: The Performance Data Sheets (PDS) yielded from the "Active Device Characterization" stage as given in the Fig. 2, has a fairly long-working term in literature, but has found a vital application opportunity in this work; (iii) Simplification of the multi-objective design procedure of the compatible (F, V_i, G_T) triplets into the design of the source Z_S and load Z_L terminations associated with the triplets. This consists of using an impedance data modeling technique to design of the two lossless and reciprocal two-ports; (iv) The scattering-parameter formulation of the matching circuits to ensure the required (F, V_i, G_T) over the predetermined bandwidth B of the transistor. A novel impedance data modeling technique the "Simplified Real Frequency Technique (SRFT)" to is used for this purpose.

Furthermore an application example is given by choosing a novel high technology transistor where "the initial value" problem is overcome applying N successive narrow-band design procedure taking all the initial values unities. Besides both performance analysis and simulation is made and compared to each other, and it is concluded they are agreed to each other.

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