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HIGH-GAIN CMOS LOW NOISE AMPLIFIER FOR ULTRA WIDE-BAND WIRELESS RECEIVER

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Abstract—A 3–5 GHz broadband CMOS single-ended LNA with a new theoretical approach based on least-square algorithm is presented in this paper. The design consists of a wideband input impedance matching network, a cascoded amplifier with inductively-degenerated LNA, and an output impedance matching network. It is simulated in TSMC 0.18 µm standard RF CMOS process. The optimum matching network is designed to minimize the noise figure (NF) and maximize the power gain. The elements values of optimum matching network have been obtained using the least-square algorithm. The proposed LNA exhibits a gain in range of 19.9–18.9 dB, over the UWB low-band (3 to 5 GHz). Moreover, the noise figure is obtained in range of 0.6–0.8 dB. Besides, the input P1-dB and IIP3 are −10.5 dBm and 18 dBm, respectively. The proposed method has minimum 4 dB power gain improvement in relative to similar works with constant noise figure. Also, the DC supply is considered to be 1.8 V.

1. INTRODUCTION

Recently, numerous methods have been proposed for ultra-wideband (UWB) communication systems of IEEE 802.15.3a. Since the Federal Communications Commission (FCC) established an unlicensed communication band (3.1–10.6 GHz) and restricted transmitted power levels, in the spring of 2002, UWB systems have become an increasingly popular technology, which is capable of transmitting data over a wide spectrum of frequency. The FCC defined an UWB signal to have a spectral occupancy over 500 MHz or a fractional bandwidth of more than 20%. There are basically two different system level communication strategies employed to efficiently utilize the entire UWB spectrum, namely, Impulse-type UWB (IR-UWB) and carrier-based orthogonal frequency division multiplexing (OFDM). There exist

several architectures to improve the frequency bandwidth of low-noise amplifiers (LNAs), including distributed [1] and shunt feedback [2] topologies. In this paper, two embedded band pass filter are used as the input and output impedance matching networks, optimized with least-squre method, for the cascode LNA with inductive source degeneration topology, yet it is capable of achieving input impedance matching and a low noise figure (NF). The proposed LNA, designed for multiband OFDM UWB systems, employs a 0.18 µm TSMC CMOS process with an f_t greater than 90 GHz. The remaining of this paper is organized as follows. In Section 2, circuit design is introduced; in Subsection 2.1, wideband matching network is proposed and in Subsection 2.2, the proposed LNA circuit is considered. Simulation results are presented in Section 3. Finally, in Section 4, conclusions of this paper are presented.

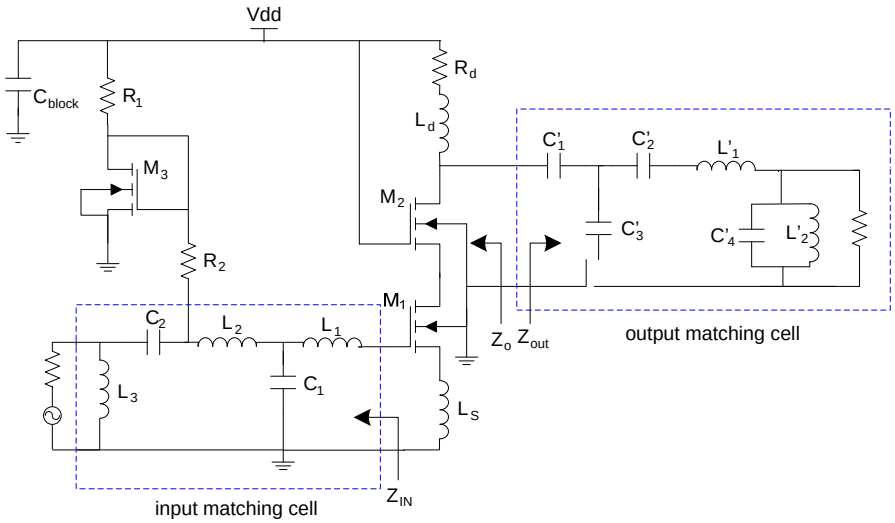

Figure 1. Schematic of the proposed low-noise amplifier for UWB system.

2. CIRCUIT DESIGN

2.1. Wideband Matching Network

The proposed method is explained and discussed by taking the circuits of a five-order band pass filter for input and output matching cell. Fig. 1 shows the circuit description of the LNA designed

with the proposed methodology in this paper. The inductive source degeneration of M_1 by L_S is used to adjust the real part of the input impedance Z_{IN} at M_1 input. Z_{IN} can be approximated by [3, 4].

$$Z_{IN} = R_{opt} + jX_{opt} \tag{1}$$

where R_{opt} and X_{opt} are the optimum source resistance and the optimum source reactance, respectively, which are given by

$$R_{opt} = \frac{m}{\omega C_{gs}} \tag{2}$$

$$X_{opt} = -\omega L_s + K/(\omega C_{gs}) \tag{3}$$

where K is a technology-dependant parameter, and its value approaches 0.8 for 0.18 µm technology, also m is another technology-dependant parameter. K and m are comparable values, and if $\omega L_s \ll K/\omega C_{gs}$, we may write $X_{opt}(\omega) \approx K/\omega C_{gs}$. So, $X_{opt} = nR_{opt}$ where $n = K/m$, and it is a constant value. Moreover, C_{gs} is gate-source capacitance.

The designing procedure is based directly on the scattering parameters data without any approximation by the unilateral model. In this paper, $[S_{ij}]$ denotes normalized scattering matrix to 50 Ω; the impedance at port 2 of the input matching network is denoted by Z_i and given by

$$Z_{IN} = \frac{a_5S^5 + a_4S^4 + a_3S^3 + a_2S^2 + a_1S + a_0}{b_4S^4 + b_3S^3 + b_2S^2 + b_1S}, \tag{4}$$

where, a_i's are defined as:

$$a_5 = L_3L_1L_2C_1C_2, \tag{5}$$

$$a_4 = Z_0\left(L_1C_1C_2L_3 + L_1L_2C_1C_2\right), \tag{6}$$

$$a_3 = L_1L_3C_2 + L_2L_3C_2, \tag{7}$$

$$a_2 = Z_0\left(C_2L_3 + L_1C_1 + L_1C_2 + L_2C_2\right), \tag{8}$$

$$a_1 = L_3 \tag{9}$$

and

$$a_0 = Z_0. \tag{10}$$

and b_is are defined as

$$b_4 = L_3L_2C_1C_2, \tag{11}$$

$$b_3 = Z_0\left(C_1C_2L_3 + C_2C_1L_2\right), \tag{12}$$

$$b_2 = L_3C_1 + L_3C_2, \tag{13}$$

and

$$b_1 = C_1 + C_2. \tag{14}$$

In the first step of this procedure the reflection coefficient (Γ_i) of the input matching network is reduced and normalized to optimum source impedance (i.e., Z_{opt}), corresponding to minimum noise figure ($\mathrm{NF}_{\min}$), and Γ_i is given by

$$\Gamma_i = \frac{Z_{IN} - Z_{opt}^*}{Z_{IN} + Z_{opt}} \tag{15}$$

The desired Z_{IN} is obtained to minimize the error function of $E(\omega)$, which is defined as:

$$E(\omega) = \sum_{i=1}^{k} \left| \left| \frac{Z_{IN}(j\omega_i) - Z_{opt}^*(j\omega_i)}{Z_{IN}(j\omega_i) + Z_{opt}(j\omega_i)} \right|^2 - |\Gamma_i(j\omega_i)|^2 \right| \tag{16}$$

where k is the observation points, and ω_i is the frequency corresponds to observation points.

Z_{IN} is specified with unknown coefficients; $E(\omega)$ can be minimized using the non-linear least-squares method [5].

The transducer power gain of the network is given by

$$G(\omega^2) = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)} \cdot (1 - |\Gamma_i|^2) \cdot \frac{1 - |\Gamma_o|^2}{1 - |\Gamma_o|^2} \tag{17}$$

where Γ_o is the reflection coefficient of output matching network at port 1; it is normalized to output impedance of active device Z_o, when its input is terminated in input matching cell and $50\,\Omega$. Γ_o is given by

$$\Gamma_o = \frac{Z_{out} - Z_o^*}{Z_{out} + Z_o} \tag{18}$$

It can be seen in Fig. 1 that Z_{out} is the impedance of the output matching network at port 1.

The second step is similar to the first one; it finds Z_{out} to reduce the reflection coefficient of output matching network.

2.2. The Proposed LNA Circuit

The cascode architecture generally improves the frequency response of the amplifier, reverses isolation, and reduces the Miller effect. Moreover, a single-ended amplifier is preferred over its differential counterpart to eliminate the need for a balun. Fig. 1 shows the complete schematic of designed LNA. The width $0.18\,\mu\mathrm{m}$ of transistor

M_1 is chosen to satisfy the power budget requirement and to achieve the minimum R_n and $\mathrm{NF}_{\min}$ (first step of design technique). With this choice of parameters, the cascode core draws a small current of 12 mA from a 1.8 V power supply. M_1, M_3 and R_1 form a current mirror to provide the bias for the input transistor. The width of M_3 is chosen to be very small to minimize the power headroom of the bias circuitry ($W_{M3} = 0.2\,\mu\mathrm{m}$). The resistor R_2 is chosen very large to reduce its noise contribution to the input of LNA [12]. Also, a matching network is designed in previous section to obtain the desired bandwidth. The values of passive elements in the input matching network are $L_1 = 8\,\mathrm{nH}$, $C_1 = 664\,\mathrm{pF}$, $L_2 = 1.1\,\mathrm{nH}$, $L_3 = 2.5\,\mathrm{nH}$, and $C_2 = 33.8\,\mathrm{pF}$. The output load of LNA is a shunt-peaking structure and is formed by an inductor ($L_d = 1.5\,\mathrm{nH}$) in series with a resistor ($R_d = 1.2\,\Omega$). The values of passive elements in the output matching network are $L_1' = 5\,\mathrm{nH}$, $C_1 = 3.1\,\mathrm{pF}$, $L_2' = 1.4\,\mathrm{nH}$, $C_2' = 0.36\,\mathrm{pF}$, $C_3' = 1.33\,\mathrm{pF}$, and $C_4' = 1.14\,\mathrm{pF}$. The inductive nature of this load compensates the gain roll-off of LNA at high frequencies. Shunt peaking load is used at the drain of the cascade transistor to enhance the bandwidth of the LNA. The value of R_d ($1.2\,\Omega$) is chosen as a compromise between the gain at low frequencies and the linearity. The inductance L_d (1.5 nH) also compensates the current gain roll-off at high frequencies. For the designed LNA, the width of M_2 is chosen grater than the width of M_1 to improve the gain and stability. The circuit is simulated by using Agilent's Advanced Design System (ADS). The power consumption is 23 mW.

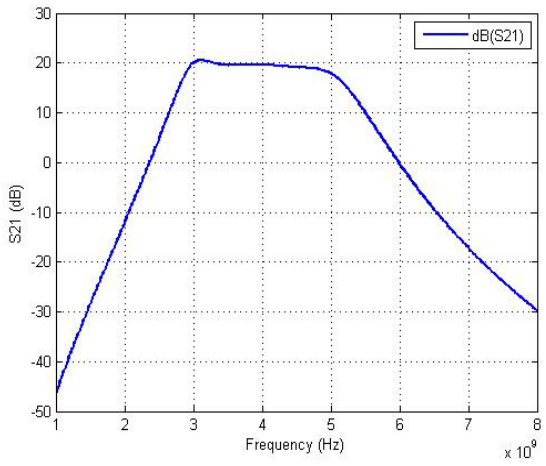

Figure 2. Power gain.

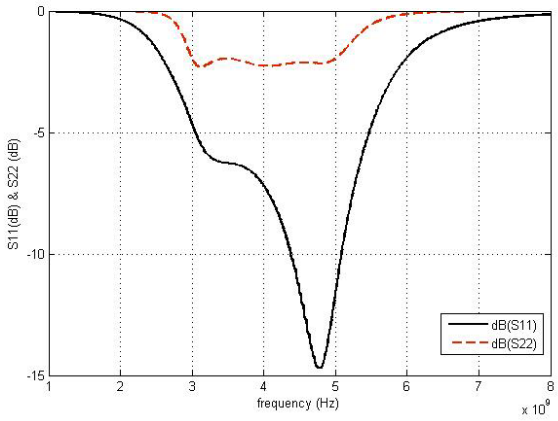

Figure 3. Input and output return loss.

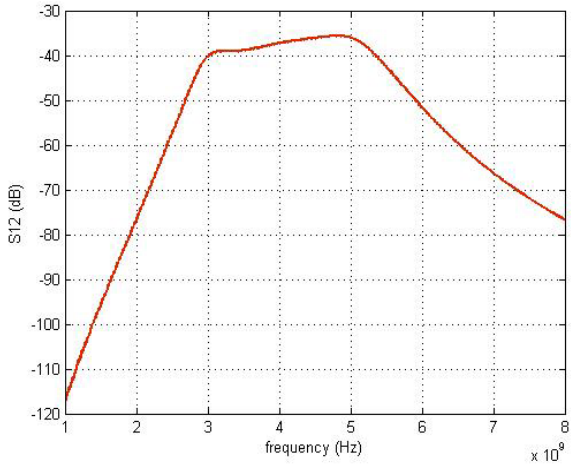

Figure 4. Reverse isolation.

3. SIMULATION RESULT

The UWB LNA circuit is simulated in Agilent ADS simulator using TSMC 0.18 µm mixed signal 1P6M CMOS process with RF model with a 1.8-V supply voltage, and the results are show in Fig. 2 to Fig. 4. Fig. 2 shows the forward gain (S_{21}) and the input and output

reflection coefficients S_{11} and S_{22} in the bandwidth between 3 GHz to 5 GHz. Using the matching network we achieve a good gain flatness of $+/-1$ dB with the maximum gain of 19.9 dB at the frequency of 3 GHz and the minimum gain of 18.9 dB at frequency of 5 GHz. Besides, the S_{11} is approximately less than -7 dB and becomes worse while the operating frequency is less 3.5 GHz. In Fig. 3, it can be seen

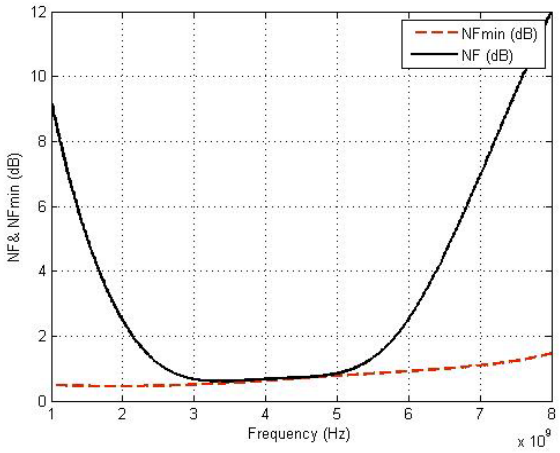

Figure 5. Noise-figure.

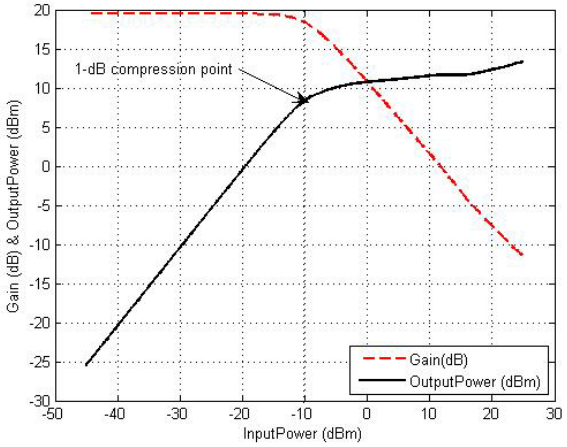

Figure 6. Input power comperssion 1 dB.

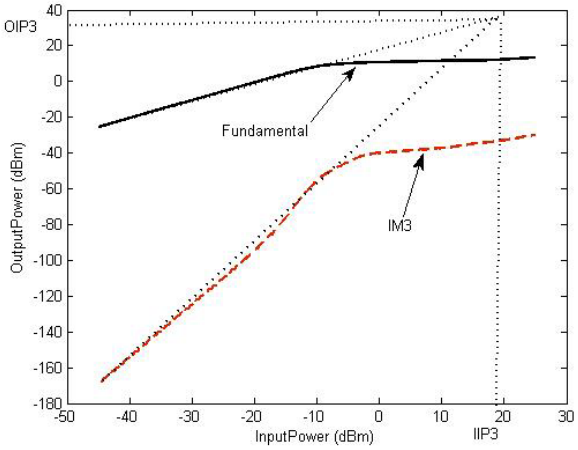

Figure 7. Third order intercep point.

that the high reverse isolation (S_{12}) is below −37 dB. The noise figure is approximately below 0.87 dB as shown in Fig. 4. The minimum one is 0.65 dB at 3.1 GHz. The 1-dB compression point (P1dBin) is approximately −10 dBm at the center frequency of 4 GHz as shown in Fig. 5. The third order inter-modulation distortion is shown in Fig. 6. The third order input intercept point (IIP3) of the LNA is +18 dBm at 4 GHz. In order to achieve a very broad bandwidth with a low noise figure, we use the relatively large bias voltage V_{gs} at the cost of power consumpation.

4. CONCLUSIONS

This paper presents a 3–5 GHz broadband CMOS LNA applied for ultra-wide-band communication applications with the 0.18 µm TSMC CMOS technology. In the UWB low band (3.1–4.8 GHz) under 1.8 V supply voltage, the broadband LNA exhibits a gain of 19–20 dB, noise figure of 0.6 dB/0.8 dB, input return loss better than 6 dB/7 dB, isolation better than 35/39 dB, IIP3 of 18 dBm and input P1dB of −10 dBm. In the 3–5 GHz range (covering 802.15a and MBOA group A) under 1.8 V compared with previously reported UWB CMOS LNAs, our LNA with a optimum match filter has an about 4–5 dB more gain and a better noise figure performance at 3–5 GHz range. This type of LNA in this paper shows a potential for high gain and low noise design applications.

REFERENCES

1. Heydari, P. and D. Lin, "A performance optimized CMOS distributed LNA for UWB receivers," *Proc. Int. Custom Integrated Circuits Conf.*, 330–333, Sept. 2005.
2. Doh, H. C., Y. K. Jeong, S. Y. Jung, and Y. J. Joo, "Design of CMOS UWB low-noise amplifier with cascode feedback," *Proc. European Solid-state Circuits Conf.*, 435–438, Sept. 2004.
3. Molavi, R., S. Mirabbasi, and M. Hashemi, "A wideband LNA design approach," *Proceedings of the International Symposium on Circuits and Systems*, 5107–5110, May 2005.
4. Hodges, D. A., R. Saleh, and H. Jackson, *Analysis and Design of Digital Integrated Circuits*, 3rd Edition, McGraw-hill, 2004.
5. Dixon, L. C. W., *Non-linear Optimization*, English University Press, London, 1972.