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EXPERIMENTAL STUDY AND SPICE SIMULATION OF CMOS INVERTERS LATCH-UP EFFECTS DUE TO HIGH POWER MICROWAVE INTERFERENCE

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Abstract—Experimental study and SPICE simulation of CMOS digital circuits latch-up effects due to high power microwave interference are reported in this paper. As a traditional inherent destruction phenomenon, latch-up effect may jeopardize the correct function of the circuits, and could be triggered in various ways such as ESD pulse, cosmic ray, heavy ion particles etc. Through the directly injected experimental investigation of CMOS inverters, it is shown that the single short high power RF pulse not only could disturb and upset the inverters output logic voltage, but also might trigger CMOS latch-up effects. It is observed that the RF pulse leading to inverters latch-up effects have energy threshold characteristics, which means that the injected RF pulse power is inversely proportional to the pulse width. SPICE simulations indicated that the inverters maximum static consumption current in latch-up state will increase up to 6600 multiples compared to the normal value when input logic state is high. With the device scaling down, higher integration and higher working frequency, the power consumption problem plays a significant role, which makes CMOS logic circuits more vulnerable due to the latch-up effects under high power microwave threats.

1. INTRODUCTION

In recent years, there has been wide interest in susceptibility understanding of electromagnetic interference effects on civil and military electronic system due to high power microwave (HPM) and ultra-wide-band (UWB) radiation. The ways of HPM radiation energy coupling to interior electronics of a system are normally defined as front-door and back-door [1]. Front-door coupling examples are the intensive EM signal couples into the front-end receivers in communication and radar systems et al through the antenna, and the interference signal frequency is normally in system operation band. Back-door coupling means EM radiation couples through apertures in system shielding structure, such as ventilation et al. The interconnected wires and power cables are also considered as strong back-door coupling ways.

A digital computer is the typical electronic system which is under HPM and UWB back-door radiation threats. Computers have been widely used in commercial and military electronics, such as real-time controlling, communications and financial systems etc. However, any computer system function errors from intentionally malicious electromagnetic pulse radiation attack or other unintentional powerful transmitters will lead to great social safety problem and economical mass loss. A number of test reports under laboratory environment indicated that intensive EM pulse coupled through the shielding cavity apertures or connecting cables might cause the computer soft failures such as restart, system abort due to complex interference effects of inner digital circuits, and even permanent physical hard damage [2–4]. It was reported that radiation field level of 4.5 KV/m can generate system crash effect in reverberation chamber susceptibility test on Pentium4 computer, and in most cases a manual restart is needed [5]. Computer networks, PC main boards and basic logic components experiments in TEM waveguide indicated that system susceptibility is more sensitive as system complexity increases [6]. Test results showed computer networks are most sensitive for field threshold UWB 0.2 KV/m, and EMP 0.5 KV/m respectively. TTL and CMOS logic components upset threshold for UWB is 25 KV/m and EMP is 120 KV/m.

Investigations on computer system EM susceptibility focus on statistical analysis of the threshold characteristics, so device level effects studies are required in order to better understand these digital circuits effects and the interference mechanism. The CMOS inverters are normally chosen in digital circuits device level effects studies because an inverter represents most CMOS fundamental

switching and DC characteristics except logic function. And typically CMOS device has an inverter in the input and output stage. The influence of pulseform and external load for TTL and CMOS inverters susceptibility were analyzed in [7], which indicated susceptibility decreases with increasing microwave frequency. By a comprehensive study of a series of electronic components (analog device and TTL, CMOS digital circuits) HPM effects and how the effects were influenced by the microwave frequency and power parameters [8], the author concluded that the basic mechanism of HPM interference is the nonlinear pn junction rectification behavior, and the strong frequency susceptibility decrease was observed. A similar report proposed that CMOS intentionally integrated additional components, such as input/output electrostatic discharge (ESD) protection nonlinear rectification response at microwave frequency is the main interference causation to make output logic state upset [9]. Destruction and malfunction of HPM experiment results demonstrated the CMOS inverter was broken with 2.46 GHz at field 10 KV/m [10]. The inverter electrical characteristics for propagation delay and static power consumer under EM pulse interference also became interesting research areas [11, 12]. Injected tests from 800 MHz to 3 GHz on individual and cascaded inverters of several channel size showed that device static power consumption increase by several orders of magnitude, which makes the system more susceptibility [13]. Except experimental studies, SPICE simulations are frequently used to investigate interference mechanism. The normal function of a clock network digital circuit can be affected by pulsed modulated radio frequency interference signal with relatively low power levels, and SPICE simulations support to explain the experimental results [14].

Latch-up effects and ESD are the traditional failure modes in CMOS circuits. Generally, the parasitic transistor combination called thyristor is triggered and generates a short channel in the CMOS circuits, thus latch-up effects happen [15]. In a very short time, a very high current flow from power supply to GND results in quite large power dissipation, and the heat accumulation will destruct the device rapidly. The parasitic thyristor in CMOS circuits can be triggered in various ways as known as port ESD pulse, cosmic ray, ionizing radiation and even high supply voltage et al. [16–18].

Although latch-up effect is no longer a problem in modern CMOS circuits except under extreme operation conditions, it still can be triggered by microwave pulse as shown in two stage CMOS inverters injected test results. The test microwave parameters are listed as follows: 1.23 GHz, pulse width 800 ns with PRF 100 Hz. When latch-up effects appeared, the circuit state maintained after the injected

microwave pulse turned off [19].

In this paper, experimental and SPICE simulation studies on integrated inverters latch-up effects is presented. A directly injected experiment setup was built carefully. In addition to the known ways to trigger CMOS circuits latch-up effects, experimental results showed that this can be also provoked by single short high power microwave pulse. Different RF pulse width injected latch-up tests demonstrated the RF pulse energy threshold characteristics. SPICE simulation results showed the inverters static power consumption increases sharply in latch-up state, which results in modern CMOS IC are more vulnerable. A clear frequency susceptibility suppressive trend is found when injected RF frequency increases. The inverters interference threshold will be significantly affected by input logic state too.

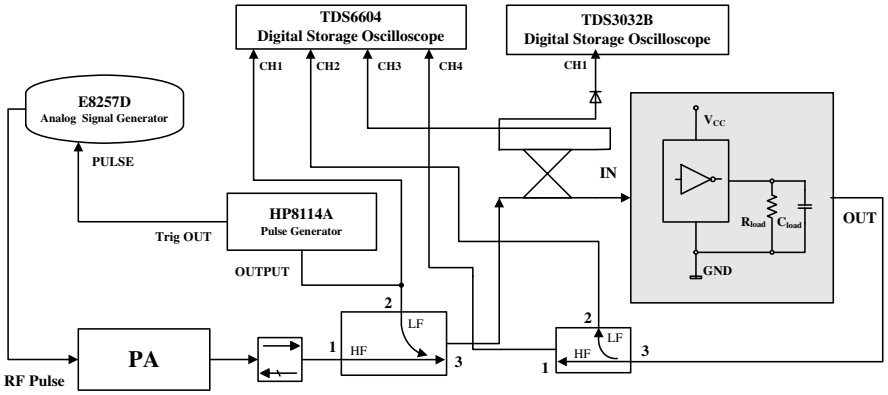

Figure 1. Schematic of directly injected experiment setup.

2. DIRECTLY INJECTED EXPERIMENTAL STUDY

The schematic of directly injected experiment setup is shown in Figure 1. The RF signal frequency ranged from 800 MHz to 4 GHz and maxim level up to 45 dBm. The modulated short RF pulse was amplified by 800 MHz–2 GHz and 2 GHz–4 GHz two power amplifiers. The tests of injected RF pulse duration located in input high or low logic state were performed separately to better understand susceptibility influence of input logic states. A single RF pulse output from signal source was manually triggered by the pulse generator which also generated the inverter synchronous operating square wave pulse. A special high isolation diplexer hybrid high power RF pulse signal with

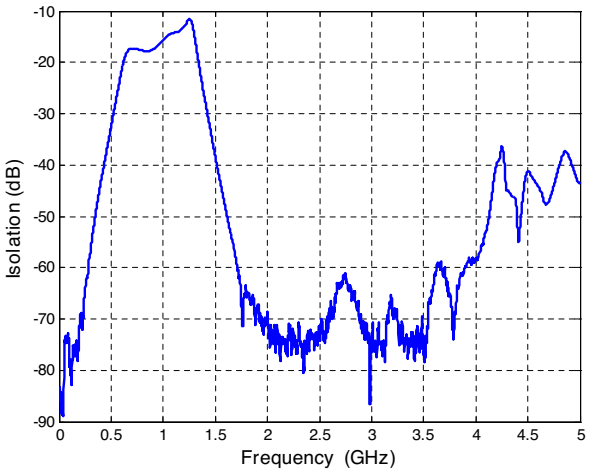

Figure 2. Measured isolation of 1.75 GHz–4 GHz/DC-100 MHz diplexer.

inverter normal square wave was designed to avoid accident leakage power damage to sensitive instruments. Two bandwidth diplexers were used to cover 800 MHz–4 GHz band. Figure 2 only shows the measured results of 1.75 GHz–4 GHz/DC-100 MHz diplexer. At the inverter output port a same diplexer was used to divide the interfered low frequency logic voltage signal and the output high frequency pulse signal. The output low frequency signal then must connect an active 1 MΩ/50 Ω impedance adapter to match the TDS6604 digital storage oscilloscope input impedance. The adapter was made by AD891 operational amplifier with DC-100 MHz band and was not shown in Figure 1. Then the four channel signals including injected RF pulse, input logic voltage, output logic voltage and output RF pulse can be correctly recorded by one digital storage oscilloscope with 50 Ω input impedance. The measured response of 1 MΩ/50 Ω impedance adapter was demonstrated in Figure 3 and the output waveform has an excellent snapshot of the input logic voltage waveform in detail. A photograph of injected PCB (printed circuits board) and shield cavity is shown in Figure 4. In order to decrease reflected RF power and insertion loss the microwave circuits board (TACONIC RF-35) was used and transmission line characteristic impedance was designed in 50 Ω.

The logic type of the test device was single gate AHC04 and partly electrical characteristics are shown in Table 1. The inverter load circuit parameter settings were defined by datasheet. The load capacity and resistance was 35 pF and 1 KΩ respectively. The inverter input logic

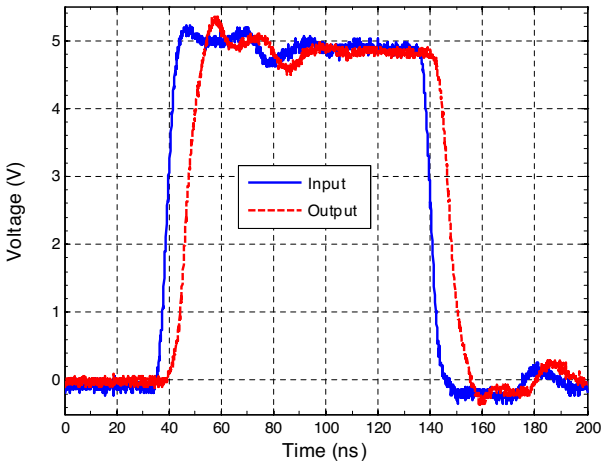

Figure 3. Measured response of active 1 MΩ/50Ω impedance adapter.

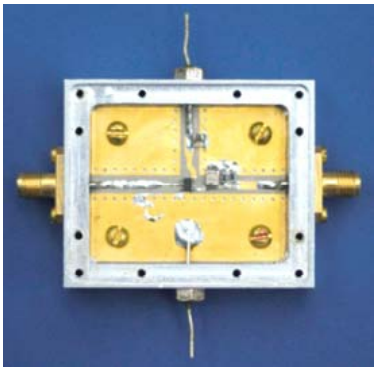

Figure 4. Inverter injected circuit.

"1" meant input voltage was Vcc (5 V/3.3 V) and input logic "0" meant input voltage was 0 V. Frequencies swept from 800 MHz to 2 GHz by step 100 MHz and five separate frequencies points as 2.3 GHz, 2.7 GHz, 3 GHz, 3.7 GHz and 4 GHz were selected in 2 GHz–4 GHz. The starting injected RF power was different at each frequency point, which means there were no obvious interference effects under starting level.

Figure 5 and Figure 6 show the measured results of inverter output logic voltage varied with injected RF pulse power and frequency under input logic "1" and "0" state cases for different supply voltage. It is clearly found the susceptibility decrease generally as RF frequency increases and the power supply voltage has little impact

Table 1. Electrical characteristics of test inverter.

Logic Type	**Function**	**Input Schmitt Trigger**	**Buffered Output**	**Input-GND Clamping Diode**
AHC04	single inverter	no	no	yes
Input-Vcc Clamping Diode	**Output-GND Clamping Diode**	**Output-Vcc Clamping Diode**	**Package Type**	**Supply Voltage**
no	yes	yes	SOT23	5 V/3.3 V

on susceptibility trend. Higher frequency tests are not performed for the amplifier band limitation. The susceptibility decrease with the RF frequency increase can be summarized by several high frequency filter factors, such as the input ESD circuits pn junction capacity, MOSFET structure and channel capacities, distributed parasitic capacity of device pins. All these circuits have low-pass characteristics. Another susceptibility trend showed in Figure 5 and Figure 6 is that threshold of input logic state might differ much.

A typical oscilloscope snapshot of inverter experimental waveform including inverter input/out logic voltage and injected/output RF pulse is shown in Figure 7. From summary of HPM narrowband source properties in [20], it is known that the pulse width ranges from some 10 ns to some 100ns and most sources operate in single shot, and normally the pulse repetition frequency is no more than 100 Hz. According to [21] particularly, pulse duration of ∼100 ns may be useful for the physical limits by the HPM source pulse shortening and microwave effects. Therefore, the single injected RF pulse with duration of 120 ns was selected from Figure 5 to Figure 8. Note that the injected RF pulse is with rise/fall time about of 6ns which is determined by the signal generator pulse modulation capability. However, various HPM narrowband source radiations may have a longer or shorter rise/fall time different with the injected waveform in Figure 7. The digital FFT analysis of inverter output RF pulse in Figure 7 (Math2) indicated a strong nonlinear effect happened. Figure 8 shows an example record of the inverter dynamic output logic voltage responses as RF pulse power varied at 1.2 GHz, which shows the process of the gradual interference in the inverter output logic waveform.

When supply voltage was 5 V and injected RF pulse duration was in input logic high state, the inverter latch-up effects appeared as demonstrated in Figure 9 and Figure 10. In injected experiments, the latch-up effects were obtained at all test frequency points. An example

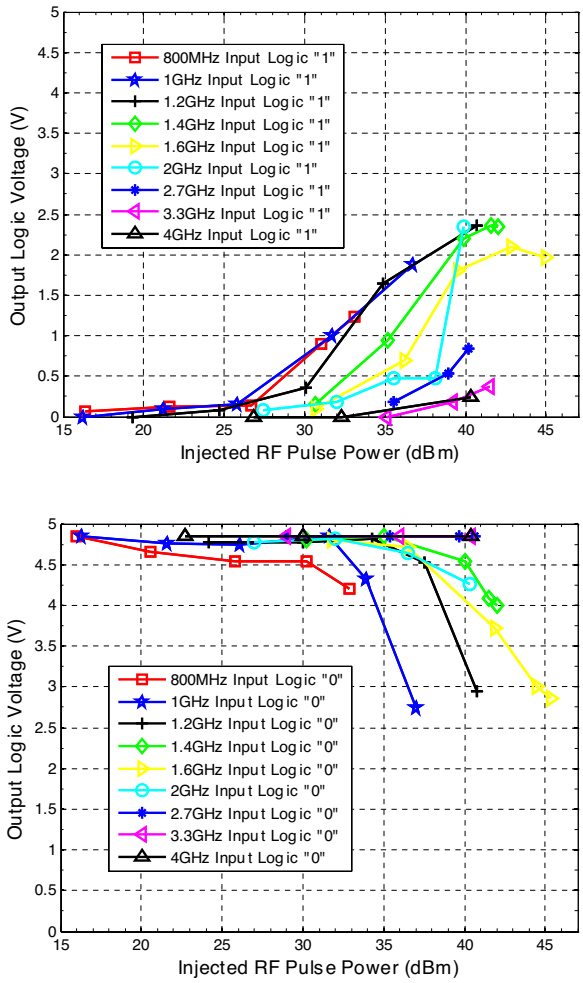

Figure 5. Measured results of the inverter output logic voltage versus frequency and power (Vcc = 5 V, left: input logic "1", right: input logic "0").

frequency point of 3 GHz was selected in Figure 9 and Figure 10. The input/output logic voltage maintained latch-up states value when injected RF pulse turned off. A manually reset operation was needed to recovery inverter normal logic function. Table 2 lists relative energy and power threshold of different RF pulse when latch-up effects just appeared. Many experiments showed the non-recovery latch-up effects would not appear under current RF pulse level when injected RF

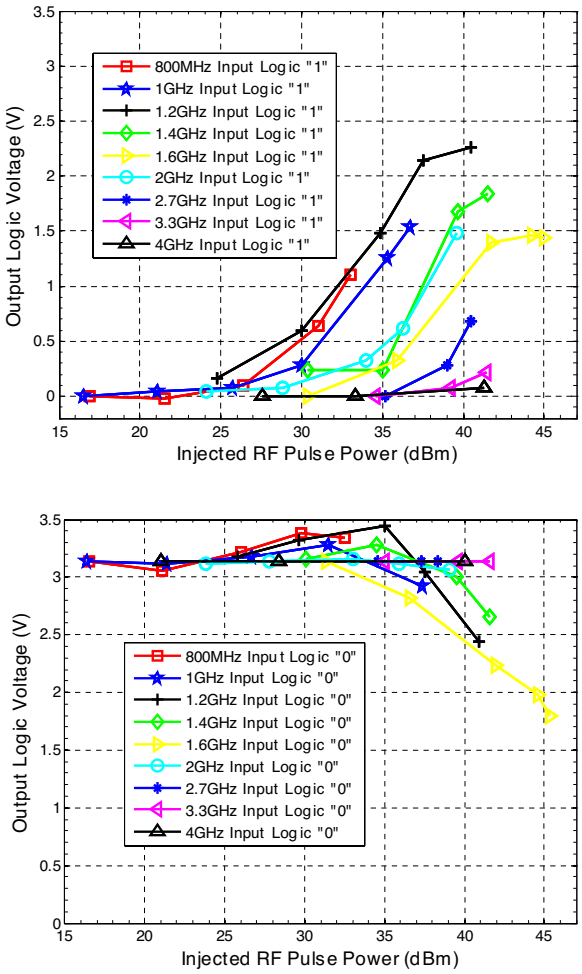

Figure 6. Measured results of the inverter output logic voltage versus frequency and power (Vcc = 3.3 V, left: input logic "1", right: input logic "0").

pulse width is lower than 60 ns. Thus the normalized threshold in Table 2 is based on 60 ns experimental data. The injected RF pulse energy threshold law is observed clearly from Table 2, which means that the injected RF pulse causing latch-up effects has characteristics of pulse power inversely proportional to the pulse width. However the minimum pulse energy causing latch-up effects is almost identical. With the increase of injected RF pulse level and pulse width, three step interference processes can be concluded as follows. First, the disturbed

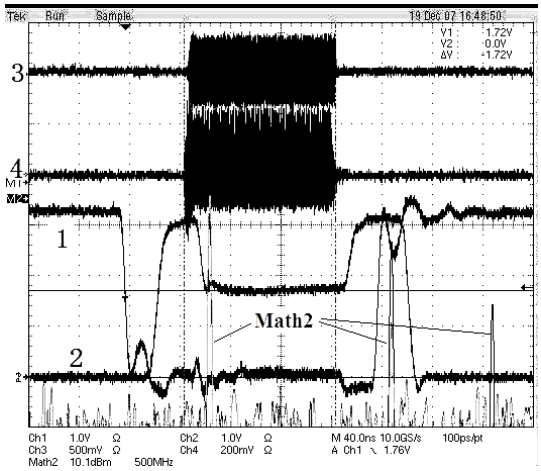

Figure 7. A typical original experimental waveform (Ch1: input logic voltage, Ch2: output logic voltage, Ch3: injected RF pulse, Ch4: output RF pulse). Vcc = 3.3 V, 1.8 GHz).

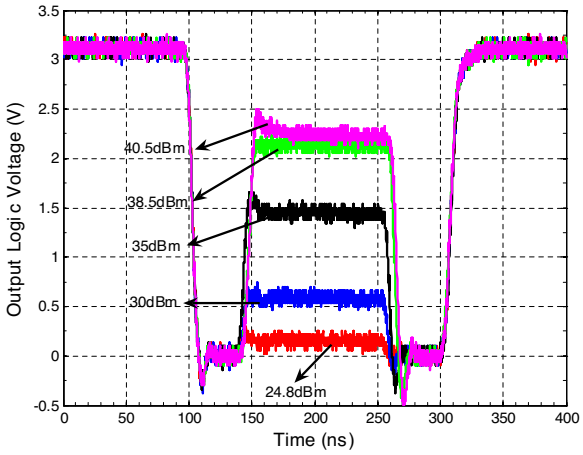

Figure 8. Measured output logic voltage waveform versus RF power (input logic "1", Vcc = 3.3 V, 1.2 GHz).

waveform width of input logic voltage was equal to injected RF pulse width. Second, the disturbed waveform width gradually increased and became larger than RF pulse width as injected power increased. However, the input logic voltage waveform would return to its normal state rapidly when the injected RF pulse width was lower than 60 ns.

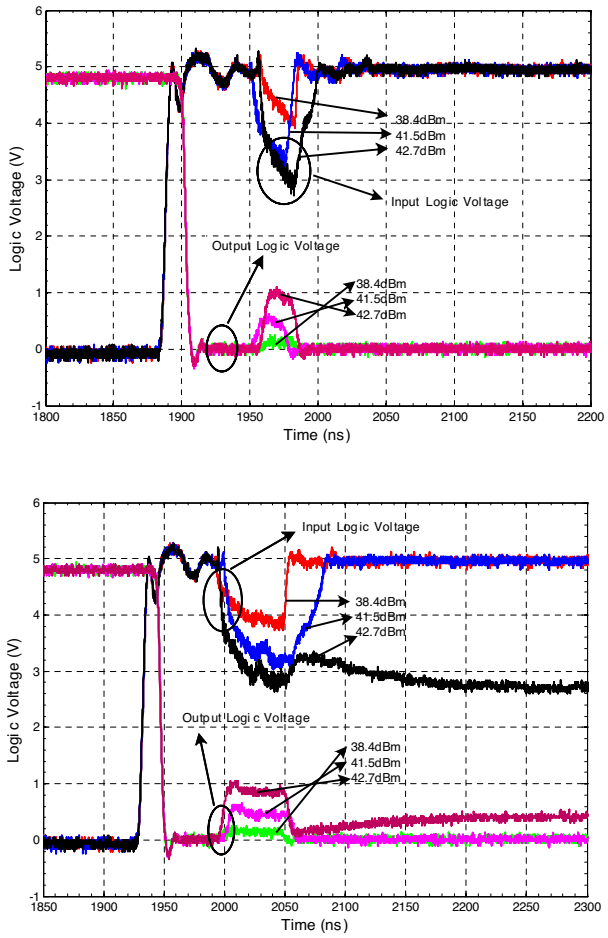

Figure 9. Measured inverter latch-up effects versus injected RF pulse width (left: 30 ns, right: 60 ns).

The third, when RF pulse width increased continually, the disturbed input/output logic voltage was fixed at abnormal value after the end of injected RF pulse, thus the latch-up effects appeared.

After injected RF pulse was turned off, the stable input/output logic voltage of 60 ns, 120 ns and 200 ns RF pulse was almost identical when the same RF pulse power level was injected into the inverter.

In Figure 11, however, when supply voltage was 3.3 V, the self-recoverable latch-up effects just appeared in injected RF pulse duration. As is previously mentioned, a higher supply voltage than

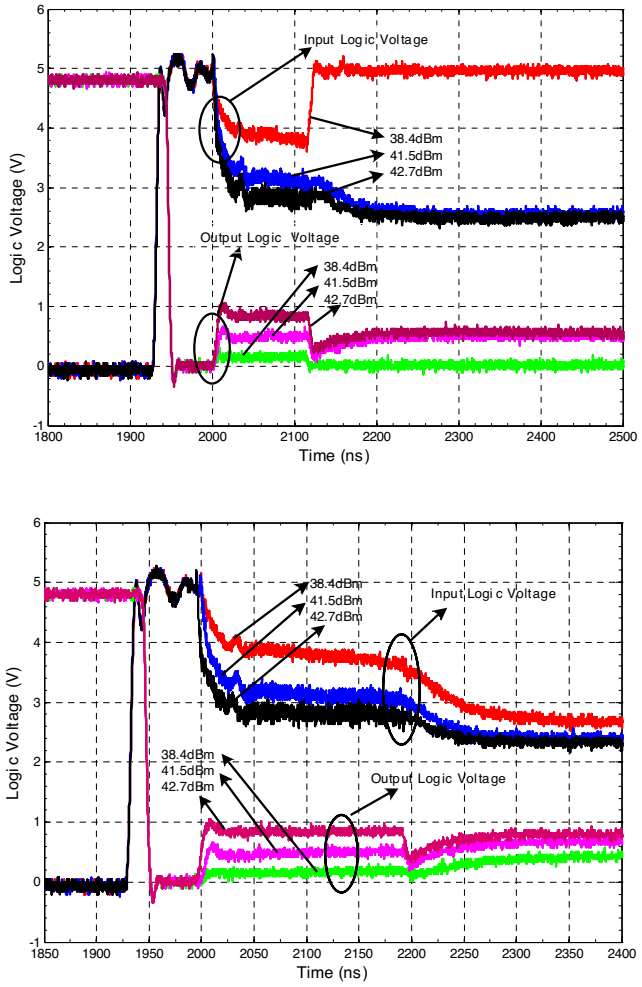

Figure 10. Measured inverter latch-up effects versus injected RF pulse width (left: 120 ns, right: 200 ns).

Table 2. Threshold characteristics of injected RF pulse causing inverter latch-up effects.

Pulse Width	30 ns	60 ns	120 ns	200 ns
Relative Power Threshold	–	0 dB	−3.2 dB	−4.7 dB
Relative Energy Threshold	–	1	0.96	1.13

the value given in data sheets may trigger the latch-up effects. So it is believed that self-recoverable latch-up effects contribute to the device lower supply voltage. Whether supply voltage was 5 V or 3.3 V, no latch-up effects were found when inverter input logic state was low.

3. SPICE SIMULATION

The inverter input/output logic voltage level will be fixed in transition state for a long time if the latch-up effects do not recover until external reset operation. This will lead to the following critical problems. The next stage circuit may confront uncertain input logic state environment, which results in output logic interference effects. What is more concerned is the very large increase in the amount of the device static current through the inverter pMOS and nMOS FET which turning on simultaneity at latch-up state. CMOS technologies are predominantly used mainly for its low power consumption. However, the sharply increasing static operation current will seriously degrade device electrical performance and even cause heat damage. So the whole system reliability will also decrease.

In order to better evaluate the impact of latch-up effects, SPICE simulations of inverter electrical characteristics under steady latch-up state are shown in Figure 11 and Figure 12. The simulation models came from semiconductor distributor with encrypted data. And inverter circuit simulation parameters were defined the same as

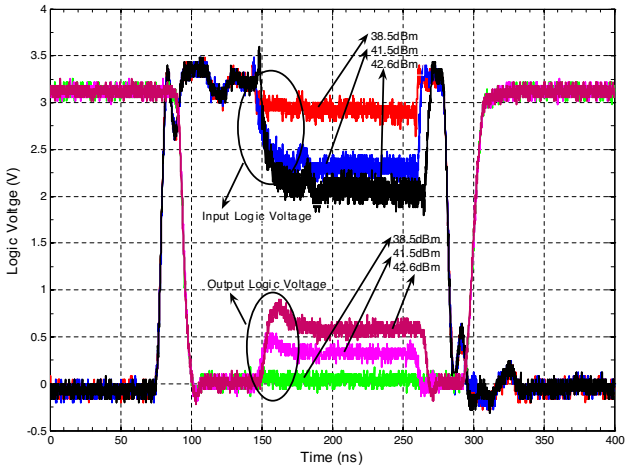

Figure 11. Measured inverter self-recoverable latch-up effects (Vcc = 3.3 V, 3 GHz).

experiments. Figure 11 (right) shows the simulations of the output logic voltage corresponding to different input logic voltage. Figure 12 shows the inverter static operation current.

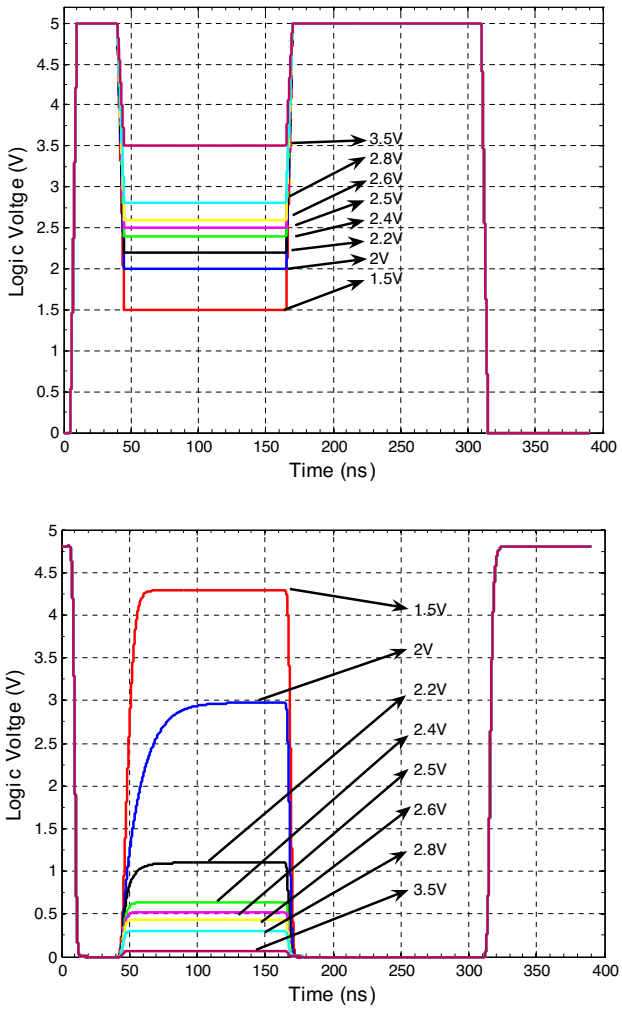

Figure 12. SPICE simulations of the inverter logic voltage under latch-up state (Vcc = 5 V, left: input logic voltage, right: output logic voltage).

From Figure 9 (right), Figure 10 and Figure 12, a good coincidence can be seen between the experimental and simulated steady input/output logic voltage. However, the experimental input/output

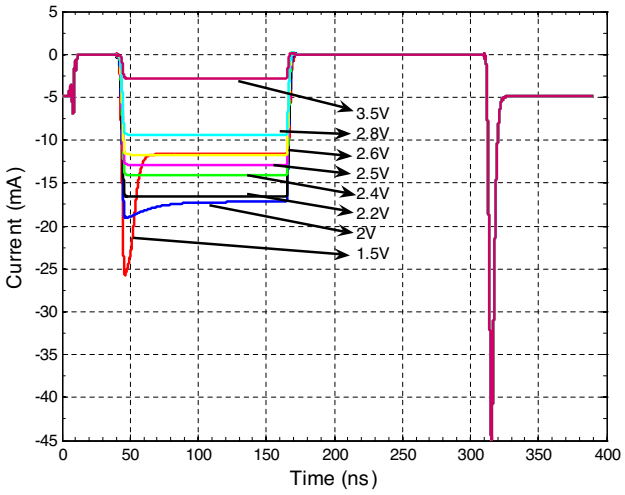

Figure 13. SPICE simulations of the inverter static operation current versus input logic voltage (Vcc = 5 V).

logic voltage relation in RF pulse injected duration was inconsistent with simulations in Figure 12. This can be explained by the effects of injected RF pulse interference. CMOS devices have very low static power consumption which results from leakage current. The normal spike current at 10 ns and 315 ns in Figure 13 validates that the CMOS devices dominant power consumption comes from dynamic logic switching process. Unfortunately, the static power consumption will increase a lot when latch-up effects appear. As shown in Figure 13, simulated latch-up current reached maxim value 17.3 mA when latch-up input logic voltage was 2 V. But the simulated normal static current value was only about 2.6 µA when input logic was high (Vcc = 5 V). Thus the increase of static current above three orders magnitude due to latch-up effects with input logic high state is obtained. If the inverter input logic voltage was 0 V, a relative small static current value of 5 mA is shown in Figure 13. The 1 KΩ resistance load contributed to this 5 mA static consumption current. Although the inverter latch-up effects tests had been continued for a long time above 1 s, the inverter damage phenomena were not observed. The main reason is the absolute maxim ratings of continuous current through from Vcc to GND in datasheet is given by ±50 mA. The steady latch-up logic voltage in Figure 10 is 2.5 V. And the corresponding simulated latch-up static current in Figure 13 is 12.5 mA, which is much lower than the device maxim ratings.

4. CONCLUSION

Experimental study and SPICE simulation of CMOS inverters latch-up effects due to high power microwave interference are reported in this paper. The experimental results showed that inverter latch-up effects will appear with the injection of only a few tens of nanoseconds single high power RF pulse. The RF pulse power inversely proportional to the pulse width characteristics of injected RF pulse causing latch-up effects is found through different RF pulse width injected experiments. However, the needed minimum RF pulse energy was identical. It is also found the inverter susceptibility trend decreases generally as RF frequency increases due to several circuit capacities bypass function. SPICE simulations indicated that the inverters maximum static consumption current in latch-up state would increase up to 6600 multiples compared to the normal value when input logic state is high. Other logic inverters experimental results showed that latch-up effects occur only when the RF pulse is injected and the devices will reset to normal logic state rapidly after the end of the pulse. It is important to minimize power consumption in a CMOS circuit to increase system reliability. However, simulations showed CMOS logic circuits are more vulnerable according to the latch-up effects under high power microwave interference. Future work will perform more investigation on the latch-up effects mechanism triggered by RF pulse.

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