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DESIGN OF A NOVEL COMPACT POWER DIVIDER WITH HARMONIC SUPPRESSION

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Abstract—This paper presents a novel compact power divider with third harmonic suppression and also can provide a direct current (dc) path which could simplify the other active circuits in the complicated phased array antenna system. The proposed power divider achieves 20% size reduction compared with the conventional Wilkinson power divider. From the measured results, it can be seen that the simulated results can guide the practical circuit very well.

1. INTRODUCTION

Wilkinson power divider is an essential components for microwave and millimeterwave antenna arrays. It is first introduced by Wilkinson in 1960 [1] and has completely matched output ports with sufficiently high isolation between them. Recently, many researchers have focused on the miniaturation and harmonic suppression for the power divider [2–9].

In this paper, a power divider with the size reduction and harmonic suppression is introduced. Apart from the above performances, it also provides a dc path for the other active circuits such as power amplifier in T/R module because of the zigzag short-ended stub of length $L1$ which is shown in Fig. 1. From the Fig. 1, we also can see two open-ended stubs of length $L2$ which is used to suppress the third harmonic signals and reduce the size with the stub $L1$. Here the two open-ended stubs $L2$ is simpler than the T-shaped microstrip lines in [3], and do not use the lumped capacitors like [2] but the two open-ended stubs play the role of them, thus it would not introduce parasitic parameters. A transmission line model is used to calculate the parameters of the zigzag short-ended stub which is to reduce the size of the power divider. The software Ansoft Designer is used to optimize the proposed power divider to take account into all the discontinuities after using Agilent ADS2004 to perform the circuit design.

2. THEORY ANALYSIS

As shown in Fig. 1, the stubs $L1$, $L2$ which is shorter than $L1$ both have an equivalent capacitive parameter C as shown in Fig. 2(b), and the value of C can be obtained from the following well known formula:

$$Z(l) = jZ_0 \tan \beta l \tag{1}$$

where Z_0 is the characteristic impedance of the short-ended stub, l is the length, β is the phase constant, we can conclude the short-ended stub whose length is less than a quarter of the wavelength would be seen as a inductor L, here the length $L1$ is more than a quarter of the wavelength, so has the equivalent effect with a capacitor $C1$. In the same way, the two open-ended stubs have the equivalent capacitors $C2$.

The analysis method is similar with the conventional Wilkinson power divider as given in [1], but here there are three equivalent capacitors $C1$ and two $C2$ for the three open-ended and short-ended

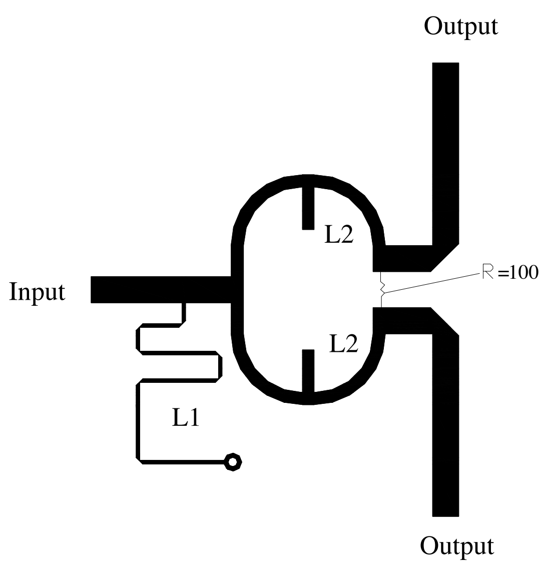

Figure 1. Schematic of proposed power divider.

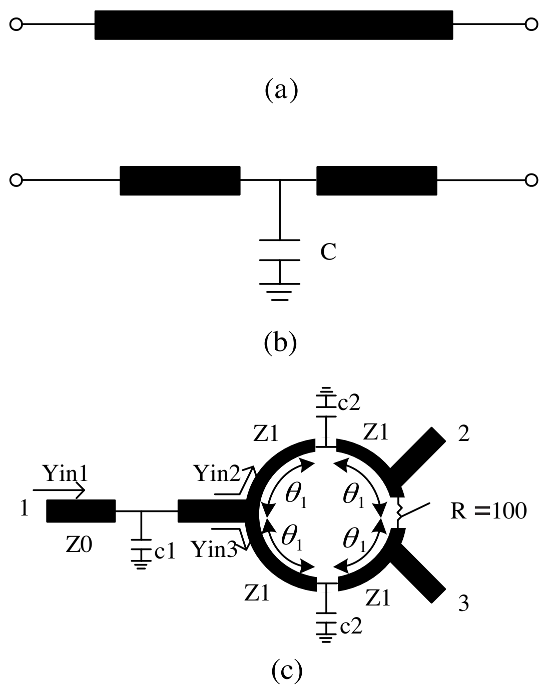

Figure 2. Schematic of (a) conventional microstrip line, (b) equivalent microstrip line with open or short stub, (c) the whole equivalent circuit for the power divider.

stubs, so the ultimate equivalent circuit is given in Fig. 2(c), the values of $C1$, $C2$, $Z1$, θ_1 can be determined by the conventional divider analysis method. The voltages at the two outputs should be equal, and for the zero reflection from all ports and infinite isolation between the ports 2 and 3, the resistor R must be equal to $2Z_0$ [1], that is $R = 100$. And the Y_{in1} can be expressed as follows:

$$Y_{in1} = Y_c + Y_{in2} + Y_{in3} = Y_0 \tag{2}$$

where $Y_c = jwc_1 = -jY_{short}ctg(\beta l_1)$

The input admittances Y_{in2} and Y_{in3} have the following expression:

$$Y_{in2} = Y_{in3} = Y_1 \frac{Y_L + jY_1 \tan\theta_1}{Y_1 + jY_L \tan\theta_1} \tag{3}$$

where $Y_L = Y_1 \frac{Y_0 + jY_1 \tan\theta_1}{Y_1 + jY_0 \tan\theta_1} + Y_2$ and

$$Y_0 = 1/Z_0, \quad Y_1 = 1/Z_1, \quad Y_2 = jwc_2 = jY_{open}tg(\beta l_2)$$

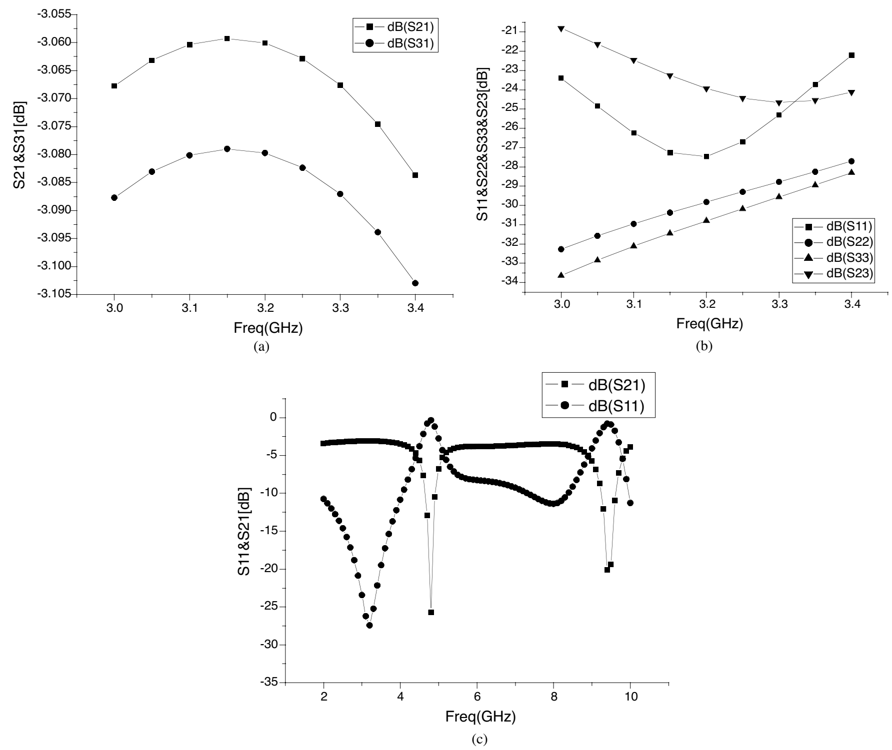

Figure 3. Simulated results of the proposed power divider, (a) transmission magnitude of the two outputs, (b) the input and output return loss at three ports and the isolation between the two outputs, (c) the input and output return loss for the third harmonic signal suppression.

According to the above formula, the values of $C1$, $C2$, $Z1$, θ_1 can be obtained and the simulations were carried out in Agilent ADS2004 [11], and then validated by another software Ansoft Designer [12]. Fig. 3 is the simulated S parameters for required bandwidth from 3.0 GHz to 3.4 GHz and a much wider bandwidth to see the harmonic suppression phenomenon. We can see the S_{21} and S_{31} is higher than -3.10 dB in Fig. 3(a), and the VSWR for all the ports is less than 1.15 from the reflection coefficient in Fig. 3(b). The isolation between the two outputs is better than 20 dB. The third harmonic at about 9.6 GHz is suppressed by 10 dB.

Figure 4. Photography of the fabricated power divider.

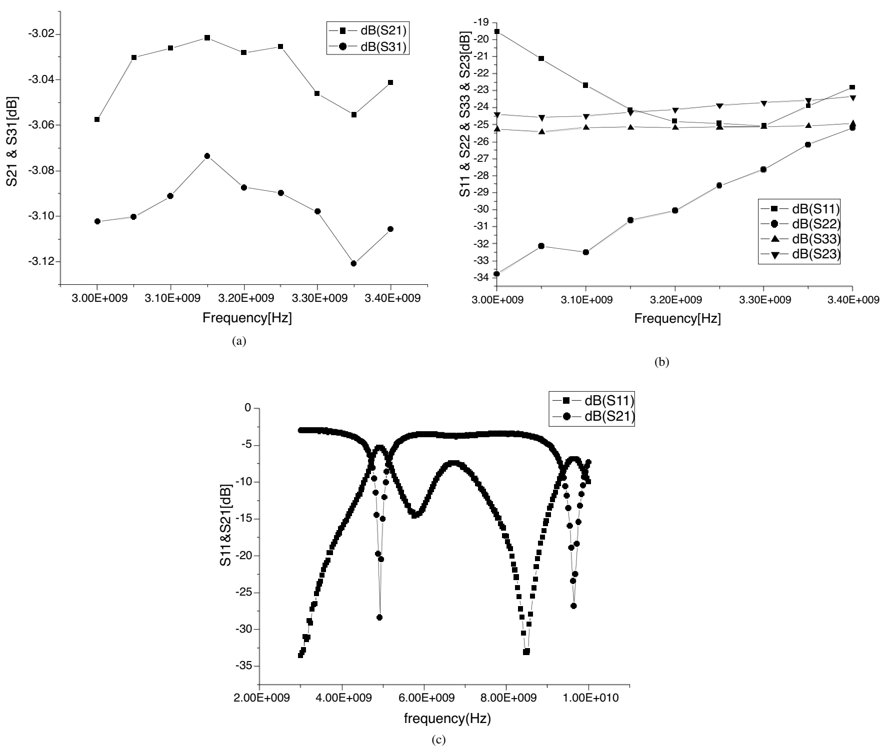

Figure 5. Measured results, (a) transmission magnitude of the two outputs, (b) the input and output return loss at three ports and the isolation, (c) the input and output return loss for the third harmonic suppression.

3. EXPERIMENTAL RESULTS

Based on the above analysis and simulated results, the proposed power divider is fabricated with Duriod5880 (relative permittivity $\varepsilon_r = 2.2$, dielectric loss $\tan\delta = 0.0009$, height $h = 0.508\,\text{mm}$). The photography of fabricated power divider is shown in Fig. 4. The size is $20\,\text{mm} \times 25\,\text{mm}$, while the conventional Wilkinson power divider is $25\,\text{mm} \times 25\,\text{mm}$, so 20% size is reduced. Then the measurements were performed by an Vector Network Analyzer Agilent E8363B with a standard Short-Open-Load-Thru (SOLT) calibration procedure. In Fig. 5(a), the average insertion loss is so small that it has been very near to the simulated ones. This is unusual for the formal design [3, 4, 10]. But there is a little amplitude imbalance about 0.06 dB, because the assembling area for resistor R is a little more than the size of the real one, thus the amplitude imbalance at the two outputs is introduced, but it is good enough. The VSWR for all the ports is less than 1.25 from the reflection coefficient in Fig. 5(b). The isolation between the two outputs is more than 23 dB which is better than the simulated one. From Fig. 5(c), the third harmonic signal at 9.6 GHz is suppressed and the suppressed level is 26 dB which is better than the simulated result because the author has taken into account the frequency deviation in simulation software.

4. CONCLUSION

A novel compact power divider with third harmonic suppression and dc path is proposed in this paper. The size is 80% of the conventional one and this can benefit the miniaturation of the feed network for the antenna array. The third harmonic suppression is good to reduce the external interference and the dc path also can save the area for the active circuits application. From the measured results, the simulation is good to guide the practical fabrication.

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