9.5 GHz 16 λ_g DELAY LINE USING MULTILAYER LTCC

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Abstract—A fabricated multilayer low-temperature co-fired ceramic (LTCC) delay line (approximate $16\lambda_g$ at 9.5 GHz), using 3D meander strip line, is proposed in this paper for the first time. The advanced quasi coaxial ground vias (QCOX-GND vias) are proposed for signal vertical interconnections in this multilayer structure. These technologies obtain good performances in the whole band (9 ~ 10 GHz). Measurement results show that, besides low insertion loss and low VSWRs, low time dispersion can be achieved as $\leq \pm 0.002$ ns, which is very important to a delay line. The more compact size, as $8 \text{ mm} \times 10 \text{ mm} \times 2.37 \text{ mm}$, can also be obtained than other delay line structures.

1. INTRODUCTION

Microwave delay lines have been widely used in many applications such as radar and phased array systems. Recently, the key issue of the implementation of a compact module has been in reducing the cost and size of these applications [1]. There are many kinds of delay lines: optical delay lines, magnetostatic wave delay lines, surface acoustic wave delay lines, HTS transmission lines delay lines, and left-handed transmission lines delay lines [2–6]. Disadvantages of delay lines mentioned above, such as big size, narrow band, worse transmission loss and complex environment conditions, limit their applications in a small size, high performance and high reliable system. The multilayer low-temperature co-fired ceramic (LTCC) technology has emerged as an attractive solution of these problems. The high-precision threedimensional (3D) integration capabilities of multilayer LTCC are a

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very good option for making size-reduction and low-cost design, and also with low loss characteristics at high frequency. As commonly known, the dispersion of strip line using in multilayer LTCC is better than other planar transmission lines, for its propagation of TEM mode, which is a critical point for delay line design.

Nevertheless, few researches deal with 3D meander strip line delay line structures using multilayer LTCC integrally. The only literature concerns about that [7] just provides simulation results.

In this paper, for the first time, 3D meander strip line based on multilayer LTCC is used to design and fabricate an X-band delay line. The delay length of this delay line is approximate $16\lambda_g$, at the center frequency 9.5 GHz and within band 9~10 GHz. Section 2 describes design details about this $16\lambda_g$ delay line, including measured data. As we will see, 3D meander strip line based on multilayer LTCC presents good potential for designing small size delay line with low return loss and time dispersion.

2. DESIGN AND MEASUREMENT

One of the important reasons for using 3D meander strip line based on multilayer LTCC to design delay line is that it can realize enough delay length in limited area. The substrate material used in this design is Ferro A6 ($\varepsilon_r = 5.9$, $\tan \delta = 0.002$), with silver/gold conductors. Theoretical analysis shows that $16\lambda_g$ (5760 degree) delay length at 9.5 GHz based on strip line embedded in Ferro A6 substrate is about 208 mm. The area of 2D planar meander strip line structure achieving this length is too big to be acceptable in practical applications. Four

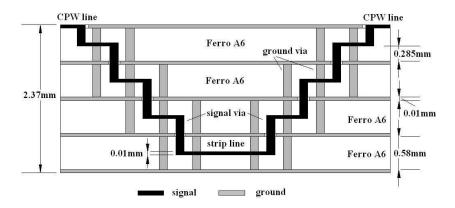


Figure 1. The sketch map of substrate layers structure of $16\lambda_g$ 3D meander strip line delay line using Ferro A6 with silver conductors.

substrate layers are used to construct 3D meander strip line in this design, as shown in Figure 1. 10 µm-thick conductors are embedded in the middle of each 0.58 mm-thick substrate layer, which is made of six 100 µm-thick layers (before co-fired). The thickness of single substrate layer has been optimized. The reduction of thickness will worsen electronic performance, especially the insertion loss. And the width of strip line with 50 Ω characteristic impedance is too small to be fabricated in thin substrate. The adopted thickness is a trade-off between theoretical performances and practical applications.

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Figure 2 shows the 3D structure of the whole $16\lambda_g$ delay line. The strip line in each substrate layer is constructed in meander configuration. The width of strip line is w, and the distance between two adjacent strip lines is g. The vertical interconnections between different conductor layers are round vias (signal vias and ground vias), with the diameter r. In order to obtain good impedance matching, coplanar waveguides (CPW) are used as surface transmission line for input/output ports. For the same reason, an advanced quasi coaxial ground vias (QCOX-GND via) is proposed for signal vertical interconnections, whose outer radius is t, and the angle between two

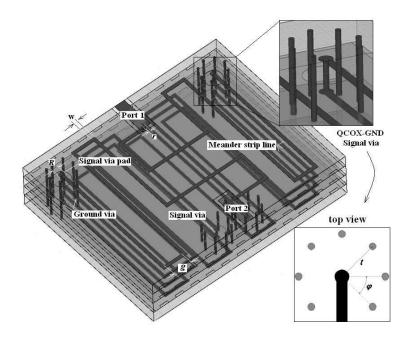


Figure 2. The 3D structure of the whole $16\lambda_g$ multilayer LTCC meander strip line delay line.

adjacent ground vias is φ , as shown in Figure 2. Reformed from equation of the coaxial transmission line, Equation (1) can be used to calculate initial values of dimensions of this proposed signal via, where Z_0 is the characteristic impedance of strip line.

As known, the crosstalk occurs between the unit lines in the meander strip line, discontinuities of QCOX-GND signal vias and dimensions of strip line and CPW will all affect the dispersion and transmission/reflection performances of delay line. For relevancy of these factors, global optimization should be executed to obtain acceptable performance and minimal space. 3D electromagnetic simulator (HFSS of Ansoft) is used to achieve this purpose. The distance between two adjacent strip lines is the most important parameter affecting the performance. Increasing it would decrease the crosstalk, but break the planar area limitation. The process of optimization is a trade-off between the performance and the size. After optimization, the final dimensions for fabrication are followings: $w = 0.15 \text{ mm}, r = 0.1 \text{ mm}, t = 0.6 \text{ mm}, \varphi = 45^{\circ}$. In different substrate layer, q is different. For process tolerance, the signal via pad is larger than the signal via, with the diameter $R = 0.2 \,\mathrm{mm}$. Final dimensions are $8 \text{ mm} \times 10 \text{ mm} \times 2.37 \text{ mm}$. Dimensions of CPW ports are shown in Figure 3. Optimization results are given in Table 1.

A flexible test fixture with SMA connectors is fabricated for

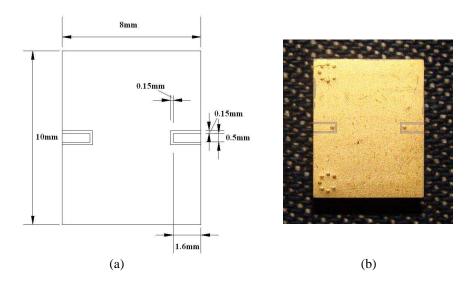


Figure 3. (a) Dimensions of surface CPW ports, (b) Photograph of $16\lambda_g$ multilayer LTCC delay line.

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Frequency (GHz)	9.1	9.5	9.9
Phase delay	5516.25	5760.39	6004.34
(degree)	(5517.5)	(5760)	(6002.5)
Insertion loss (dB)	-3.89	-3.94	-4.09
VSWR 1/2	1.32/1.28	1.25/1.21	1.27/1.31

Table 1. Optimization results of $16\lambda_g$ delay line.

Numbers in brackets are the phase delay of $16\lambda_g$ ideal delay line



Figure 4. Photograph of $16\lambda_g$ multilayer LTCC delay line with the test fixture.

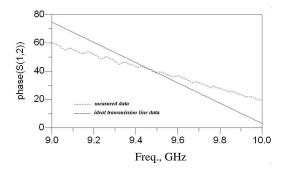


Figure 5. Comparison of phase delay between measured data and simulation data of ideal transmission line.

measurement, as shown in Figure 4. Measurements have been done with an Agilent E8363B vector network analyzer. The key problem of measurement is to remove the dispersion of discontinuities of joints accurately. In order to achieve this purpose, this delay line was replaced by a section of 50Ω standard CPW transmission line with the same length (8 mm). Figure 5 shows the comparison of phase delay between measurement and simulation data of ideal transmission line. Because dispersions of CPW line and coaxial connector are negligible, comparing this measured phase delay with simulated ones of ideal transmission line without dispersion, the dispersion of discontinuities of joints could be extracted, as the phase difference between both mentioned above.

The measured data are shown in Figure 6; the insertion loss is about $-4.7 \,\mathrm{dB} \sim -5.9 \,\mathrm{dB}$; and VSWRs for two ports are less than 1.5. All these data include the effect of the test fixture, which means better performances can be obtained without the test fixture. The known dispersion of discontinuities of joints can be subtracted from original

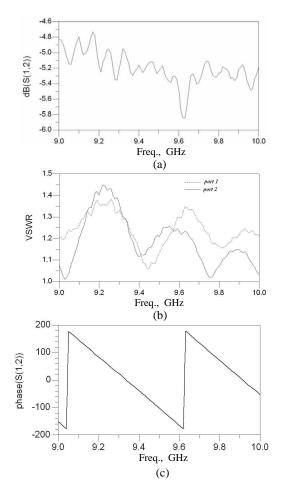


Figure 6. Measured (a) insertion loss (b) VSWRs and (c) phase delay of $16\lambda_g$ multilayer LTCC delay line with the test fixture.

phase delay data, which is shown in Figure 6(c). By the following simple equation (2), the time delay can be calculated. From results of the calculated time delay without the dispersion of discontinuities of joints for 11 frequency points (9~10 GHz, with step 0.1 GHz), as shown in Figure 7, the time dispersion of the $16\lambda_g$ multilayer LTCC delay line $\leq \pm 0.002$ ns in the whole band.

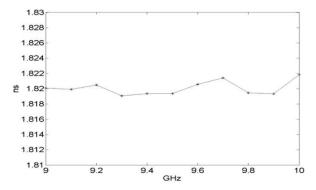


Figure 7. Calculated time delay of $16\lambda_g$ multilayer LTCC delay line with the test fixture.

3. FORMULATIONS AND EQUATIONS

$$t = \frac{r}{2} \times e^{\frac{Z_0 \sqrt{\varepsilon_r}}{60}} \tag{1}$$

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$$Timedelay = \frac{Phasedelay}{2 \times \pi \times freq}$$
(2)

4. CONCLUSION

In this paper, a very compact delay line is presented, with delay length approximate $16\lambda_g$ (9.5 GHz), which is designed and realized by 3D meander strip line with multilayer LTCC for the first time. Some technologies, such as QCOX-GND vias and CPW, are used to reduce the dispersion and achieve impedance matching. From measured results with the test fixture, good transmission/reflection performances can be observed. After removing effects of discontinuities of joints between delay line and the test fixture, low time dispersion performance can be obtained from measured data, which is a key factor to delay lines. Theoretically, the measurement comparison between the test fixture with the proposed delay line and the same test fixture with 0° delay CPW line could extract the original performance of the proposed delay line. But in practical measurement, it is very difficult to obtain accurate results of the test fixture with 0° delay CPW line now. Our future works will focus on achieving this purpose. Because of low VSWRs, low time dispersion and high compactness, multilayer LTCC technology could be a good alternative compared with other technologies for delay line, by using its 3D potential. It allows to design original and compact structures with great electrical performances.

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