Progress In Electromagnetics Research, PIER 90, 31–49, 2009

SYSTEM LEVEL INTEGRATION OF SIMULATION METHODS FOR HIGH DATA-RATE TRANSMISSION CIRCUIT DESIGN APPLICATIONS

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Abstract—A system level integration of simulation methods for high data-rate transmission circuit design applications is developed in this paper. While the elementary circuit theory was responsible for designing the circuits to meet the required performance specifications, three dimensional full-wave electromagnetic simulation technique was adopted to characterize the off-chip parasitic effects induce from the packages. The developed technique was applied for the design of optical Pick-Up Head (PUH) driver circuitry and a data transmission rate up to 640 Mega bits per second (Mb/s) was achieved with standard 0.35 μm CMOS technology, showing the promising feature of applying such technique in successful design for high data-rate transmission circuits.

1. INTRODUCTION

The dramatically-increasing processing speed of microprocessor motherboards, optical transmission links, intelligent hubs, etc., is pushing the off-chip data rate into the gigabits-per-second range. Off-chip data rates have gained little benefit from scaling of silicon

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technology due to the excessive power consumption required to drive the impedance-controlled electrical interconnects, leading to an increase in costs related to packaging and thermal management. Moving off-chip data rate to the range of Gb/s-per-pin is beneficial since the traditional way to realize high data rates was achieved by massive parallelism with increased complexity and cost for the IC package and the printed circuit board (PCB) [1, 2]. Besides, reduction of power is always desired for systems to relieve the extra costs related to packaging incurred by thermal management.

As the flexibility and performance of chips continue to increase, the output driver circuits will play an important role on off-chip data transmission. Fig. 1 shows the block diagram of off-chip interface circuitry. For the case in PUH interface applications, different transmission speed of data/clock is required under different recording/reading speed while accessing Laser-Diode Driver (LDD) circuitry inside PUH through flat-ribbon cables. Therefore, output driver needs to transmit different rate of data based on user's commands. Conventional Tri-state buffer can serve for off-chip transmission speed below 100 MHz with the benefits of zero static power consumption. However, for higher speed data transmission, Tri-state buffer suffers severely from performance degradations due to LC-bouncing and reflections due to impedance mismatch. Such problems can be solved using Low-Voltage-Differential-Signaling (LVDS) technology which was developed in order to provide a low-power and low-voltage alternative [3, 4] to other high-speed I/O

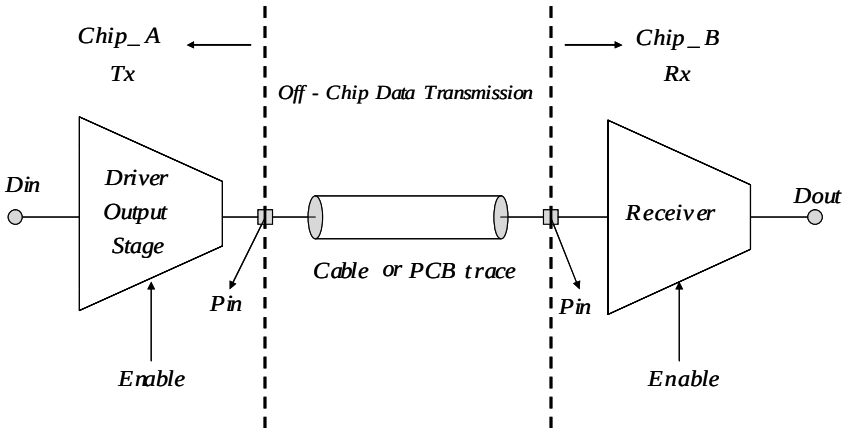


Figure 1. Block diagram of off-chip data transmission interface circuit.

interfaces. LVDS achieves significant power savings by means of a differential scheme for transmission and termination with a low voltage swing.

While concentration has been put on the novelty of circuit design topologies to achieve high data rate transmission, accurate characterization of the parasitic effects induced by the output bonding pads of the driver stage, bonding wires, package lead-frames, and signal traces on PCB is also required. The reason being that these chip-level interconnecting structures will contribute to the reactive part of the termination impedances loaded to the chips, especially when the transmission rate is high (for example, 600 Mb/s data rate with a 0.25 ns rise time clocked signal corresponds to approximately 1.4 GHz of operation). Moreover, the existence of the reactive impedance caused by the discontinuities will also cause excess unwanted signal reflections and possible resonances as the output stage drives the clocked signal through the off-chip interconnections.

Conventionally, equivalent circuit extraction technique [5–11] is adopted to model the behavior of interconnections at high frequencies. S-parameters of the interconnections with fundamental mode of excitation are firstly evaluated followed by numerical optimization routines to match the frequency response of the equivalent network. Though this method seemed to be straightforward, special attention must be paid on the effective bandwidth of the equivalent network. With higher and higher packaging density desired, complicated coupling schemes (such as RF to DC coupling or coupling between signals with different clock rates) are expected to exist among the interconnections. Furthermore, higher-order modes of propagation may also easily be excited by the discontinuities. Thus, how to derive adequate equivalent networks that can take care of the wideband feature and rather complicated coupling schemes at the same time has casted very challenging tasks on the conventional approaches [12–18].

In this paper, system level integration of simulation methods for high data-rate transmission circuit design applications is proposed. In addition to the proposed novel switching-mode output driver circuitry according to data transmission speed to reduce the DC power consumption, full-wave electromagnetic (EM) characterization of the interconnections were performed to address the bandwidth and complicated coupling issues among the tightly-spaced traces. Similar to the concepts of the hybridization methods proposed in solving complex electromagnetic propagation problems [19], the proposed approach provides a seamless integration of EM simulators (accounting for the high frequency behaviors of the interconnections) and circuit level simulators (accounting for the specified electrical functionalities).

To be specific, the results obtained from EM simulators serve as the corresponding boundary conditions which are equivalent to the accurate terminations of the circuit level simulators. Numerical example is presented to demonstrate the utilization of the proposed system level integration approach.

2. IMPLEMENTATION STRATEGIES

Figure 2 illustrates the basic implementation flow chart of the proposed system level integration algorithm. With the completion of the landscaping for the footprints of bonding pads, the estimated overall chip size and tentative bonding plan can be determined. Note that relative dimensions in the ball park are good enough at this stage since the electric design of the circuit has not been performed yet. Based on the preliminary dimensions of the footprints, selection of the package type (e.g., QFN, QFP, etc.) is readily completed with detailed information such as dimensions and material properties of the lead frames specified.

In order to have an accurate model for the package over the desired operation bandwidth (which should usually be very broad due to high data rate of transmission), the detailed 3D physical model of the package including the lead frames, the die attachment soldering and the molding compound will be constructed or imported into the full-wave electromagnetic simulator for analysis. The simulation tool used for presented analysis is CST Microwave Studio [20] which is mainly based on the Finite Integration in Time Domain (FIT) algorithm. The reason for adopting time domain simulator lies in the fact that for certain application scenarios, truly transient clocked signal which can not be possibly represented by analytical expression is used as excitation. In such cases, steady state frequency domain analysis through Fourier Transform techniques may not be adequate since the accuracy of the results depends strongly on the sampling rate especially for high clock rate signals. Additionally, time domain solvers show overwhelmingly efficiency over frequency domain solvers for analysis of complex structures at high frequencies since there are no inversions of matrices involved.

As the spectral content of the signal becomes higher with more complicated structures involved for simulation, more complex electromagnetic models are required to assess the very complicated couplings in between the structures at high frequencies. As a consequence, obtaining an accurate equivalent circuit over the band of operation is quite challenging since substantial increase in simulation effort is expected. To efficiently derive an accurate model that

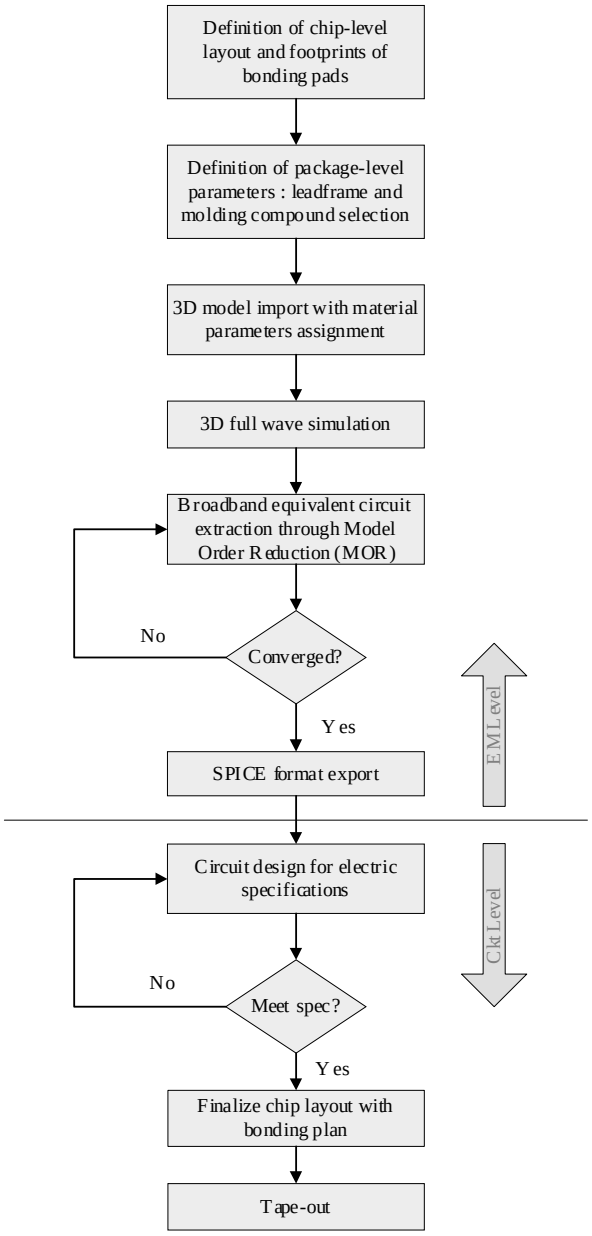


Figure 2. Implementation flow chart of the proposed system level integration algorithm.

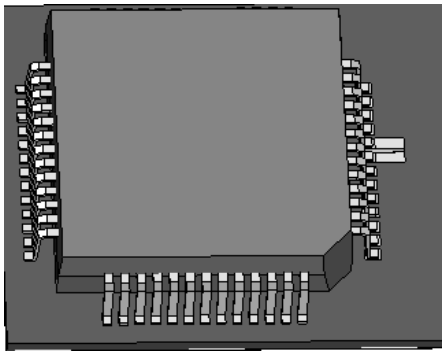
accounts for all the possible couplings at high frequencies, Model Order Reduction (MOR) technique is adopted in our approach. In order to make sure the correctness of the converged results representing the original responses of the package, issues related to the inclusion of eigenvalues and passivity are carefully taken care of [21]. SPICE compatible equivalent circuit based on such MOR technique which ensures passivity is exported directly once the desired level of convergence is reached. The extracted package model will in turn serve as the proper load terminations for circuit level design, analysis and optimization. Design iterations may be necessary with the fixed load termination in circuit simulator to guarantee the compliance of the electric specifications before final chip layout and bonding plan can be finalized.

3. DESIGN EXAMPLE

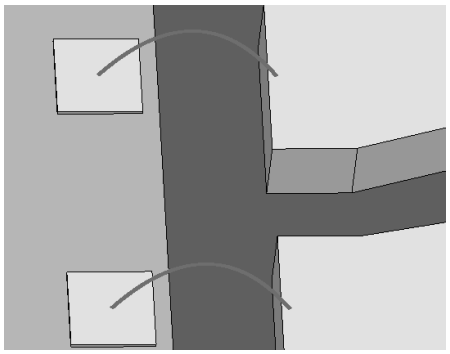
3.1. Electromagnetic Level Simulation

The proposed algorithm was applied to the design of novel switching-mode output driver circuitry for high-speed data transmission. While standard 3.3 V 0.35 μm CMOS technology was targeted for real implementation, the design goal was to achieve an off-chip data transmission rate of up to 640 Mbits per second. In this specific design example, the full-functionality chip was in tended to be housed in QFN package with 13 pins on each side using standard IC packaging process. Fig. 3(a) shows the imported 3D complete structure for electromagnetic simulation. Note that the bond wires were also included for simulation as shown in the enlarged plot in Fig. 3(b).

With the imported 3D model, the excitation source was assigned in one of the pairs and differential mode excitation mode was adopted. Though only one of the pairs were used as the excitation, the whole lead frame and the printed circuit board with a pair of transmission lines were included for simulation to accommodate for all the possible couplings to other areas through the down-set and common ground of the differential traces. For better signal integrity consideration, the 100 Ω termination between the differential traces was also included in the simulation. As is mentioned in the previous section, the choice of time domain has the key advantage of using truly time-domain transient signals as the excitation source to accurately characterize the electromagnetic response of the associated package. Moreover, to characterize the package completely, the frequency range of interest should cover at least twice the highest frequency component involved in the time signal. The reason being that in a lot of applications, mixed-mode operation is desired. Under such circumstances, complicated



(a)



(b)

Figure 3. (a) The complete 3D model for electromagnetic simulation; and (b) enlarged plot of (a) showing the inclusion of the bond wires for simulation.

coupling schemes such as coupling through multiples of fundamental frequencies are expected. Thus, electromagnetic analysis at such high frequency region is absolutely necessary to guarantee the complete assessment of the possible existing couplings.

To examine the effect of signal rise time (and thus the highest frequency spectrum contained in the signal) on the possibly unwanted high frequency coupling in the vicinity of the excitation source, the two-dimensional surface current distribution at 10 GHz is plotted in Fig. 4. Note that in order to have reasonable comparison, the peak current density has been normalized to the same value of 50 A/m. It is clear seen that as the rise time decreases from 20 psec (Fig. 4(a)) all the way down to 5 psec (Fig. 4(d)), the signal confinement as a differential mode becomes worse and worse. Meanwhile, severe coupling evidenced

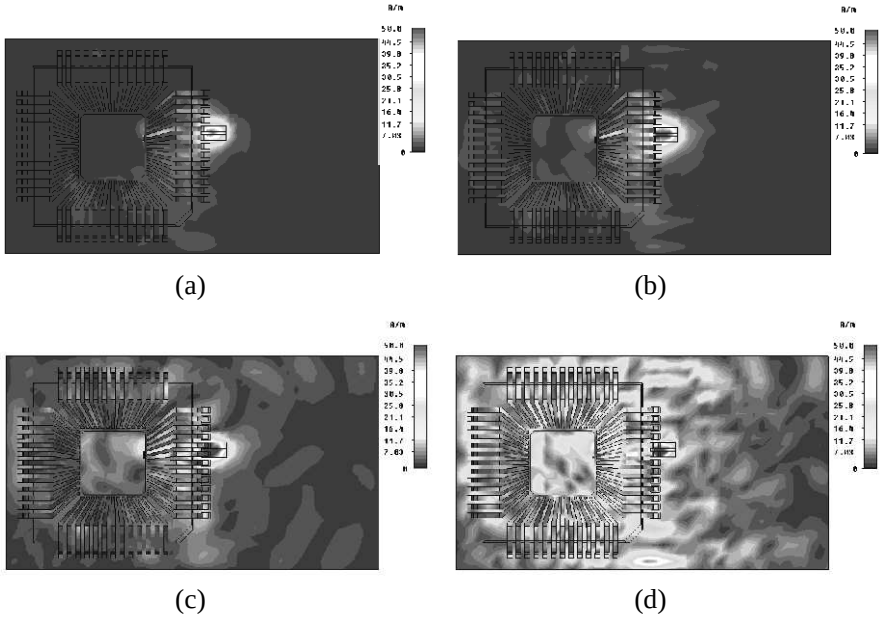
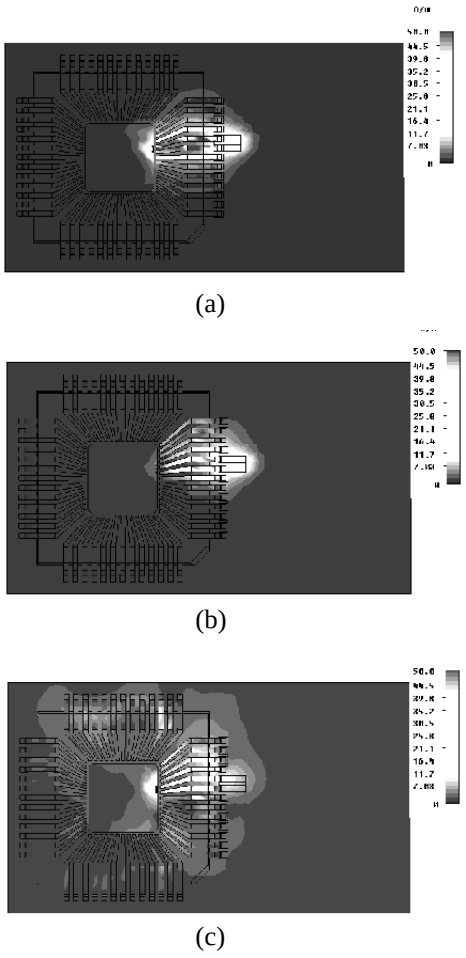


Figure 4. Two-dimensional surface current distribution at 10 GHz plotted with various signal rise time: (a) 20 psec, (b) 15 psec, (c) 10 psec, and (d) 5 psec.

by the spotty locations with large values of current densities existing all over the area of interest was observed at the extreme case when the rise time was 5 psec. Such unwanted coupling characterized by very large localized currents certainly causes fluctuations in the system impedance which in turn deteriorates the overall signal quality of the system especially under high data rate of transmission. Same surface current density distributions were plotted against different frequency with the same excitation signal of 20 psec rise time in Fig. 5. It is observed, as expected, that the above mentioned effect certainly becomes pronounced at higher frequencies.

Since our design target was set as an off-chip transmission rate of 640 Mbits per second, a broadband signal (in the sense of the frequency component composed in the time signal) up to 10 GHz was used as the excitation source. Model Order Reduction (MOR) technique with a total number of thirty poles was adopted for equivalent circuit extraction over such a wide band of operation. With passivity enforced for all the frequency values, the resultant equivalent circuit was exported as SPICE compatible differential netlist for the purpose of



(a)

(b)

(c)

Figure 5. Two-dimensional surface current distribution with excitation signal of 20 psec rise time with various frequencies: (a) 1 GHz, (b) 5 GHz, and (c) 10 GHz.

further circuit simulation. Fig. 6 shows the comparison between the corresponding S-parameters of the extracted circuit model and that obtained from the direct electromagnetic analysis. An accuracy level of 1.00E-06 was achieved.

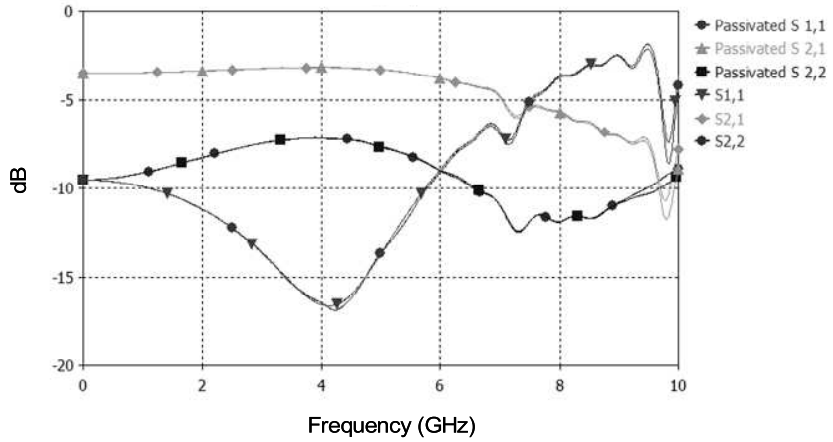


Figure 6. Comparison of the S-parameters between the extracted ones and those obtained from electromagnetic simulation.

3.2. Circuit Level Simulation

In terms of circuit level simulation, novel circuitry including LVDS-mode driver, Tri-state-mode driver, and switching control circuitry were proposed. With the accurate load impedance obtained from the EM level simulation, the proposed output circuitry features extremely high level of flexibility in a sense that the users have the freedom of switching over different modes based on the required transmission rate required by the system.

3.2.1. Circuit Design of LVDS Driver with switching Control

Figure 7 illustrates the schematic of proposed LVDS driver with switching control. With a 100 ohm termination resistor at receiver end, the output voltage of the LVDS type should satisfy the definition made by LVDS standard as follows:

$$\begin{aligned} 250\,\mathrm{mV} \le |V_{od}| \le 450\,\mathrm{mV} \\ 1.125\,\mathrm{V} \le V_{\mathrm{cm}} \le 1.375\,\mathrm{V}, \end{aligned} \tag{1}$$

where V_{od} and V_{cm} represent output differential voltage and output common mode voltage, respectively. As shown in Fig. 7, when LVDS driver is activated, "*lvds_en*" should be set to "high". The output

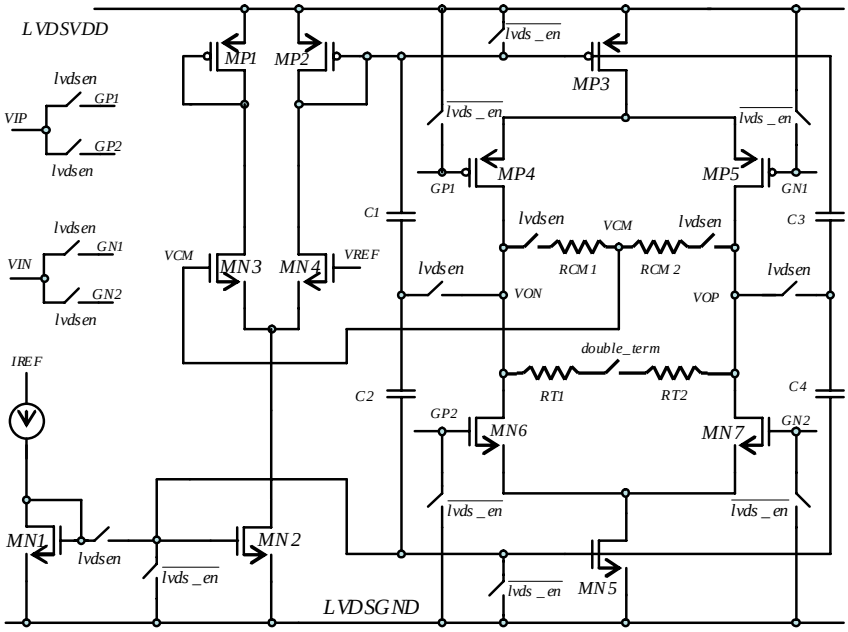


Figure 7. Circuit implementation of LVDS type output driver.

current mirrored by (*MN2-MN5*) can be decided by

$$I_{MP3} = I_{MN5} = I_{ref} * \frac{\left(\frac{W}{L}\right)_{MN5}}{\left(\frac{W}{L}\right)_{MN2}} \tag{2}$$

Besides, the differential output signal V_{od} is defined as:

$$V_{od} = I_{MP3} \cdot [(R_{T1} + R_{T2}) \,//\, R_{TR}] \tag{3}$$

where R_{T1} and R_{T2} are termination resistors shown in Fig. 7 and R_{TR} is the termination resistor at receiver end. The output common mode voltage *Vcm* is detected by *RCM1* and *RCM2*. Also, the detected voltage *Vcm* will be compared with *VREF*, and stabilized at *VREF* set at 1.25 V through common-mode feedback circuitry formed by *MN2*, *MN3*, *MP1*, *MP2*, and*MP3*. Capacitors $C1$–$C4$ are added to guarantee enough phase margin of common-mode feedback loop. The nodes *Vop* and *Von* here are both in high-Z state when "*lvds_en*" = "low".

3.2.2. Circuit Design of Tri-State Driver with switching Control

Figure 8 illustrates the schematic of proposed Tri-State driver with switching control. For the lower speed data transmission application

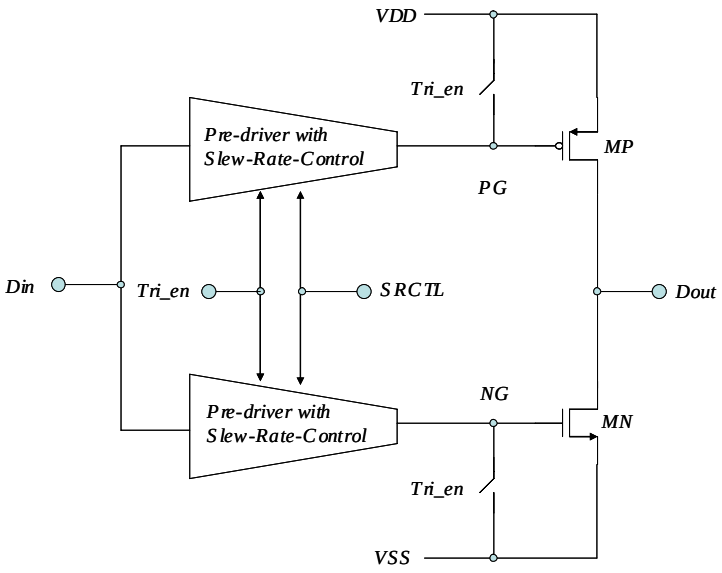


Figure 8. Circuit implementation of Tri-state output driver.

(frequency below 100 MHz), Tri-State buffer can be activated by setting "*Tri_en*" to be "high". As can be seen from Fig. 8, there is no DC path from Vdd to Vss when Tri-state buffer is activated regardless of the polarity of Din. The pre-driver can be designed with output slew rate control (*SRCTL*) functionality to reduce the off-chip signal ringing.

3.2.3. Circuit Design of Novel Switching-Mode Driver

To implement the novel switching mode output driver, we have to merge LVDS-mode driver and Tri-State driver together with proper switching control. Fig. 9 illustrates the block diagram of LVDS-mode driver and Tri-State driver, respectively. Fig. 10 shows the schematic of proposed novel switching mode output driver according off chip transmission speed. Under lower data rate of transmission (below 100 MHz), we set "*lvds_en*" to be low; Tri-state buffer is thus activated whereas LVDS-mode driver is kept in high-Z state. For high speed data transmission application with "*lvds_en*" setting to be "high", LVDS mode driver is thus activated whereas Tri-state buffer kept in high-Z state. With the help of this novel switching mode output driver, users can transmit lower speed data/clock with zero static power consumption and high speed data/clock (640 Mb/s with cable length as long as 12 cm) with good signal integrity.

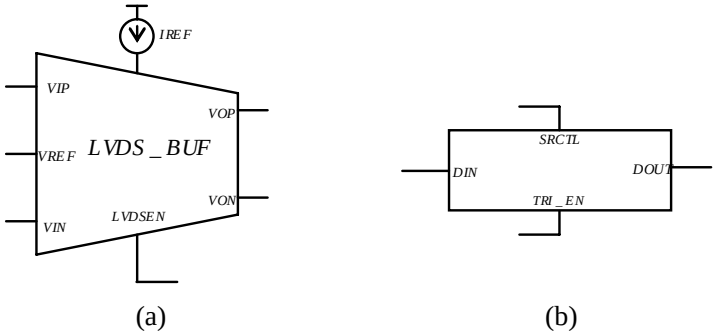


Figure 9. Block diagram of (a) LVDS driver and (b) Tri-state driver.

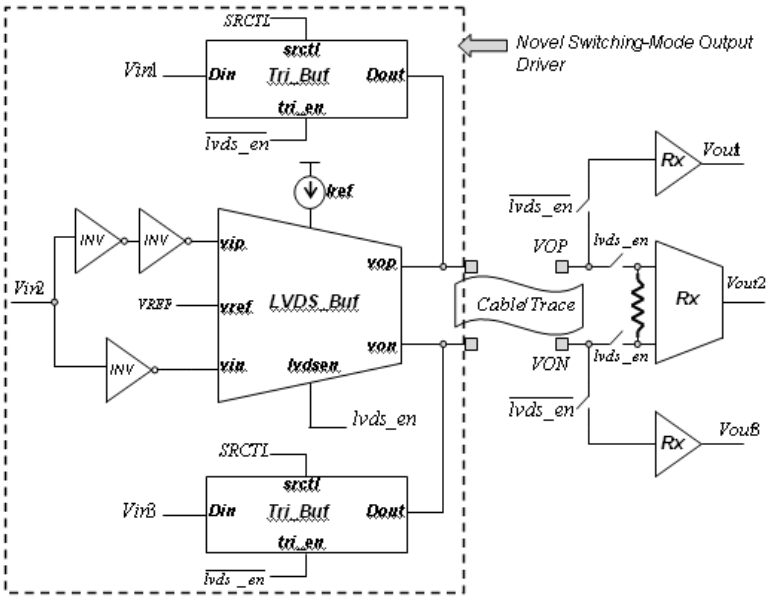


Figure 10. Circuit implementation of proposed novel switching-mode output drive.

4. SIMULATION RESULTS

The proposed novel switching mode output driver has been implemented by 0.35 µm 3.3 V CMOS process and simulated by HSPICE. For the accuracy of off-chip data transmission, the equivalent circuit model of package and connector obtained from the full-wave

electromagnetic simulation has been included in the simulation set up. Besides, the cable/PCB trace has been modeled with a 12 cm long transmission line and included in the simulation. Complete simulation of off-chip data transmission was carried out according to the topology shown in Fig. 10. The differential outputs are probed at the far-end of cable/PCB trace.

Figure 11 demonstrates the simulation results of proposed output driver with "*lvds_en*" switching to high state when the input NRZ data rate is up to 640 Mb/s. The amplitude of the output differential signal $|V_{OP} - V_{ON}|$ is about 350 mV and the rising/falling time (t_r/t_f) of the differential signal is 0.5 ns. The power consumption (P_d) of output driver when "*lvds_en*" setting to be high is 26.4 mW.

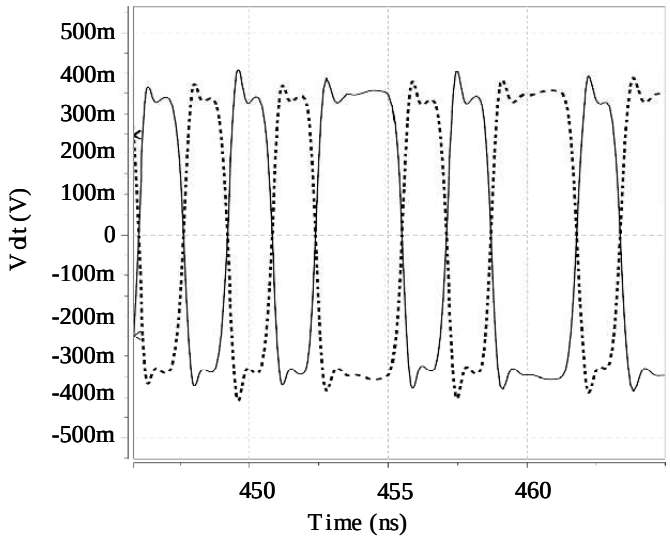


Figure 11. Simulation results of proposed output driver when switching to *lvds_en* = "high" and transmitted data rate up to 640 Mb/s.

To investigate the proposed circuit performance versus the variation on temperature, power supply voltage, and process, corner case analysis has been performed. Fig. 12 demonstrates the corner case simulation results of the differential output signal $|V_{OP} - V_{ON}|$ of proposed output driver with "*lvds_en*" setting to high. Three cases, the best, typical, and worse were analyzed with corresponding bias settings and operating temperatures according to the definitions of LVDS standard. It can be seen that the timing variation of the differential output signal across reference level ($V = 0$) is about 200 ps.

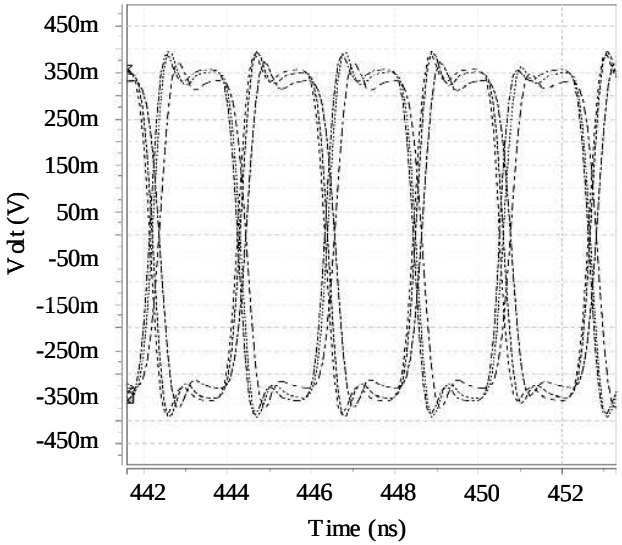


Figure 12. Corner case (worst, typical, and best) simulation results of proposed output driver when *lvds_en* = "high".

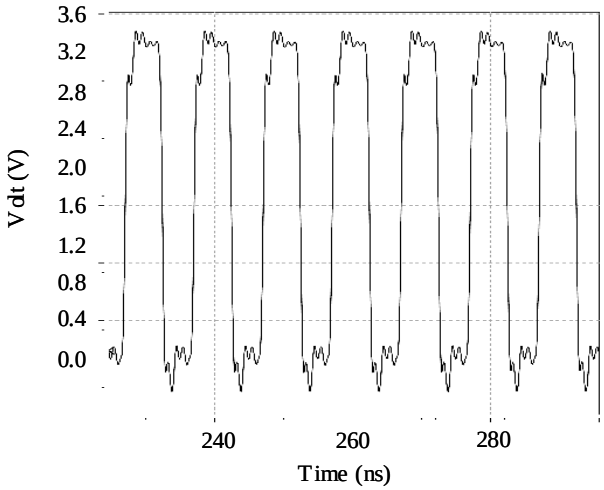


Figure 13. Simulation results of proposed output driver when switching to *lvds_en* = "low" and transmitted data frequency up to 100 MHz.

Figure 13 shows the simulation results of proposed output driver with "*lvds_en*" setting to be "low" when off-chip data transmission frequency is up to 100 MHz. It can be seen that under this mode

of operation, the output signal (*Vop/Von*) swing is as high as 3.3 V with zero DC power consumption. Complete package model obtained from EM level simulator and cable/PCB trace transmission line model are also included in this simulation. Fig. 14 illustrates the output voltage *Vop*, *Von* and common mode voltage *Vcm* of the proposed novel switching-mode output driver when "*lvds_en*" setting to be high. With the CMFB (common-mode feedback) circuitry shown in Fig. 7, the output common-mode voltage *Vcm* has been shown to be set at about 1.25 V. The HSPICE simulation results and performance of proposed novel output driver were summarized in Table 1.

Table 1. Summary of the simulated results of the proposed circuitry.

	Proposed Driver with *lvds_en*="high"	Proposed Driver with *lvds_en*="low"
Mode of operation	LVDS Buffer Activated	Tri_ State Buffer Activated
Signal Swing	320 mV ∼ 380 mV	3.3 V
Output common-mode	1.25 V	none
DC power Consumption	26 mW	0
Suitable data rate/freq of transmission	Up to 640 Mb/s	Below 100 MHz

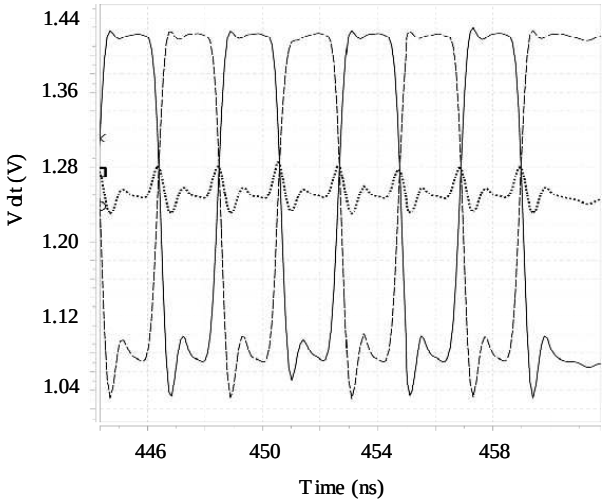


Figure 14. Simulation results of output common-mode voltage (center dotted line) when output driver switching to *lvds_en* = "high".

5. CONCLUSION

For the first time, system level integration of simulation methods consisting of full wave electromagnetic simulation and circuit level simulation was proposed and applied for the design of novel switching-mode output driver for off-chip data transmission using standard 0.35 µm 3.3 V CMOS process. While the effect of the package was accurately characterized by the EM level simulation, the extracted equivalent circuit model through MOR was adopted as the proper termination to the output load in the circuit simulator. Simulation results have been demonstrated proposed output driver with switching-mode can both transmit lower data rate/clock with zero DC power consumption and high off-chip transmission rate up to 640 Mb/s along 12 cm flat ribbon cable with good signal integrity. The proposed output driver also offers designer/users with high design flexibility and pin count saving while performing system integration.

ACKNOWLEDGMENT

The author H. S. Hsu would like to acknowledge the support from National Science Council of Taiwan, R.O.C. for this work under contract number NSC 97-2221-E-035-086.

REFERENCES

1. Chen, M., J. Silva-Martinez, M. Nix, and M. E. Robinson, "Low-voltage low-power LVDS drivers," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 2, 472–479, Feb. 2005.
2. Boni, A., A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s-per-pin operation in 0.35-µm CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 4, 706–711, Apr. 2001.
3. *IEEE Standard for Low-Voltage Differential Signaling (LVDS) for Scalable Coherent Interface (SCI)*, 1596.3 SCI-LVDS Standard, IEEE Std 1596.3–1996, 1996.
4. *Electrical Characteristics of Low-voltage Differential Signaling (LVDS) Interface Circuits, TIA/EIA-644*, National Semiconductor Corp., ANSI/TIA/EIA, 1996.
5. Wang, Y., J. Li, and L.-X. Ran, "An equivalent circuit modeling method for ultra-wideband antennas," *Progress In Electromagnetics Research*, PIER 82, 433–445, 2008.
6. Eshrah, I. A., A. A. Kishk, A. B. Yakovlev, and A. W. Glisson, "Generalized equivalent circuit model for transverse waveguide

slots and applications," *Progress In Electromagnetics Research*, PIER 69, 1–20, 2007.

7. Zheng, H.-X., X.-Q. Sheng, and E. K.-N. Yung, "Computation of scattering from conducting bodies coated with chiral materials using conformal FDTD," *Journal of Electromagnetic Waves and Applications*, Vol. 18, No. 11, 1761–1774, 2004.
8. Chen, X., D. Liang, and K. Huang, "Microwave imaging 3-D buried objects using parallel genetic algorithm combined with FDTD technique," *Journal of Electromagnetic Waves and Applications*, Vol. 20, No. 13, 1471–1484, 2006.
9. Yang, Z. Q., T. Yang, Y. Liu, and S. H. Han, "MIM capacitor modeling by support vector regression," *Journal of Electromagnetic Waves and Applications*, Vol. 22, No. 1, 61–67, 2008.
10. Xu, Y. H., Y.-C. Guo, R.-M. Xu, B. Yan, L. Xia, and Y. Q. Wu, "Modeling of SIC MESFETs by using support vector regression," *Journal of Electromagnetic Waves and Applications*, Vol. 21, No. 11, 1489–1498, 2008.
11. Mohammadi, F. A. and M. C. E. Yagoub, "Electromagnetic model for microwave components of integrated circuits," *Progress In Electromagnetics Research B*, Vol. 1, 81–94, 2008.
12. Hu, X.-J. and D.-B. Ge, "Time domain analysis of active transmission line using FDTD technique," *Progress In Electromagnetics Research*, PIER 79, 305–319, 2008.
13. Xiao, S., B.-Z. Wang, P. Du, and Z. Shao, "An enhanced FDTD model for complex lumped circuits," *Progress In Electromagnetics Research*, PIER 76, 485–495, 2007.
14. Kung, F. and H.-T. Chuah, "A finite-difference time-domain (FDTD) software for simulation of printed circuit board (PCB) assembly," *Progress In Electromagnetics Research*, PIER 50, 299–335, 2005.
15. Young, J. L. and R. Adams, "Excitation and detection of waves in the FDTD analysis of N-port networks," *Progress In Electromagnetics Research*, PIER 53, 249–269, 2005.
16. Chen, Z.-H. and Q. Chu, "FDTD modeling of arbitrary linear lumped networks using piecewise linear recursive convolution technique," *Progress In Electromagnetics Research*, PIER 73, 327–341, 2007.
17. Bernardi, P., R. Cicchetti, G. Pelosi, A. Reatti, S. Selleri, and M. Tatini, "An equivalent circuit for EMI prediction in printed circuit boards featuring a straight-to-bent microstrip line

coupling," *Progress In Electromagnetics Research B*, Vol. 5, 107–118, 2008.

18. Sabri, M. M., J. Rashed-Mohassel, and N. Masoumi, "Application of FDTD-based macromodeling for signal integrity analysis in practical PCBs," *Progress In Electromagnetics Research Letters*, Vol. 5, 45–55, 2008.
19. Chou, H.-T. and H.-T. Hsu, "Hybridization of simulation codes based on numerical high and low frequency techniques for the efficient antenna design in the presence of electrically large and complex structures," *Progress In Electromagnetics Research*, PIER 78, 173–187, 2008.
20. CST 2008 User's Manual, www.cst.com
21. Cangellaris, A. C., S. Pasha, J. L. Prince, and M. Celik, "A new discrete transmission line model for passive model order reduction and macromodeling of high-speed interconnections," *IEEE Transactions on Advanced Packaging*, Vol. 22, No. 3, 356–364, Aug. 1999.