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A SPICE COMPATIBLE MODEL OF ON-WAFER COUPLED INTERCONNECTS FOR CMOS RFICS

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Abstract—This paper investigates the properties of the on-wafer coupled interconnects built in a 0.18 µm CMOS technology for RF applications. A SPICE compatible equivalent circuit model is developed. The proposed model is an extension of a 2-Π equivalent circuit model for single-line interconnects by adding two coupling components. The model parameters are extracted from four-port S-parameter simulation results through a calibrated electromagnetic (EM) simulator, i.e., HFSS. The accuracy of the model is validated from 500 MHz to 20 GHz.

1. INTRODUCTION

Due to its fabrication cost advantage, CMOS technology has become a desirable choice for radio frequency integrated circuits (RFICs), especially for wireless consumer applications. With the ever-increasing operating frequency, chip size, circuit density and complexity, interconnects have become one of the crucial factors affecting the circuit performance [1]. Therefore, it is increasingly essential to consider the interconnect effect in an early stage of the RFIC design. As it is known, interconnect performance can be predicted by numerical electromagnetic (EM) simulations [2]. However, in-depth EM knowledge is required for using those EM simulators. SPICE compatible equivalent circuit models are much easier to handle and therefore are preferred by circuit designers [3].

In the literature, numerous reports on characterizations of single-line interconnects could be found. However, in a real case, the density of the interconnects is high and correspondingly the interconnect pitch is very fine. The crosstalk and proximity effects among

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interconnects must be taken into consideration [4]. Therefore, accurate, fast and robust models for coupled interconnects are also highly demanded. However, reports on coupled interconnects are limited [5]. In [6], four-port S-parameter measurement results were used to extract mutual and self RLC parameters of the asymmetric coupled lines. No equivalent circuit model was reported and the extracted parameters were frequency-dependent. In [7, 8], an equivalent circuit model with frequency-dependent components were described. A quasi-magnetostatic integral formulation approach was used for the computation of the component values. In [9], a framework with RLC components was proposed based on transmission-line theory. In [5, 10], multiple cascaded Γ-sections of RLCs were used to model the coupled interconnects. Values of the model components were extracted from two-port S-parameter measurements.

In this work, a SPICE compatible lumped equivalent circuit model is proposed to characterize the on-wafer coupled interconnects for CMOS RFICs based on the previously proposed 2-Π single-line interconnect model [11, 12]. Four-port S-parameter simulation results of a well-calibrated EM simulator, are used for parameter extraction and model verification of the coupled interconnects.

This paper is organized as follows: Section 2 presents the simulator calibration and simulation setup. Section 3 interprets the equivalent circuit model development. Section 4 lists the extracted parameters. Verifications are also presented. Finally, the paper is summarized and concluded in Section 5.

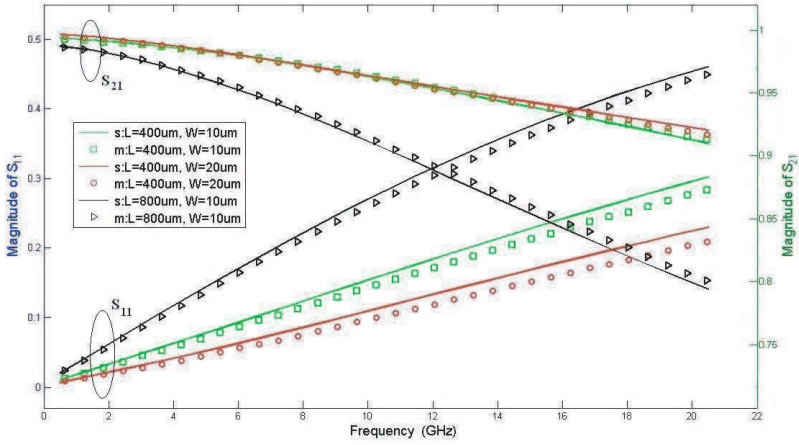
2. SIMULATION SETUP

The objective of interconnect modeling is to enable circuit designers to incorporate interconnect effects at an early design stage. Hence, over-design or excessive design iterations after tapeout could be prevented. Therefore, it is essential that the proposed model is with silicon-verified accuracy. There are mainly two ways to guarantee the required accuracy. The most straightforward way is to design and fabricate all the test structures. On-wafer measurements are then performed and the results are used for both model parameter extraction and model verification. However, it is extremely costly and time consuming of the fabrication process. An alternative way is to adopt an EM simulator and use several fabricated samples to calibrate that EM simulator. Then characteristics of other structures can be obtained by using that calibrated simulator [13].

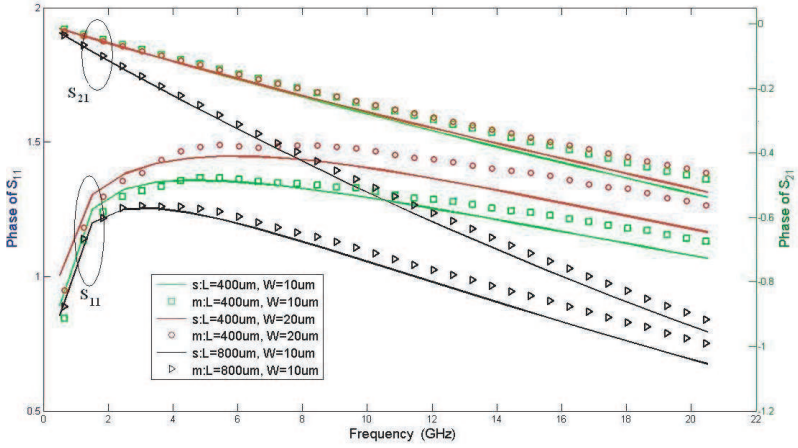
In this work, Ansoft's High-Frequency Structure Simulator (HFSS) is employed to perform the EM simulation. Several single-

line interconnect test structures have been fabricated in the top metal layer using a 0.18 μm RF CMOS process by Chartered Semiconductor Manufacture Ltd. (CHRT) [8]. The simulation environment of HFSS is set up according to that process.

In order to verify the accuracy of the settings of the EM simulator, i.e., HFSS, three sets of single-line interconnect test structures with



(a) Comparisons of the magnitudes

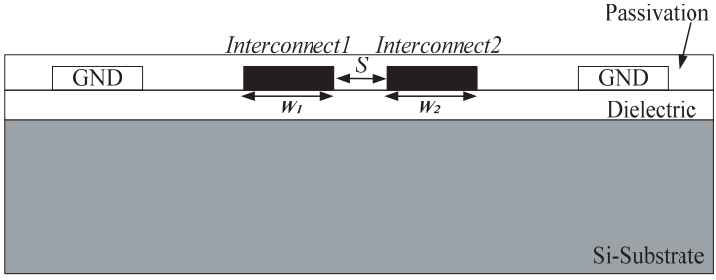


(b) Comparisons of the phases

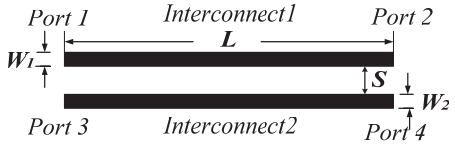
Figure 1. Comparisons between HFSS simulation results and on-wafer measurements.

different combinations of length (L) and width (W) have been examined. HFSS simulated S-parameters are compared with the corresponding on-wafer measurements from 500 MHz to 20 GHz. The comparisons are shown in Figure 1. The discrete squares, circles and triangles represent the measured S-parameters of the structures with $L = 400\,\mu m$, $W = 10\,\mu m$; $L = 400\,\mu m$, $W = 20\,\mu m$ and $L = 800\,\mu m$, $W = 10\,\mu m$, respectively. The solid lines represent the corresponding simulation results obtained by HFSS. It could be noted from Figure 1 that with appropriate settings, the HFSS is capable of characterizing the test structures with acceptable silicon-verified accuracy.

With the calibrated HFSS, coupled interconnect structures using the top metal layer, as illustrated in Figure 2(a), are simulated from 500 MHz to 20 GHz. Several physical dimension combinations of the coupled interconnects are examined. For each set of the structure, L of *Interconnect* 1 and *Interconnect* 2 are identical. It is 400 μm or 800 μm. W is 10 μm or 20 μm. The line spacing (S) varies from 1.5 μm to 10 μm. The width of the ground (GND) lines is fixed at 40 μm and the space between the two GND lines is fixed at 160 μm. The top view of the test structure and the assignment of the ports are illustrated in Figure 2(b).



(a) Cross-sectional view of the test structure



(b) Top view of the test

Figure 2. Illustration of the test structures.

3. MODEL DEVELOPMENGT

According to the physical configuration of the test structure as shown in Figure 2, a pair of coupled interconnects consists of two single-line interconnects. Therefore, the proposed equivalent circuit model of coupled interconnects is developed based on the single-line interconnect model.

3.1. Equivalent Circuit Model

The equivalent circuit model for single-line interconnects is shown in Figure 3. This 2-Π model is capable of characterizing frequency-variant high frequency effects, i.e., skin effect, substrate effect and distributed effect, with frequency-independent components. Details of the model can be found in our previous work [11, 12].

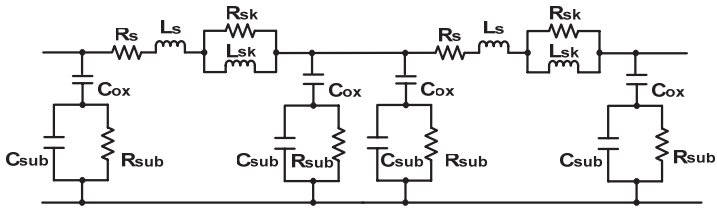


Figure 3. 2-Π equivalent circuit model of single-line interconnects.

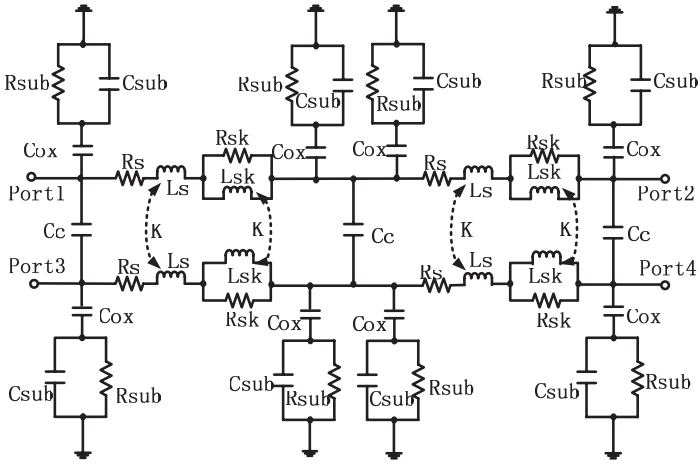


Figure 4. Equivalent circuit model of coupled interconnects.

A desirable model is accurate, physically meaningful and capable of maintaining the simplicity as much as possible. Thus, two more components are added to the single-line interconnect model to depict the coupling effect as shown in Figure 4. C_c is introduced to represent the coupling capacitance between the two interconnects through the oxide layer as well as air. Since the 2-Π model is used to model each single-line interconnect, a C_c is added to each node of the Π-sections to characterize the distributed coupling effect. Therefore, all together three coupling capacitors (C_c) are added between the two single-line interconnects. The mutual inductance coupling coefficient K is introduced to characterize the mutual inductance coupling. K indicates the strength of the magnetic coupling between two interconnects. Its value is in the range from 0 to 1.

3.2. Parameter Extraction

Based on the proposed equivalent circuit model in Figure 4, values of the model components could be extracted from the four-port HFSS S-parameters simulation results.

From Figure 4, the four-port S-parameters can be expressed as functions (Eqs. (1) to (4)) of the model components.

$$S_{11}(\omega) = f_1(\omega, L_s, R_s, L_{sk}, R_{sk}, C_{ox}, C_{sub}, R_{sub}, C_c, K) \quad (1)$$

$$S_{12}(\omega) = f_2(\omega, L_s, R_s, L_{sk}, R_{sk}, C_{ox}, C_{sub}, R_{sub}, C_c, K) \quad (2)$$

$$S_{13}(\omega) = f_3(\omega, L_s, R_s, L_{sk}, R_{sk}, C_{ox}, C_{sub}, R_{sub}, C_c, K) \quad (3)$$

$$S_{14}(\omega) = f_4(\omega, L_s, R_s, L_{sk}, R_{sk}, C_{ox}, C_{sub}, R_{sub}, C_c, K) \quad (4)$$

where ω is the angular frequency in radians.

Since the model is derived from the single-line interconnect model, values of the model components L_s, L_{sk}, R_{sk}, C_{sub} and R_{sub} can be calculated from the empirical equations in [11] and adopted in the coupled interconnect model directly. Due to the proximity effects, values of R_s and C_{ox} have to be modified, which is consistent with the report in [5]. Values of R_s and C_{ox} obtained from the empirical equations are used as the initial values.

Together with the four-port S-parameters obtained from the HFSS, the parameter extraction becomes a least square curve-fitting problem. The objective function F_0 can be derived as Eq. (5).

$$F_0 = \sum_{i=1}^{m} \left[(S_{11\_i\_HFSS} - f_{1\_i})^2 + (S_{12\_i\_HFSS} - f_{2\_i})^2 + (S_{13\_i\_HFSS} - f_{3\_i})^2 + (S_{14\_i\_HFSS} - f_{4\_i})^2 \right] \quad (5)$$

where m is the total number of frequency points under consideration, $S_{1x\_i\_HFSS}$ is the S-parameters obtained from HFSS at each frequency

point i and f_{x_i} is the corresponding S-parameters at frequency point i represented as functions of the model components. Considering the symmetry of the test structures, it is known that $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$. Therefore, only S_{11}, S_{12}, S_{13} and S_{14} are included in the objective function in Eq. (5).

The circuit simulation and the curve-fitting features, as well as the Levenberg-Marquardt [14] optimization algorithm provided by Agilent Advanced Design System (ADS) [15] are employed to acquire the optimized values of R_s, C_{ox}, C_c and K.

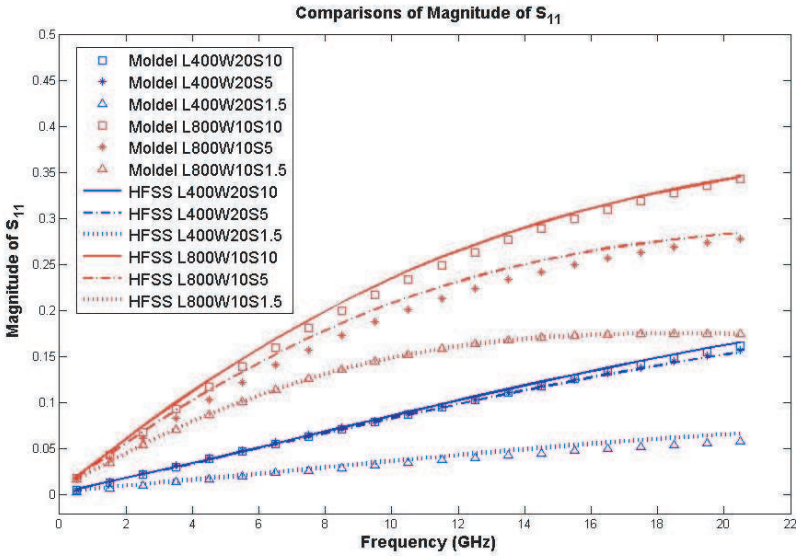
4. RESULTS AND VERIFICATIONS

With the extraction steps described in Section 3.2, extracted component values of nine pairs of coupled interconnects are summarized in Table 1.

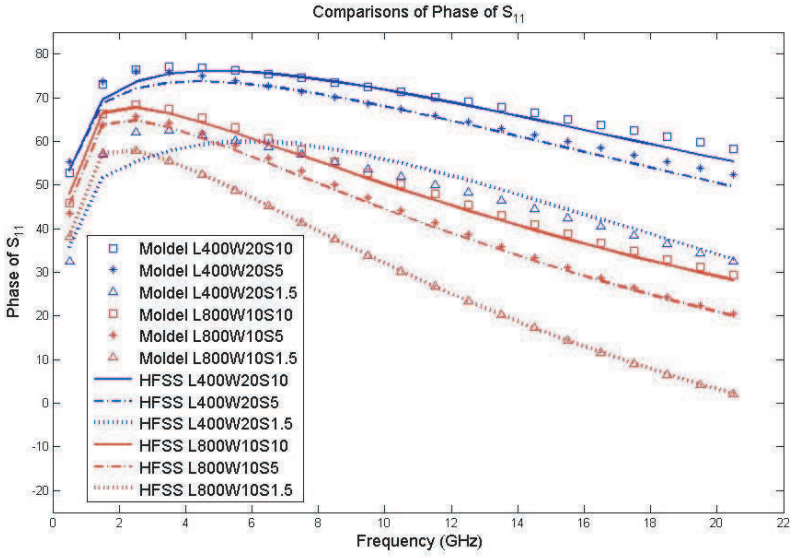
From Table 1, it could be observed that C_c is proportional to the length (L) and the width (W) of each single-line interconnect but reversely proportional to the space (S) between the two adjacent interconnects, which accords with our understanding of the definition of capacitors. It could also be noted that the mutual coupling coefficient K is proportional to the width (W), reversely proportional to the space (S), but independent of the length (L). This can be explained with the EM theory. As depicted in Eq. (6), K defines the portion of magnetic flux that is shared between the two coupled interconnects. In other words, $(1 - K)$ indicates the portion of the magnetic flux leakage. When $L \gg W$ and S, it will not affect the

Table 1. Extracted parameters of the coupled-line interconnect model.

physical dimension (μm)	*L*=800 *W*=10			*L*=400 *W*=10			*L*=400 *W*=20		
	S=1.5	*S*=5	*S*=10	*S*=1.5	*S*=5	*S*=10	*S*=1.5	*S*=5	*S*=10
R_s (Ω)	0.568	0.608	0.632	0.298	0.300	0.307	0.100	0.105	0.163
L_s (pH)	308.45	308.45	308.45	156.95	156.95	156.95	318.20	318.20	318.20
R_{sk} (Ω)	0.747	0.747	0.747	0.531	0.531	0.531	0.546	0.546	0.546
L_{sk} (pH)	18.207	18.207	18.207	8.647	8.647	8.647	8.020	8.020	8.020
C_{ox} (fF)	11.60	15.24	15.52	6.71	7.13	6.71	5.76	5.76	5.76
C_{sub} (fF)	20146	20.146	20.146	8.707	8.707	8.707	9.219	9.219	9.219
R_{sub} (Ω)	158.70	158.70	158.70	476.51	476.51	476.51	392.55	392.55	392.55
C_c (fF)	30.75	13.75	7.08	14.96	6.56	4.16	20.84	7.61	5.65
K	0.750	0.684	0.590	0.684	0.590	0.684	0.842	0.711	0.618

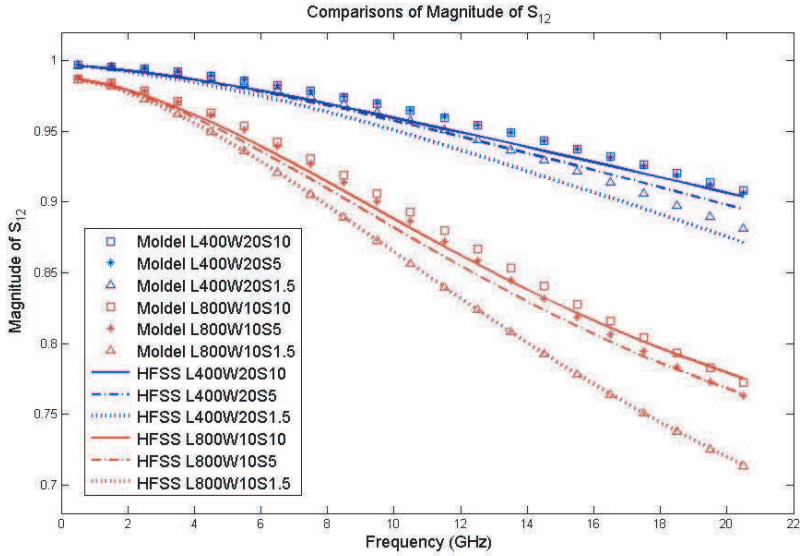


(a) Comparisons of the magnitudes of S_{11}

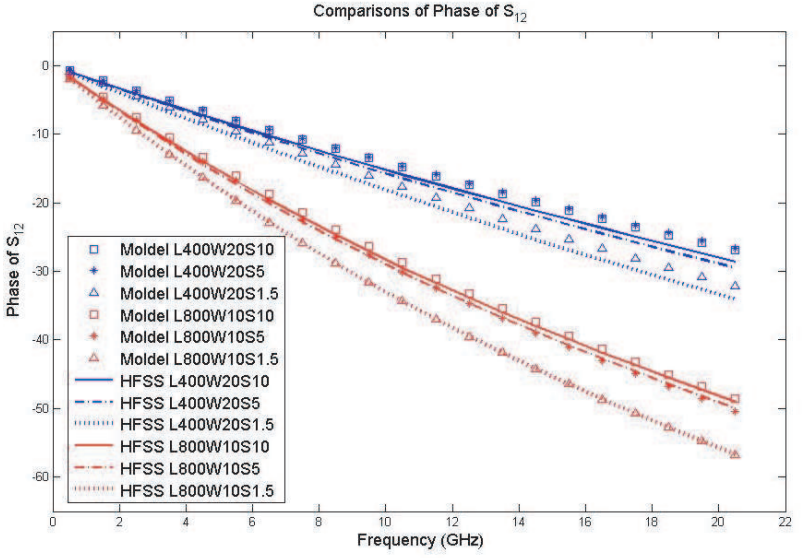


(b) Comparisons of the phases of S_{11}

Figure 5. Comparisons of S_{11}.

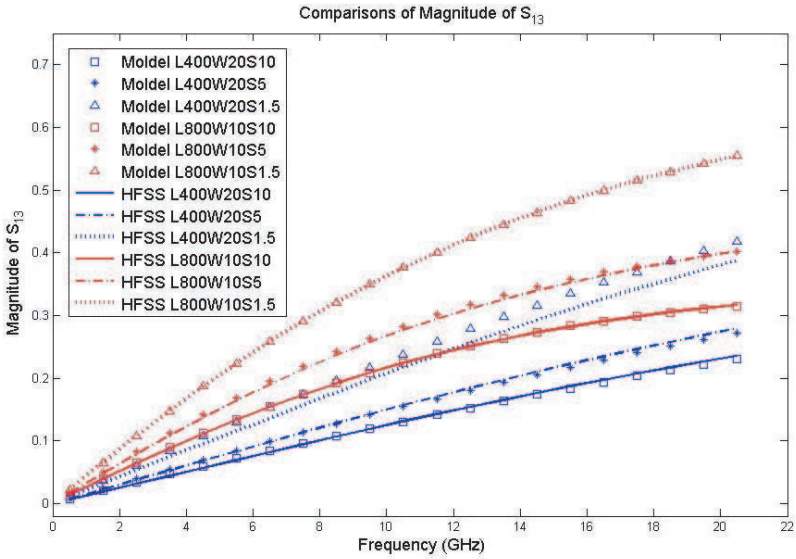


(a) Comparisons of the magnitudes of S_{12}

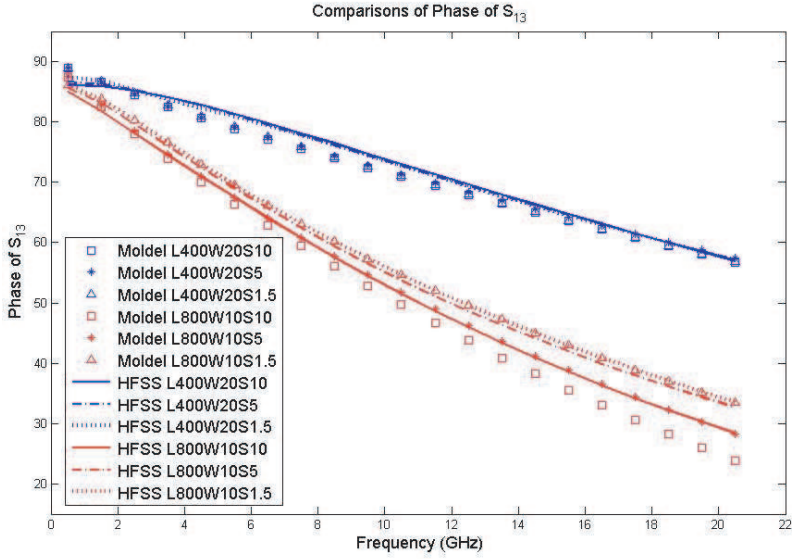


(b) Comparisons of the phases of S_{12}

Figure 6. Comparisons of S_{12}.

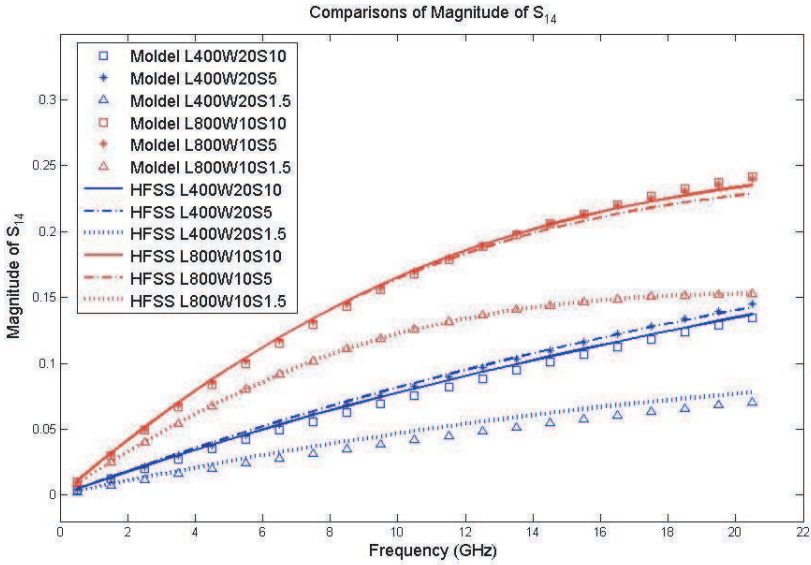


(a) Comparisons of the magnitudes of S_{13}

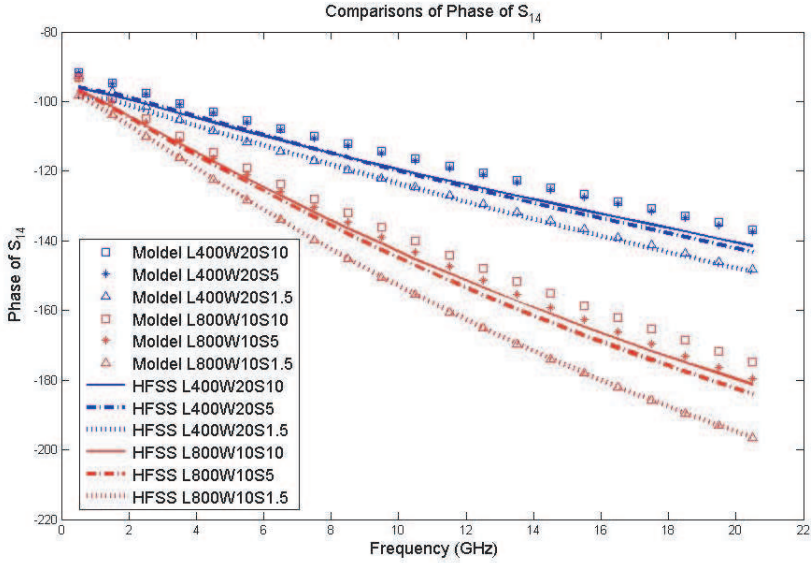


(b) Comparisons of the phases of S_{13}

Figure 7. Comparisons of S_{13}.



(a) Comparisons of the magnitudes of S_{14}



(b) Comparisons of the phases of S_{14}

Figure 8. Comparisons of S_{14}.

portion of the magnetic flux significantly.

$$K = \frac{M}{\sqrt{L_1 L_2}} \tag{6}$$

where L_1 and L_2 are the self inductances of the two interconnects. M is the mutual inductance between L_1 and L_2.

Simulations of the proposed coupled-line equivalent circuit model are performed by ADS. The simulated S-parameters are compared with the corresponding HFSS simulation results. Considering the symmetry of the test structures, it is known that $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$. Therefore, only S_{11}, S_{12}, S_{13} and S_{14} are compared here. The magnitudes and phases are plotted separately. From Figures 5 to 8, very good agreement can be observed over the entire frequency range from 500 MHz to 20 GHz. Thus, the proposed model and extracted model component values are validated. The average error is less than 10%.

5. CONCLUSION

In this work, an equivalent circuit model is proposed for on-wafer coupled interconnects for CMOS RFIC applications. The proposed SPICE compatible model is derived from a 2-Π single-line interconnect model by adding two coupling components. Due to the cost advantage, a calibrated EM simulator HFSS is used to obtain the four-port S-parameters of the coupled interconnects built in a 0.18 µm RF CMOS technology. EM simulations are performed for nine pairs of coupled interconnects with different combinations of lengths, widths and spaces. The results are used for model parameter extraction and model validation. The average error is less than 10% for the worst case.

REFERENCES

1. Avinash, S., B. N. Joshi, and A. M. Mahajan, "Analysis of capacitance across interconnects of low-K dielectric used in a deep sub-micron CMOS technology," *Progress In Electromagnetics Research Letters*, Vol. 1, 189–196, 2008.
2. Xia, L., R.-M. Xu, and B. Yan, "LTCC interconnect modeling by support vector regression," *Progress In Electromagnetics Research*, PIER 69, 67–75, 2007.
3. Xie, H., J. Wang, R. Fan, and Y. Liu, "Study of loss effect of transmission lines and validity of a spice model in electromagnetic

topology," *Progress In Electromagnetics Research*, PIER 90, 89–103, 2009.

4. Gazizov, T. R., "Far-end crosstalk reduction in double-layered dielectric interconnects," *IEEE Trans. Electromagn. Compat.*, Vol. 43, No. 4, 566–572, 2001.
5. Kumar, R., S. C. Rustagi, K. Kang, K. Mouthaan, and T. K. S. Wong, "Characterization and modeling of CMOS on-chip coupled interconnects," *37th European Solid State Device Research Conference*, 159–162, Sep. 2007.
6. Arz, U., D. F. Wiliams, D. K. Walker, and H. Grabinski, "Asymmetric coupled CMOS lines — An experimental study," *IEEE Trans. Microwave Theory Tech.*, Vol. 48, No. 12, 2409–2414, 2000.
7. Zheng, J., Y. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Microwave Theory Tech.*, Vol. 48, No. 9, 1443–1451, 2000.
8. Zheng, J., V. K. Tripathi, and A. Weisshaar, "Characterization and modeling of multiple coupled on-chip interconnects on silicon substrate," *IEEE Trans. Microwave Theory Tech.*, Vol. 49, No. 10, 1733–1739, 2001.
9. Agarwal, K., D. Sylvester, and D. Blaauw, "Modeling and analysis of crosstalk noise in coupled RLC interconnects," *IEEE Trans. Computer-aided Design*, Vol. 25, No. 5, 892–901, 2006.
10. Kumar, R., K. Kang, S. C. R. Rustagi, K. Mouthaan, and T. K. S. Wong, "SPICE compatible modelling of on-chip coupled interconnects," *Electron. Lett.*, Vol. 43, No. 9, 19–20, 2007.
11. Shi, X., J. Ma, K. S. Yeo, M. A. Do, and E. Li, "Equivalent circuit model of on-wafer CMOS interconnects for RFICs," *IEEE Trans. VLSI Syst.*, Vol. 13, No. 9, 1060–1071, 2005.
12. Shi, X., J. Ma, K. S. Yeo, M. A. Do, and E. Li, "Complex shaped on-wafer interconnects modeling for CMOS RFICs," *IEEE Trans. VLSI Syst.*, Vol. 16, No. 7, 922–926, 2008.
13. Shi, X., K. S. Yeo, J. Ma, M. A. Do, and E. Li, "Sensitivity analysis of coupled interconnects for RFIC applications," *IEEE Trans. Electromagn. Compat.*, Vol. 48, No. 4, 607–613, 2006.
14. Dreyfus, G., *Neural Networks: Methodology and Applications*, Springer, 2005.
15. http://www.home.agilent.com/agilent/product.jspx?nid=-34346.0.00&cc=US&lc=eng.