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FREQUENCY RESPONSE COMPARISON OF TWO COMMON ACTIVE INDUCTORS

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Abstract—The frequency responses of two widely used active inductor topologies are analyzed and compared using a generalized circuit model for the active devices in the circuits. A very wideband active inductor in CMOS was subsequently fabricated and tested and the inductor exhibits a measured self-resonant frequency of 9.7 GHz.

1. INTRODUCTION

The main attributes of active inductors include their small size, higher quality factors relative to passive inductors, and that they can be designed to be tunable. However, the traditionally large power dissipation, low self-resonant frequency and limited linearity performance of these circuits have restricted their applicability in radio-frequency integrated circuits (RFIC's). Implementing active inductors in a compound semiconductor (III-V) technology can certainly improve their frequency response but their power dissipation is rather high [1]. With the emergence of CMOS as a dominant technology in low to medium-power RFIC applications, there has been renewed interest in microwave active inductor design and some of the problems identified above are being successfully addressed.

In this paper, two widely used active inductor circuit topologies [2, 3] are analyzed using a generalized device circuit model for the transconductance elements. This approach allows us to remove transistor-specific variables such as gate-length and gate-width from the analysis and it enables us to draw a better comparison of the frequency performance of the two topologies. The analytic results show that one of the active inductor circuits has an inherently higher cutoff

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frequency than the other and based on that information we fabricated an active inductor that exhibits an exceptionally wide bandwidth of 9.7 GHz in a standard 0.18-μm CMOS process.

2. TWO ACTIVE INDUCTOR TOPOLOGIES

The majority of active inductor designs are based on the principle of using an impedance inverter connected to a capacitive load so that the impedance looking into the input of the inverter circuit becomes inductive. Here we will discuss two active inductor circuits that have come into widespread use. The circuits are shown in Figs. 1 and 2 and we will arbitrarily refer to them as Type 1 and Type 2 active inductors, respectively. Both of these circuits implement a single-ended inductor in which one terminal is grounded.

The Type 1 active inductor uses two operational transconductance amplifiers (OTA's) in a feedback configuration. OTA's are used here because they are more suitable for gigahertz-range applications [4] than operational amplifiers, for instance, which stems from the fact that OTA's are current-mode circuits. In contrast to the Type 1 active inductor, the Type 2 makes use of two feedback loops. Transistors M_1 and M_2 make up the first loop and transistors M_3 and M_4 make up the second loop. The two loops are joined at transistor M_2. Having two feedback loops results in more degrees of freedom when designing the inductance value and cutoff frequency of the Type 2 inductor.

The circuits in Figs. 1 and 2 have been individually studied and analyzed in previous works [2, 3, 5, 6], but a direct comparison between

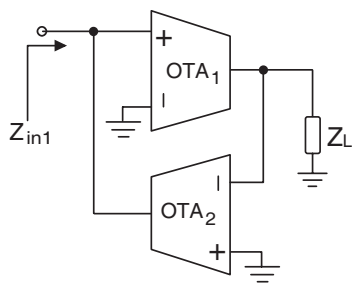

Figure 1. Type 1 active inductor.

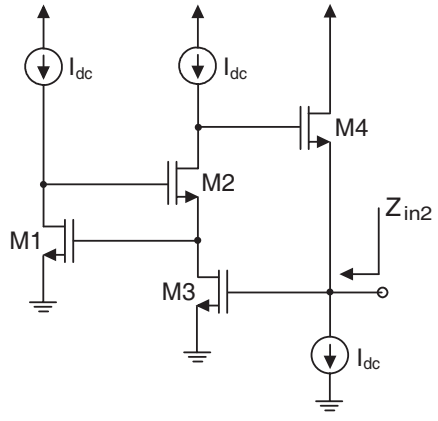

Figure 2. Type 2 active inductor.

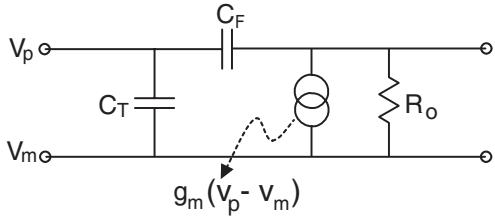

Figure 3. Device circuit model for both transistors and OTA's.

the two topologies with regards to their frequency response has not been carried out, to the best of our knowledge. To facilitate such a comparison, we will adopt the same device circuit model for the OTA's in Fig. 1 and the transistors in Fig. 2. The rationale for this approach stems from the observation that a single FET can be considered as a 'primitive' OTA and, to that end, the device circuit model depicted in Fig. 3 is suitable for our purposes. In the circuit model, C_T is the parasitic capacitance between the OTA input terminals, R_o is the current source output resistance, and C_F is the parasitic feedback capacitance, which is equivalent to C_{gd} in a FET.

3. FREQUENCY RESPONSE ANALYSIS

The self-resonant frequency of an inductor is defined as the frequency at which the inductor's reactance becomes negative, meaning it starts to behave like a capacitor. Therefore, the self-resonant frequency of an inductor establishes the absolute upper frequency limit on its useful operating frequency range. Both passive and active inductors exhibit self-resonance but the causes for this behavior are different for each inductor type. In passive spiral inductors, self-resonance occurs when the parasitic capacitive reactance between the coil windings overtakes the inductive reactance of the coil. In active inductors, self-resonance is primarily the result of the system's transfer function behavior but the roll-off in the gain of the active elements also plays a role. Next, we will examine the frequency response of the Type 1 and Type 2 active inductors.

3.1. Type 1 Active Inductor

Substituting the device circuit model of Fig. 3 for the OTA's in the Type 1 active inductor, the input impedance for that circuit is found

to be,

$$Z_{in1}(\omega) = \frac{R_{o2}||Z_{T1}}{g_{m1}g_{m2}(R_{o1}||Z_{T2}||Z_L)(R_{o2}||Z_{T1}) + 1} \tag{1}$$

where Z_{T1} and Z_{T2} are the impedances of capacitors C_{T1} and C_{T2}, respectively. If Z_L is a capacitive load of the type $1/j\omega C_L$, then Z_{in1} will be an inductive impedance. The self-resonant frequency of the inductor is found by determining the frequency at which the reactance of Z_{in1} changes from positive to negative and that frequency is,

$$\omega_{sr1} = \sqrt{\frac{g_{m1}g_{m2}}{C_{T1}(C_{T2} + C_L)}} \tag{2}$$

The device output resistances R_{o1} and R_{o2} limit the maximum inductance value, but they have only a minimal impact on the self-resonant frequency of the active inductor, which is why the ouptut resistances are absent from Eq. (2). Given that in most FET's and OTA's, $C_F \ll C_T$, the C_F capacitance was ignored in the derivation of Z_{in1} and therefore the value of ω_{sr1} (and ω_{sr2} in Section 3.2) should be interpreted as an absolute upper bound because the Miller effect, amongst other factors, will work to reduce the self-resonant frequency.

3.2. Type 2 Active Inductor

To analyze the response of the Type 2 inductor, each transistor in Fig. 2 is replaced by the device circuit model in Fig. 3. The input impedance of the resulting equivalent circuit is given by,

$$Z_{in2} = \frac{1}{Y_{T3} + (1 - \psi)Y_{T4} - g_{m4}\psi} \tag{3}$$

where

$$\psi = \frac{Y_{T4} - g_{m2}\beta}{\frac{1}{R_{o2}} + Y_{T4}}$$

and

$$\beta = \frac{g_{m3}(Y_{T2} - g_{m1})}{\left(Y_{T1} + g_{m2} - \frac{1}{R_{o3}}\right)(Y_{T2} - g_{m1}) - Y_{T2}\left(g_{m1} + \frac{1}{R_{o1}}\right)}.$$

The reactive part of Z_{in2} starts as a positive quantity (inductive) at 0 Hz and undergoes multiple sign changes at high frequencies. The frequency of the first sign change determines the self-resontant frequency of this active inductor, which occurs at

$$\omega_{sr2} = \sqrt{\frac{g_{m1}g_{m2}}{C_{T1}C_{T2}}}. \tag{4}$$

3.3. Comparisons

To enable us, again, to draw some general conclusions, we will assume that the Type 1 and Type 2 active inductor circuits are biased so that the transconductances g_{m1} and g_{m2} have same values in the two circuits. Thus, we observe that the Type 2 inductor has a higher self-resonant frequency than the Type 1 inductor because the Type 2 inductor does not make use of a load capacitor, C_L.

In some cases, chip designers using a Type 1 active inductor will employ the parasitic input capacitance of OTA_2 as the capacitive load, in which case $C_L = 0$, and this leads to the result that,

$$\omega_{sr1} = \omega_{sr2} = \sqrt{g_{m1}g_{m2}/(C_{T1}C_{T2})} \tag{5}$$

Therefore, the absolute bandwidth of a Type 1 inductor can, at most, be equal to the bandwidth of a Type 2 inductor but usually the Type 1 will have a lower bandwidth because often $C_L \neq 0$ and, furthermore, a practical OTA has a larger parasitic input capacitance than the single FET devices used for a Type 2 active inductor.

4. EXPERIMENTAL RESULTS AND DISCUSSION

In view of the higher frequency response of the Type 2 active inductor, we have designed and tested an IC with that active inductor topology using a standard 0.18-μm CMOS process. The measured and simulated results are plotted in Fig. 4 along with a microphotograph of the fabricated chip. The drop in inductance at the lower end of the frequency range is due to the use of a series DC bypass capacitor at

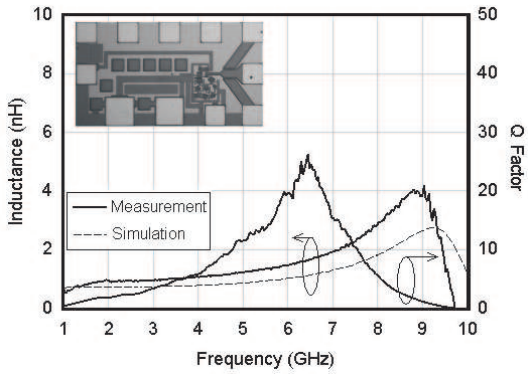

Figure 4. Measured and simulated frequency response for a fabricated Type 2 active inductor.

the input terminal of the chip. From 1 GHz to 5 GHz the inductance is around 1 nH and the frequency response is reasonably flat. The inductance starts to increase above 5 GHz until it reaches a maximum value of 4 nH at around 9 GHz, after which point the inductance quickly drops and becomes negative when the self-resonant frequency is reached, which occurs at 9.7 GHz. The chip consumes 13.5 mW of DC power and the core measures only 0.0064 mm^2.

In a CMOS implementation, the Type 1 active inductor should be able to surpass the Type 2 active inductor in linearity performance. This observation stems from the fact that the OTA's in Fig. 1 can be designed to have a much larger 1-dB compression point ($P_{1\,\mathrm{dB}}$) and third-order intercept point (TOI) than the individual NMOS devices in Fig. 2. The situation changes if Gallium Arsenide or Gallium Nitride transistors, for example, are used in the Type 2 inductor. These type of transistors can handle large amounts of RF power, but at the same time they also consume more dc power than silicon transistors, which must be taken into consideration in any RFIC application.

A comparison between the chip presented here and other CMOS-based active inductors is shown in Table 1. Only papers that report experimetnal results have been included in the table. Our active inductor has the highest self-resonant frequency of this set of works, but also the largest power consumption amongst those that reported this quantity. The somewhat high power consumption stems from the fact that we used a different dc bias current for transistor M_4 in Fig. 2 compared to the other transistors in the circuit in order to optimize the frequency response of the active inductor. The bias current of M_4 was 2.9 mA compared to an average of 0.8 mA for transistors M_1–M_3. To mitigate this issue, the transistors can be resized so that the overall power consumption is reduced but the circuit speed remains about the same.

Table 1. CMOS-based active inductor comparison table.

Ref.	**Self-Resonant Frequency**	**Maximum Inductance**	**DC Power (mW)**	**Die Area (mm^2)**
[7]	3.6 GHz	70 nH	–	–
[5]	6.25 GHz	2 nH	5.58	–
[8]	7.25 GHz	18 nH	12	–
This Work	9.7 GHz	4 nH	13.5	0.0064

5. CONCLUSION

Two predominant active inductor topologies were analyzed in this paper and expressions were derived for their inductance and self-resonant frequencies. Theoretically, with all things being equal, a Type 1 and a Type 2 active inductor can have the same self-resonant frequency but, in practice, the Type 2 will usually outperform the Type 1 in terms of frequency response due to its lower input parasitic capacitances. The Type 1 active inductor does have a potential advantage over the Type 1 in terms of linearity performance because specialized linearization techniques can be adopted in the design of the constituent OTA's.

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