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HIGHLY INTEGRATED MINIATURE-SIZED SINGLE SIDEBAND SUBHARMONIC KA-BAND UP-CONVERTER

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Abstract—A highly integrated up-converter MMIC is presented for low cost and high performance Ka-band transmitter module application. The multiple functions of the up-converter, such as local oscillator (LO) amplifier, single sideband subharmonic mixer, LO bandstop filter, and three-stage RF amplifier, are integrated into a single chip. A proper circuit topology for the complete integrated circuit is selected to achieve the miniature chip size. The combination of lumped and microstrip lines are used to realize the compact sub-circuits. The layout of the circuit is optimized using electromagnetic (EM) simulations. The chip is fabricated in WIN 0.15 μm PHEMT technology on 4-mil GaAs substrate with a layout area of only 2.8 mm × 0.8 mm (2.24 mm^2). Measured conversion gain is 12 ± 1 dB over 28–37 GHz for the LO pumping power of 0 dBm. The sideband and 2 × LO suppressions are above 20 dBc. The 1 dB gain compression output power (P-1 dB) is 12 dBm and LO to RF isolation is above 35 dB.

1. INTRODUCTION

Ka-band wireless systems have various applications in point-to-point, point-to-multipoint, very small aperture terminal (VSAT), and RADAR systems [1–13]. At such high frequency bands, the transmitter system has been known as the most expensive part because of the incorporation of a number of MMIC chips, such as LO amplifier, LO frequency doubler, mixers, RF amplifier, and power amplifiers. Designing a transmitter module therefore becomes complex in the

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fabrication and processing of numerous chips, their assembly, and resultant interconnecting mismatches and losses. This increases system cost and degrades overall performance. MMIC chips are also expensive due to their large area and expensive GaAs-based technology materials. To reduce design complexity and cost, an integrated chip is the solution which includes number of circuits into a single chip to reduce chip numbers in transmitter module. However, for the integrated solution, the chip size should be compact to reduce the cost of the system and with the high performance. Due to number of advantages, the integrated chips become ultimate solution for the low cost and high performance transmitter systems at high frequency band. Hence, there is always great interest in reducing the size of MMIC chips [7–10]. Consequently, 3D MMIC technology was developed for the realization of highly integrated and miniaturized chips [4]. The integrated up- and down-converter MMICs for the customer premise equipment application at 28 GHz have been presented [11]. The design was focused for the compact chip size to provide low cost solution. Mahon et al. have also reported low band and high band up- and down-converters [12]. However, further investigation in more compact integrated Ka-band up- and down-converter MMICs is still needed.

In this paper, a highly integrated miniature-sized Ka-band up-converter is presented to replace a number of MMICs in the transmitter module. This will reduce transmitter design complexity and cost, as well as provide high performance to the system. Subharmonic mixing in chip can reduce local oscillator frequency by half, as it is easier to obtain high performance oscillator at lower frequency. Similarly, a single sideband design can suppress unwanted sideband frequency. In addition, an anti-parallel diode mixing can suppress the undesired second harmonic of the local oscillator ($2 \times$ LO). The suppression of sideband and $2 \times$ LO frequency is indispensable as these undesired signals are very close to the desired one. The topology of the circuit is then aimed to meet the compact layout size, which then can advance circuit performance.

2. DESIGN AND PERFORMANCE OF THE INTEGRATED CHIP

The schematic of the integrated up-converter chip is shown in Fig. 1(a). It consists of an LO amplifier, subharmonic single sideband (SSB) mixer, LO bandstop filter, and a three-stage RF amplifier. The integration of the LO amplifier has reduced LO power requirement to less than 0 dBm. The SSB mixer is designed using two subharmonic mixers, an LO inphase power divider, and an RF 90° phase power

combiner. To achieve the sideband suppression, the LO signal is divided into two ways with in-phase divider to pump two subharmonically pumped (SHP) mixers. The RF output of the two SHP mixers is combined by quadrature phase combiner. The subharmonic mixer, as shown in Fig. 1(c), is designed using an anti-parallel diode pair. At the LO port of the SHP mixer, a circuit to shorten IF (intermediate frequency) and RF signals is used. Similarly, the LO short circuit is used at the RF port to shorten LO signal. The IF is fed through the lowpass filter at the RF port-end of the diode. The lumped and microstrip circuit elements are used to achieve the compact size of the mixer. The LO in-phase divider is realized using the lumped element Wilkinson divider. The lumped element approach is used to realize the compact layout size as well as wide bandwidth. The RF 90° phase power combiner is realized using Lange coupler. It is also compact in size and provides wide bandwidth.

The LO amplifier, as shown in Fig. 1(b), is a single stage power amplifier utilizing 0.40 mm pHEMT transistor which is capable of providing P-1 dB output power greater than 20 dBm. The gain of the LO amplifier is greater than 12 dB for the frequency of 13–19 GHz. The RF amplifier is used to amplify the output RF signal of the SSB mixer. The 3-stage RF amplifier is designed to get gain above 24 dB over the bandwidth of 25–36 GHz, as well as P-1 dB output power greater than 20 dBm, is shown in Fig. 1(d). For the design of the amplifier, the gain, linearity, and compact layout size are the major considerations. To suppress LO signals coming from the mixer, the LO stopband filter is integrated at the input of the RF amplifier. This prevents LO signals from entering into RF amplifier and generating harmonics.

The integration of LO bandstop filter at the input of the RF amplifier additionally attenuates LO frequencies to about 20 dB. Third-order intermodulation distortion for the two-tone test of the RF amplifier is 68 dBc at output power level of 10 dBm. The layout of the multiple circuits is miniaturized by folding the microstrip lines and tested by EM (electromagnetic) simulations. The simulations of the circuits were performed using AWR's Microwave Office software. The EM simulations of the layouts were done with Zeland's IE3D simulator.

The microphotograph of the fabricated MMIC and the corresponding schematics of the miniature upconverter chip are shown in Fig. 2. The circuits were fabricated by using WIN Semiconductor's standard 0.15 μm GaAs MMIC technology on a 100-μm thick substrate. The chip dimension is 2.8 mm × 0.8 mm. Measurement results are compared with simulation results at a drain bias voltage of 3 V and gate bias in class A condition. The maximum conversion gain of 12.5 dB occurs at the LO power of −2 dBm. The required LO power for the

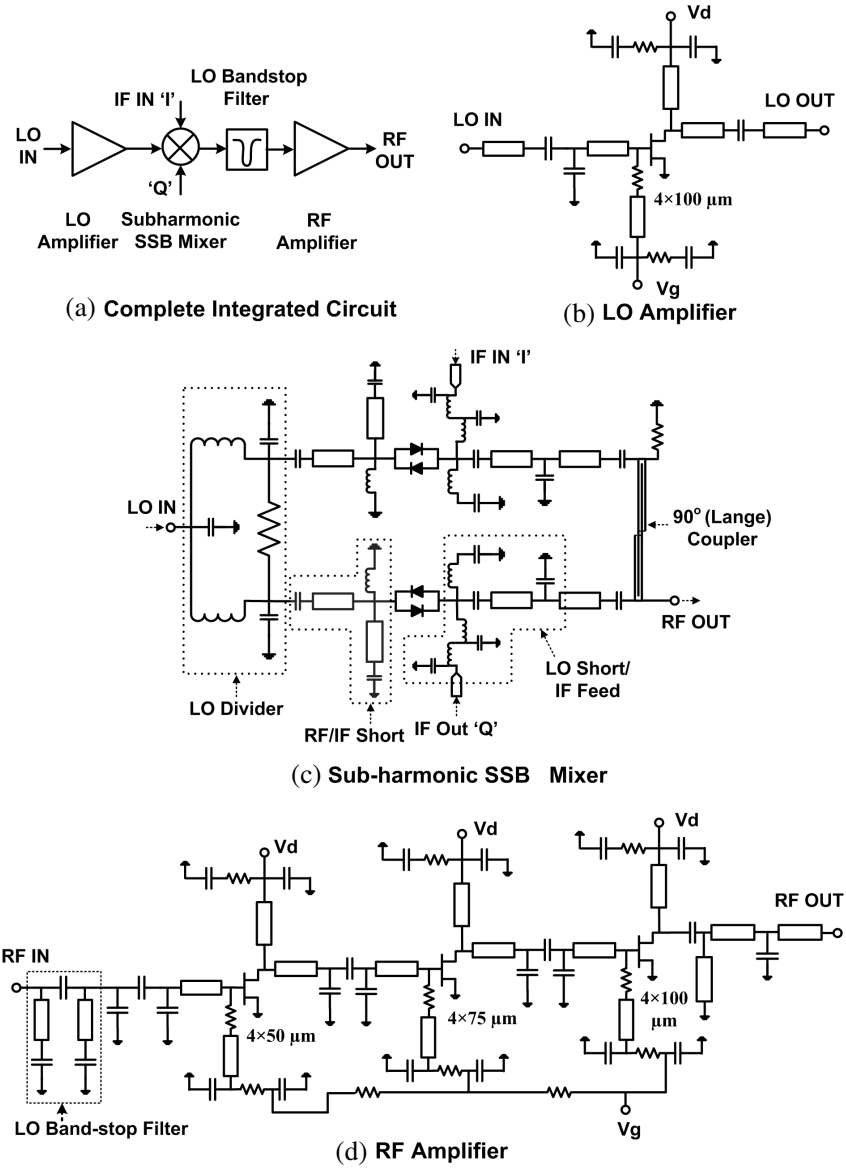

Figure 1. Schematics of the circuit, (a) complete integrated up-converter, (b) LO amplifier, (c) SSB subharmonic mixer, and (d) RF amplifier with integrated LO band-stop filter.

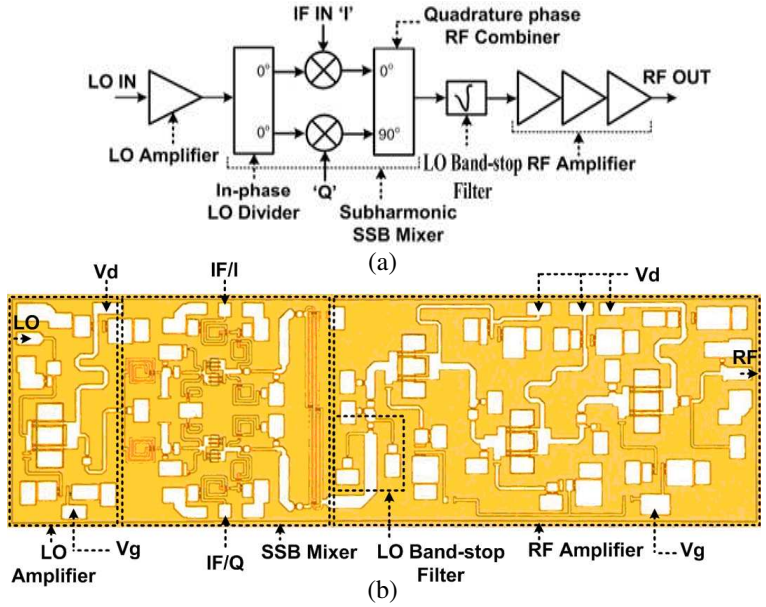

Figure 2. (a) Schematics of the miniature upconverter chip and (b) microphotograph of the integrated up-converter MMIC. Layout area is 2.24 mm^2.

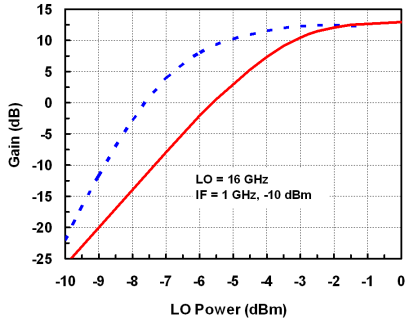

Figure 3. Measured (continuous lines) and simulated (dotted lines) conversion gain versus LO power.

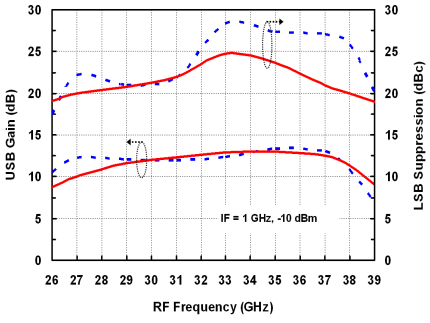

Figure 4. Measured (continuous lines) and simulated (dotted lines) upper sideband (USB) conversion gain and lower sideband (LSB) suppression.

maximum conversion gain is below 0 dBm, as shown in Fig. 3. The difference between measurement and simulation results is due to the inaccuracies in the non-linear model of the devices. The maximum

conversion gain for the RF frequency of 28–37 GHz is 12 ± 1 dB, as presented in Fig. 4. The LSB suppression is 20 dBc or better for the frequency of 27–38 GHz. The different sideband suppression is due to the phase and amplitude imbalance between two RF signals of the two mixers combined at 90°RF combiner. Overall, the 20 dBc suppression of LSB shows a good performance of the up-converter.

The measured P-1 dB RF power of 12 dBm was obtained, as shown in Fig. 5. Third-order intermodulation distortion product (IM3) for the two-tone test of the integrated up-converter with an IF frequency of

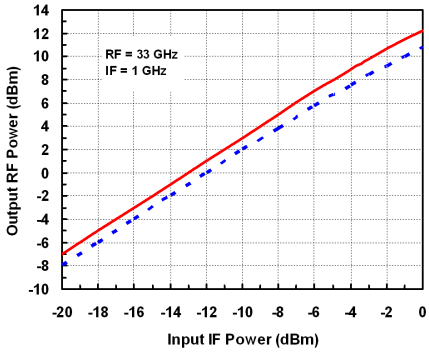

Figure 5. Measured (continuous lines) and simulated (dotted lines) RF output power versus IF input power.

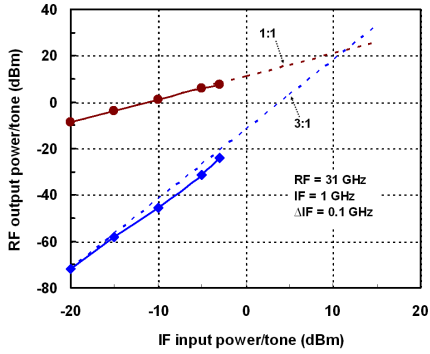

Figure 6. Third-order intermodulation distortion for the two-tone test.

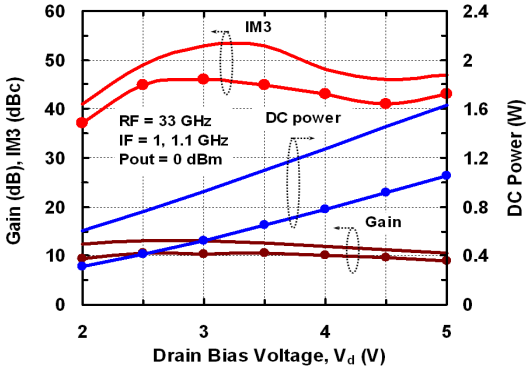

Figure 7. The third order intermodulation distortion and conversion gain variation with drain bias voltage (i.e., DC power) at class A (continuous lines) and class AB (circle line) gate bias conditions of the amplifiers.

1 GHz and RF frequency of 31 GHz is shown in Fig. 6. The OIP3 and IIP3 are above 20 dBm and 10 dBm, respectively. The 50-dBc suppression of the intermodulation distortion (at output power of 0 dBm) is found suitable for the complex modulation level up to 64 QAM.

The effect of DC power consumption on gain and nonlinearity of the up-converter is shown in Fig. 7. The circuit can operate at a drain bias voltage as low as 2.5 V without degrading performance.

The suppression of $2 \times$ LO signal is above 20 dBc, as shown in Fig. 8. A high LO to RF isolation, which is better than 35 dB, was also achieved due to addition of the LO bandstop filter. Measured

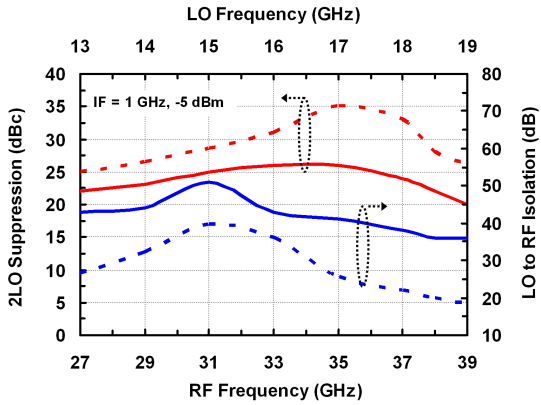

Figure 8. Measured (continuous lines) and simulated (dotted lines) $2 \times$ LO suppression and LO to RF isolation.

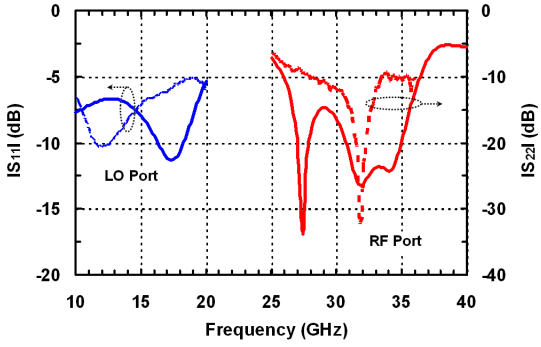

Figure 9. Measured (dotted lines) and simulated (continuous lines) return loss.

Table 1. Comparison of the measured performance of the presented chip with other reported chips.

Parameters	[7]	[11]	[12]	[12]	[13]	**This Work**
RF frequency band (GHz)	22–38	24–29	17–36	32–45	38	**28–37**
Conversion gain (dB)	9–15	0–5	10–13	3	−12	12 ± 1
P-1 dB output power (dBm)	7–12	1	-	-	-	**12**
IIP3 (dBm)	16	-	12	15	14	**15**
Side-band supp (dBc)	17–27	16	0	15	15	**20–27**
2 LO suppression (dBc)	15–35	-	5–15	> 0	-	**22–25**
LO to RF isolation (dB)	20–35	15	15–40	-	-	**35**
LO power (dBm)	9–16	0	0	2	0	**0**
Layout area (mm^2)	4.2	4.2	6.8	5.9	6.89	**2.24**
D. C. power (W)	0.9	0.8	2	0.8	0.9	**1.0**

and simulated S-parameters for the mismatch at the LO and RF ports are shown in Fig. 9. The magnitude of S_{22} at the RF port is about -10 dB. Similarly, the measured magnitude of S_{11} at the LO port is about -5 dB or better at 10–20 GHz frequency. The comparison of the chip performance with other published results is shown in Table 1. The size of the chip is miniaturized by using some lumped design techniques with promising performance.

3. CONCLUSION

The design and implementation of the highly integrated miniature-sized Ka-band subharmonic single sideband up-converter MMIC is presented. Measured conversion gain is 12 ± 1 dB for the RF frequency at 28–37 GHz. The P-1 dB RF output power level of 12 dBm is achieved

with an IIP3 of 12 dBm. The amount of the sideband and $2 \times$ LO suppression is above 20 dB. The chip is most compact at a layout area of as small as 2.24 mm^2. This integrated chip is very suitable for the proposed low cost and high performance Ka-band transmitter module application.

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