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A TUNABLE BANDPASS FILTER USING Q-ENHANCED AND SEMI-PASSIVE INDUCTORS AT S-BAND IN 0.18-μM CMOS

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Abstract—A fully-integrated bandpass filter using Q-enhanced and semi-passive inductors is design, implemented and verified experimentally in a standard 0.18-μm CMOS process. The inductors achieve high-Q factors by using a tapped-inductor feedback technique to produce negative resistances. Compared with conventional transformer feedback, the proposed technique not only compensates resistive losses with low-power consumption but also provides a high-inductance inductor which is suitable for low-frequency applications. The 2-pole Chebyshev series-C coupled bandpass filter provides a frequency tuning range of 300 MHz around 2.65 GHz. Measurements shown that it consumes 2.4 mW to achieve 1.0-dB insertion loss, 12-dB return loss, 6.3-dB noise figure, and −2.5-dBm input $P_{1\text{dB}}$ with a 950-MHz bandwidth at 2.8 GHz. And it consumes 5.6 mW to achieve 1.5-dB insertion loss, 10-dB return loss, 7.9-dB noise figure, and −4-dBm input $P_{1\text{dB}}$ with a 700-MHz bandwidth at 2.5 GHz. The overall chip size of the filter is 0.7 mm × 0.9 mm including all testing pads.

1. INTRODUCTION

Rapid advances in CMOS technology make wireless communication systems on a single chip (SOC) come true [1, 2]. The silicon-based integrated circuits (ICs) feature low cost manufacturing and high volume integrating capabilities. However, poor-Q factors of CMOS inductors which are suffered from the low-resistivity substrate limit their system applications and integrations at radio frequencies (RF).

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The inherent losses of the passive components lead to bandpass filters having relatively high insertion losses, limited dynamic range and low out-of-band attenuation rates. Therefore, many giga-hertz receivers still require bulky and expensive off-chip bandpass filters to attenuate large out-of-band interferences and to pass in-band signals with minimal losses. Once on-chip high-Q inductors are realized, LC-based filters can be obtained. And the integrated filters would enable a greater variety of transceiver architectures to be achieved in a monolithic form.

Typically, on-chip inductors use symmetric and wide-metal layout, differential drive, thick metal layers, and ground shielding techniques for high-Q factors [3–8]. Other Q-enhanced techniques such as silicon-on-insulator (SOI) or micro-electro-mechanical systems (MEMS) minimizing resistive losses in the silicon substrate require special and additional photolithography [9, 10]. The inductors discussed above are all purely passive components since these inductors merely consist of metal lines without any active devices. Therefore, a purely passive inductor usually consumes large chip area. Recently, many active inductors take advantage of CMOS transistors to realize superior-Q factors [11–14]. The main attributes of the active inductors include their smaller chip size and higher Q factors compared with passive inductors, and can be a tunable design. However, these purely transistor-based techniques consume high-power consumption. In addition to purely passive and active inductors, many semi-passive inductors consisting of MOS transistors and passive inductors or transformers are presented [15–18]. These inductors utilize complementary cross-coupled pairs or transformer feedback architectures to compensate the resistive losses These so-called semi-passive inductors are integrated into bandpass filters which are one of the most critical barriers for the realization of RF SOC. Though semi-passive inductors achieve high Q factors with moderate power consumption, they still consume large chip area. The equivalent inductance of a transformer-feedback inductor is merely contributed by the inductance of the primary inductor and the mutual inductance between the primary and secondary inductors. Moreover, the secondary inductor doesn't contribute equivalent inductance as well as equivalent negative resistance directly.

In this paper, a tapped-inductor feedback technique is proposed for high-Q inductors The Q-enhanced technique demonstrates that the secondary inductor will contribute inductance and negative resistance directly of the equivalent inductor, and achieve a high-Q and low-power inductor design. The semi-passive inductors are suitable for low-frequency applications, and then are incorporated into a 2-pole

Chebyshev series-C coupled bandpass filter at S-band. To the best of authors' knowledge, this design is the first tunable bandpass filter using tapped-inductor feedback technique in a standard 0.18-μm CMOS process with low-power consumption. The design will be detailed in the following sections. In Section 2, we review the semi-passive inductors using transformer feedback, and describe the circuit design of the proposed semi-passive inductor using tapped-inductor feedback. In Section 3, the design and implementation of the series-C coupled bandpass filter are presented. The experimental results and discussions of the filter are also reported in Section 4. Finally, Section 5 concludes this work.

2. DESIGN OF A SEMI-PASSIVE INDUCTOR

This section is divided into four parts to investigate the properties of the semi-passive inductor. Section 2.1 reviews the semi-passive inductor using transformer feedback. Sections 2.2 and 2.3 introduces the circuit design, and validates the concept of the proposed inductor, respectively. Finally, Section 2.4 describes the noise analysis of the proposed inductor.

2.1. Transformer Feedback

Figure 1(a) illustrates the schematic of a Q-enhanced semi-passive inductor using transformer feedback which was presented in [16]. The mutual inductance M caused by the magnetic coupling of L_1 and L_2 forming a negative resistance which compensates the resistive losses of L_1. Therefore, a high Q-factor inductor with an inductance of L_1 is obtained by the transformer feedback technique. Since the transformer is placed at the drain and gate terminals of the MOS transistor, the implementation of the architecture requires RF chokes for DC biasing. Therefore, this kind of semi-passive inductors is hard to be a compact design with the area-consuming RF chokes and the transformer. The revised schematic of the semi-passive inductor presented in [17] is shown in Fig. 1(b). L_1 and L_2 of the transformer are grounded in one end, and L_2 is connected to the source of the NMOS transistor in the other end. The negative resistance can be obtained when the phase difference between i_1 and i_2 is 90° or 270° [16]. Unlike Fig. 1(a), this architecture requires no additional RF chokes, and its equivalent circuit represents a grounded inductor.

Based on Fig. 1(b) and the small-signal analysis, the current i_1 and i_2 can be expressed as

$$i_1 \cong j\omega C \cdot V_{gs} \tag{1}$$

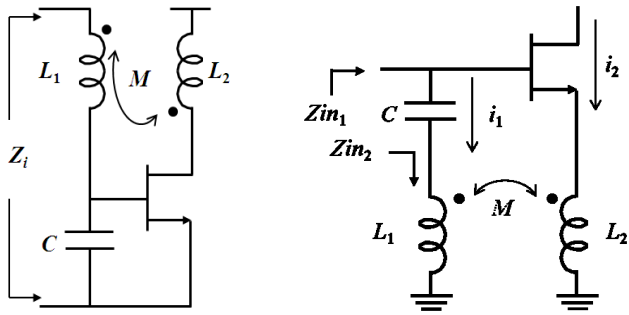

Figure 1. (a) Schematic of a semi-passive inductor reported in [16]. (b) Schematic of a semi-passive inductor reported in [17].

and

$$i_2 = g_m V_{gs}, \tag{2}$$

respectively. The approximation in (1) results from the unequal inductance of coupled inductor L_1 and L_2 By neglecting the effect of the input impedance of the transistor, therefore, the input impedance Z_{in1} can be obtained as shown in (3). The V_{gs}, g_m, and R_1 are gate-to-source voltage, transconductance of the transistor, and resistance of L_1, respectively. The resistive losses of L_1, or R_1 is mainly compensated by the negative resistance formed by mutual inductance M of the transformer, transconductance g_m of the transistor, and the capacitor C. Moreover, Z_{in1} is capacitive at low frequencies, as shown in (3). Therefore, an infinite-Q inductor of Z_{in1} must satisfy (4) and (5).

$$Z_{in1} = \frac{1}{j\omega C} + j\omega L_1 + R_1 + j\omega M\left(\frac{i_2}{i_1}\right) = \left(R_1 - \frac{Mg_m}{C}\right) + j\left(\omega L_1 - \frac{1}{\omega C}\right) \tag{3}$$

$$\omega > \frac{1}{\sqrt{L_1 C}} \tag{4}$$

$$R_1 = \frac{Mg_m}{C} \tag{5}$$

For a fixed M and C in (3), a high negative resistance requires a high g_m, or power consumption to compensate the resistive losses R_1. Moreover, L_1 should be as high as possible to be an inductive component at low frequencies. The alternative input impedance (Z_{in2}) is expressed in (6), which is inductive from DC to its self-resonant frequency.

$$Z_{in2} = \left(R_1 - \frac{Mg_m}{C}\right) + j\omega L_1 \tag{6}$$

2.2. Tapped-inductor Feedback

As discussed above, the transformer feedback doesn't make use of the inductance of L_2, and the equivalent input impedance is capacitive around low frequencies. Fig. 2(a) illustrates schematic of the semi-passive inductor using two independent inductors feedback. The input impedance (Z_{in3}) can be expressed as (7). Compared to the transformer feedback mentioned above, the imaginary part consists of L_2, which increases the equivalent inductance of the inductor. However, the real part consists of resistive losses of L_1 and L_2, which requires more power consumption to compensate the overall resistive losses.

$$\begin{aligned} Z_{in3} &= j\omega L_1 + R_1 + \left(\frac{i_2 + i_1}{i_1}\right)(j\omega L_2 + R_2) \\ &= \left(R_1 + R_2 - \frac{L_2 g_m}{C}\right) + j\omega\left(L_1 + L_2 + \frac{g_m R_2}{\omega C}\right) \end{aligned} \tag{7}$$

The proposed semi-passive inductor using tapped-inductor feedback is shown in Fig. 2(b). V_G and V_D with bypass capacitors are the bias for the gate and drain terminals of M_1, respectively. R is a high-resistive resistor providing RF signal blocking, and eliminating the need for an RF choke. The tapped-inductor is tapped to the source of M_1 and to L_2 resulting in a current flow $i_1 + i_2$ into L_2. The current flow and the mutual inductance will increase the equivalent inductance of the circuit drastically. The input impedance Z_{in} of the proposed

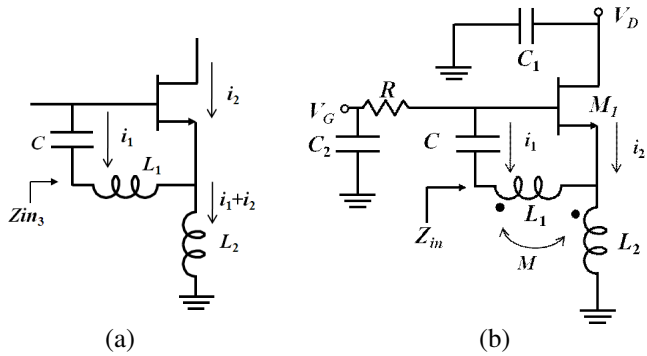

Figure 2. Schematic of semi-passive inductors using (a) two independent inductors or (b) a tapped-inductor feedback technique.

inductor can be expressed as

$$Z_{in}=j\omega L_1+R_1+j\omega M\left(\frac{i_2+i_1}{i_1}\right)+\left(\frac{i_2+i_1}{i_1}\right)\left[j\omega L_2+R_2+j\omega M\left(\frac{i_1}{i_2+i_1}\right)\right]$$
$$=\left(R_1+R_2-\frac{Mg_m}{C}-\frac{L_2g_m}{C}\right)+j\omega\left(L_1+L_2+2M+\frac{g_mR_2}{\omega C}\right) \quad (8)$$

The real part of Z_{in} consists of resistive losses of L_1 and L_2, and negative resistance related to M, L_2, g_m and C_3. Conceptually, the overall resistive losses of Z_{in} can be compensated by the proper mutual inductance of M and inductance of L_2. Typically, L_2 is larger than M with limited coupling coefficient. Therefore, the negative resistance term generated by L_2 is larger than the term generated by M with the same g_m and C_3. For example, assume $R_1 = R_2 = R_r$, $L_1 = L_2 = L$, coupling coefficient $k = 0.5$, and $C = C_r$ in Fig. 1(b) and Fig. 2(b), and the corresponding g_m compensating the resistive losses can be calculated from (3) and (8). The obtained g_m in Fig. 1(b) and Fig. 2(b) is $2(R_rC_r/L)$ and $4(R_rC_r/L)/3$, respectively. Therefore, the proposed architecture is believed that the desired negative resistance can be achieved easily with low-power consumption. The input impedance Z_{in} is inductive from DC to high frequencies as shown in (8) since the effects of high impedance of the RC_3 series network and the input impedance of the transistor at the gate terminal can be neglected. Moreover, the imaginary part of Z_{in} not only consists of L_1 but also L_2 and two times M. Unlike conventional transformer-feedback architecture mentioned above, the proposed tapped-inductor feedback architecture demonstrates an inductance-enhanced characteristic which is suitable for low-frequency applications.

Figure 3 shows the equivalent circuit model of a center-tapped spiral inductor in a CMOS process. Compared with a model of a standard inductor, the model in Fig. 3(a) consists a mutual inductance M contributed by the physical layout of a center-tapped inductor. Therefore, the center-tapped spiral inductor can be regarded as an equivalent transformer circuit model with the common node, or the tapped node. For most applications, the center tap of the inductor usually connects with ground or V_{DD}. Thus, the polarity of the equivalent transformer formed by L_1 and L_2 is shown in Fig. 3(a). In this paper, the center tap of the inductor of the proposed architecture is not AC grounded. As result of it, a simplified model and relative polarity of the transformer can be obtained as shown in Fig. 3(b). P_1, P_2, and P_3 in Fig. 3(b) are connected to the corresponding node Z_{in}, source terminal of M_1 and ground in Fig. 2(b), respectively. From (8) and Fig. 3(b), the self-resonant frequency (f_{res}) of the proposed

semi-passive inductor can be approximated as

$$f_{res} = \frac{1}{2\pi\sqrt{\left(L_1 + L_2 + 2M + \dfrac{g_m R_2}{\omega C}\right) \cdot C_t}} \tag{9}$$

where C_t is the total capacitance including metal coupling capacitance, oxide capacitance between the inductor and substrate, and other paracitic capacitance. Fig. 4(a) and Fig. 4(b) show a physical layout of 3-turn center-tapped and non-center-tapped spiral inductors,

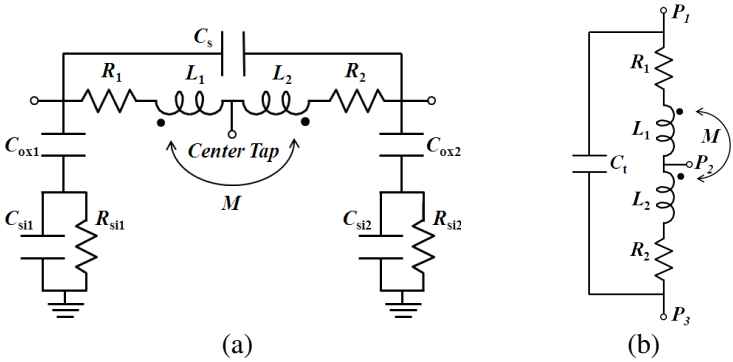

Figure 3. (a) Equivalent model of a center-tapped spiral inductor on silicon. (b) Simplified model of a tapped spiral inductor when P_2 is not AC grounded.

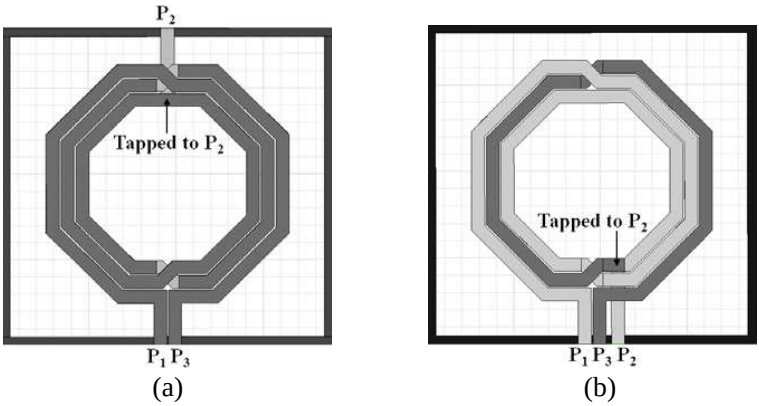

Figure 4. (a) Physical layout of a center-tapped spiral inductor. (b) Physical layout of a non-center-tapped spiral inductor.

respectively. The P_2 is tapped via an underneath metal line as shown in Fig. 4. The width, spacing, and inner radius of the layout in both Fig. 4(a) and Fig. 4(b) are 15 μm, 2 μm, and 90 μm, respectively. The tapped inductors in Fig. 4 can be also regarded as a kind of interleaved transformers with a common node, and the model in Fig. 3(b) is applicable to the different layouts both.

2.3. Validation of the Proposed Semi-passive Inductor

Typically, foundry provides the model of center-tapped spiral inductors. As result of it, it is easy to make a quick assessment and validation of the proposed semi-passive inductor by using the physical layout in Fig. 4(a). The Q factor of an inductor can be defined by the ratio of stored energy to the dissipated energy. Therefore, the quality factor can be shown that

$$Q = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \tag{10}$$

where Z_{11} is the input impedance seen at one port of the inductor while the other is grounded. Extraction of the inductance and resistance from Z_{11} enables the evaluation of Q factor. Moreover, assuming R, C, V_D, and aspect ratio of M_1 in Fig. 2(b) are 10 KΩ, 2 pF, 0.8 V, and (32 μm/0.18 μm), respectively. The resistance extraction and Q evaluation of the proposed semi-passive inductor without practical layout effects are shown in Figs. 5(a) and 5(b), respectively. Increasing V_G bias reduces the equivalent resistance as shown in Fig. 5(a). Moreover, with V_G of 0.564 V, the equivalent resistance approaches zero while maintaining the overall stability of the circuit. As shown in Fig. 5(b), with different V_G of 0 V, 0.544 V, 0.56 V, and 0.564 V, the peak Q factor are 7.3, 20.1, 52.3, and 124, respectively. Moreover, the V_G of 0.564 V draw a current flow of 0.36 mA, demonstrating a low-power design. The extracted resistance and Q factor are all positive from DC to self-resonant frequency, which represents the semi-passive inductor is inductive within this frequency range. Thus the simulated results in Figs. 5(a) and 5(b) validate the circuit concept and analysis of the proposed semi-passive inductor. Since the voltage-tuning mechanism doesn't affect the inductance and parasitic capacitance of the semi-passive inductor, the self-resonant frequency is independent of V_G. The self-resonant frequency of the inductor is around 6.1 GHz.

The use of the tapped-inductor feedback could result in potential instability depending on the g_m or power consumption. Fig. 6 shows the S_{11} of the proposed inductor under different bias conditions. An ideal inductor with in infinite-Q factor locates on the upper-half plane of the unit circle in the Smith Chart. The Q factor with V_G of 0 V is

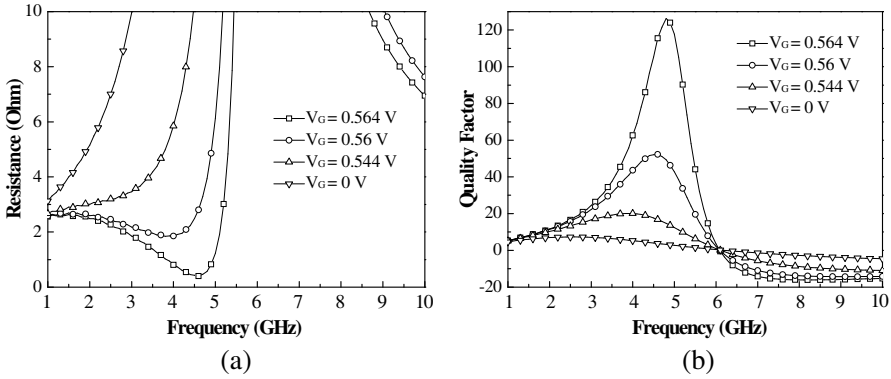

Figure 5. (a) Simulated resistance and (b) Q factor of the proposed inductor under different bias conditions.

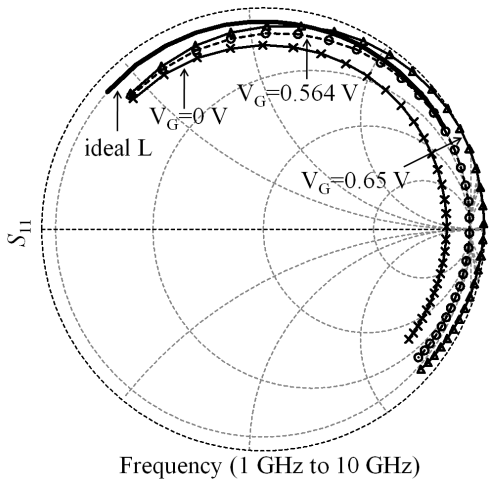

Figure 6. Simulated S_{11} of the proposed inductor under different bias conditions.

low, and the circuit is stable. Moreover, the Q factor with V_G of 0.564 V is high, and the circuit is operated close and within the unit circle of the Smith Chart to maintain its stability as shown in Fig. 6. Once V_G of 0.65 V is applied, the more power consumption makes the magnitude of S_{11} will exceed 1, which results in circuit stability problem. In order to make sure the circuit is stable, it must ensure that the magnitude of the S_{11} less than 1 for all frequencies. To maintain the stability of the circuit, the g_m must comply with the following equation which can

be derived from (8).

$$g_m \leq \frac{C(R_1 + R_2)}{M + L_2} \tag{11}$$

2.4. Noise Analysis of the Proposed Semi-passive Inductor

The detailed noise analysis Q-enhanced and parallel resonant LC tanks has been presented in [19]. The thermal drain noise current of transistors can be expressed as the following equation [20].

$$\frac{\overline{i_d}}{\sqrt{\Delta f}} = \sqrt{4kT\gamma g_m} \tag{12}$$

where g_m is the transconductance of transistors in saturation, and the coefficient γ is derived to be equal to 2/3 for long-channel transistors and may need to be replaced by a larger value for submicron transistors. With reference to the circuit shown in Fig. 2(b) and Equation (8), the three main noise sources are the thermal noise ($\overline{v_{1n}^2}$) of R_1, the thermal noise ($\overline{v_{2n}^2}$) of R_2, and the thermal drain current noises ($\overline{i_{d1}^2}$) of M_1. The RF signal block/bias resistor, R, although typically large ($\sim 10\,\mathrm{k}\Omega$), does not contribute significantly to the overall noise of the circuit Assuming Z_{src} and g_{ds} is the source resistance at the input terminal of the circuit and the transconductance between drain and source of the transistor, respectively. Therefore, the total noise voltage ($\overline{v_{in}^2}$) that appears at the input terminals of the circuits can be derived from the summation of the three noise sources.

$$\overline{v_{in}^2} = \overline{v_{1n}^2} + \overline{v_{2n}^2}\left(\frac{Z_{src}}{Z_{src} + j\omega L_1 + R_1}\right)^2 + \overline{i_{d1}^2}\left[\frac{Z_{src}}{g_{ds}(Z_{src} + j\omega L_1 + R_1)}\right]^2 \tag{13}$$

where

$$\overline{v_{1n}^2} = 4kTR_1\Delta f, \tag{14}$$

$$\overline{v_{2n}^2} = 4kTR_2\Delta f, \tag{15}$$

and

$$\overline{i_{d1}^2} = 4kT\gamma g_m \Delta f. \tag{16}$$

3. DESIGN OF A TUNABLE FILTER

Sections 3.1 and 3.2 introduces the filter topologies and the implementation of the bandpass filter in a standard 0.18-μm CMOS process, respectively.

3.1. Filter Topologies

LC-based bandpass filters consist of LC-ladder and coupled-resonator topologies. The ladder topologies utilize both series and parallel resonators with components spanning a wide range of values, and some of these components cannot be realized in a standard CMOS process at low-gigahertz frequencies. The coupled-resonator topology utilizes either series or parallel resonators with reasonable component values which is practical in a standard CMOS process. Two common coupled-resonator topologies are shunt-C coupled and series-C coupled networks. Fig. 7(a) shows a 2nd order shunt-C coupled bandpass filter using impedance (K) inverters. The shunt-C coupled topology is suitable for differential implementation, and is applied to a CMOS bandpass filter design successfully [16]. In order to reduce the number of the inductors, the K-inverters are realized by capacitive elements as shown in Fig. 7(b). However, the differential design doubles the number of inductors, and requires additional RF chokes and large coupling capacitor values.

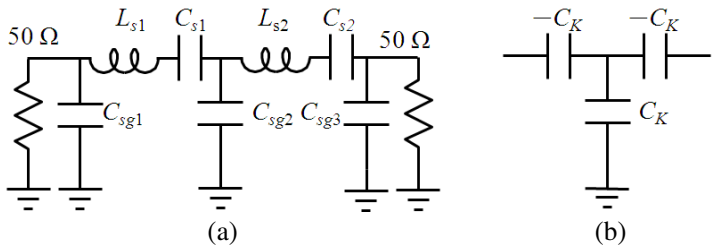

Figure 7. (a) A 2nd order shunt-C coupled bandpass filter. (b) The equivalent circuit of K-inverters.

A more suitable topology is series-C coupled bandpass filters using admittance (J) inverters which minimize the number of inductors as shown in Fig. 8(a). The J-inverters are also realized by capacitive elements as shown in Fig. 8(b), and the negative elements could be absorbed into adjacent elements. One advantage of coupled-resonator filter is the repeatability of the same resonator, which simplify filter tuning circuitry. For examples, the two resonators in Fig. 8(a) are the same, which represents $C_{p1} = C_{p2} = C_p$ and $L_{p1} = L_{p2} = L_p$. The center frequency (f_o) of the filter can be expressed as

$$f_o = \frac{1}{2\pi\sqrt{L_p C_p}}. \tag{17}$$

As shown in (17), the center frequency is decided by the resonators. Therefore, varactors can be introduced into the resonators for a tunable

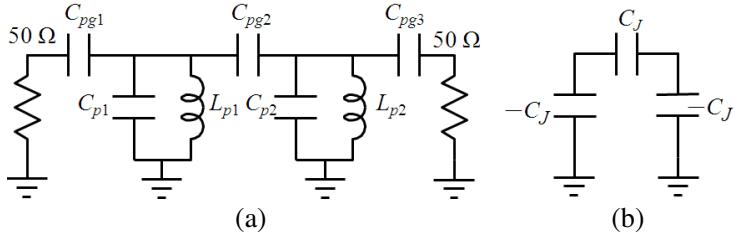

Figure 8. (a) A 2nd order series-C coupled bandpass filter. (b) The equivalent circuit of J-inverters.

bandpass filter design. The coupling capacitors C_{pg1}, C_{pg2}, and C_{pg3} which are all derived from the J-inverters (C_J) control the filter bandwidth.

3.2. Filter Implementation

Figure 9 shows the schematic of the tunable bandpass filter using Q-enhanced semi-passive inductors. The filter is a single-ended 2-pole Chebyshev bandpass filter, and the reference impedance is a 50 Ω termination to facilitate standard RF test equipment for on-chip measurements. The tuning range of the filter is from 2.65 GHz to 3 GHz. Moreover, the ratio between bandwidth and center frequency is more than 25% to avoid too small and impractical coupling capacitances when considering manufacturing process variation. The R, C_3, V_D, and aspect ratio of M_1 in Fig. 9 are 10 KΩ, 2 pF, 0.8 V, and (32 μm/0.18 μm), respectively. The width, spacing, and inner radius of the non-center-tapped inductor in Fig. 9 are 15 μm, 2 μm, and 95 μm, respectively. C_1 and C_2 and bypass capacitor, and C_a and C_b are coupling capacitors of the filter. V_G is a bias control for achieving different power consumption, and V_c is a bias control of varactors for center frequency tuning.

The filter is fabricated in a standard 0.18-μm CMOS process which provides one poly layer and six metal layers (1P6M). All the capacitors are implemented by metal-oxide-metal (MOM) capacitors which consist of five metal layers (from M_1 to M_5 layers). The area-scalable MOM capacitors can be designed easily with the capacitance of 1.1-fF/μm^2. The two pairs of varactors are realized by accumulation-type MOS varactors for high Q factors and wide tuning ranges. To minimize resistive losses, the tapped inductors are implemented on the top metal layer (M_6), or 2.3-μm-thick AlCu. Fig. 10 shows the chip photo of the bandpass filter with a chip area of 0.63 mm^2.

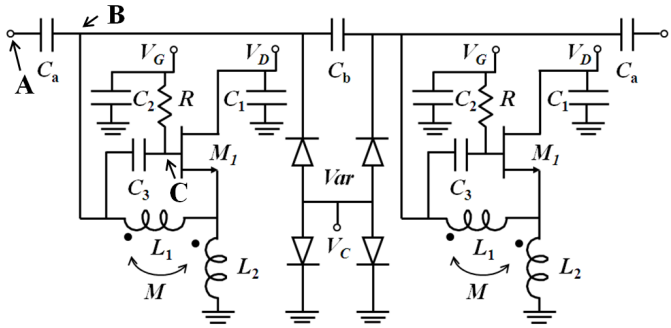

Figure 9. Schematic of the tunable bandpass filter using Q-enhanced semi-passive inductors.

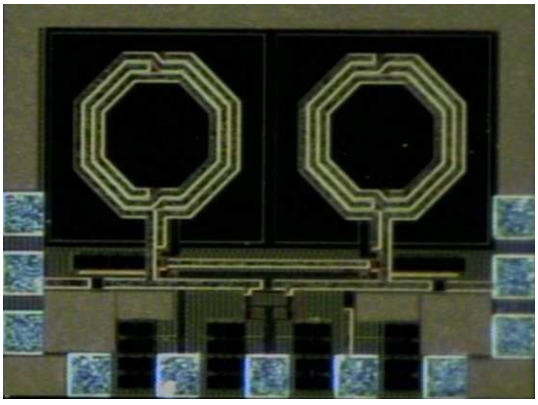

Figure 10. Chip photo of the bandpass filter with a chip size of 0.7 mm × 0.9 mm.

4. MEASUREMENTS AND DISCUSSIONS

The bandpass filter was measured using a vector network analyzer (VNA) through on-wafer probing. The small signal experiments are performed after the short-open-load-through (SLOT) calibration procedures to eliminate the parasitic of the ground-signal-ground (GSG) pads. Fig. 11 shows the simulated and measured results of the filter under different bias conditions. The total current of Fig. 11(a) is 3 mA from a 0.8 V supply voltage, and the control voltage of the varactors is 1 V. The measured results demonstrate that the center frequency of the filter is 2.8 GHz, and the bandwidth is 950 MHz with 1-dB insertion loss and 12-dB return loss. Similarly, the total current

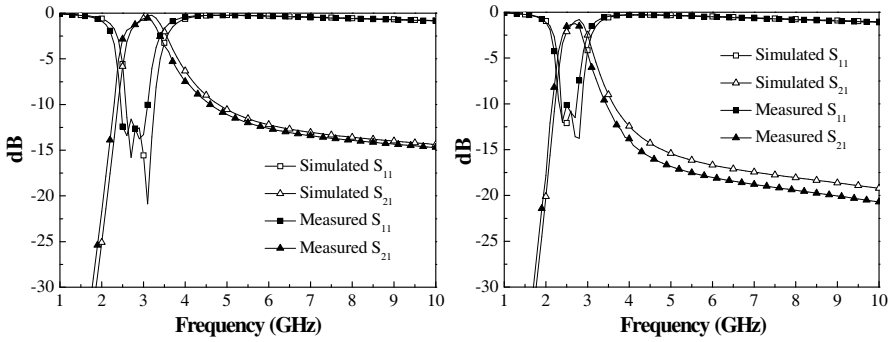

Figure 11. Simulated and measured frequency responses with different center frequencies. (a) 2.8 GHz, (b) 2.5 GHz.

of Fig. 11(b) is 7 mA from a 0.8 V supply voltage, and the control voltage of the varactor is −1 V. The measured results demonstrate that the center frequency of the filter is 2.5 GHz, and the bandwidth is 700 MHz with 1.5-dB insertion loss and 10-dB return loss. Therefore, the varactors in the filter provide a frequency tuning range of 300 MHz around 2.65 GHz. The simulated and measured frequency responses of Fig. 11 agree well, with only 100-MHz frequency drift which is induced by parasitic capacitances.

The Q-enhanced inductor is a 1-port device, or a grounded inductor making it difficult to apply conventional measures of linearity such as IP_3 and P_{1dB}. The main source of nonlinearity of the inductor is the transistor, and will occur when large signal swings (V_{gs}) are applied to pull M_1 into triode regions. The linearity of the series-C coupled filter can be discussed by applying a time domain signal at the source (node **A**), and observe signal levels at other nodes, as shown in Fig. 9. The signal at the input of the filter, or node **A**, is $32\,mV_{pk}$ as shown in Fig. 12(a). The simulated signal level at node **B** is $94\,mV_{pk}$, which is increased by the high impedance of the LC tank around resonant frequency. The voltage swings at node **C** is $100\,mV_{pk}$with V_G of 0.7 V as shown in Fig. 12(b). Equation (8) is derived from the small-signal model, which is related to g_m. The g_m can be regarded as a function of V_{gs} which contributes nonlinearities of the filter. As shown in Fig. 12(b), the simulated V_{gs} is mere $50\,mV_{pk}$, which is smaller than that at node **C**. The feedback loop avoids large V_{gs} swings, thus it can yield a high linearity.

As shown in Fig. 13(a), the measured input $P1_{dB}$ of the 2.5-GHz and 2.8-GHz filter are −4 dBm and −2.5 dBm, respectively. The

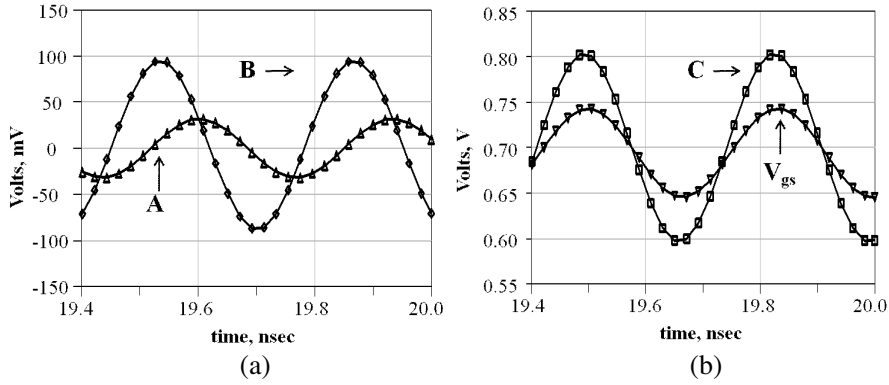

Figure 12. Simulated voltage levels at (a) node **A** and **B**, and (b) node **C** and V_{gs} of M_1 of the filter with a 2.8-GHz, -20 dBm available source power, or 32 mV_{pk} in a 50 Ω system.

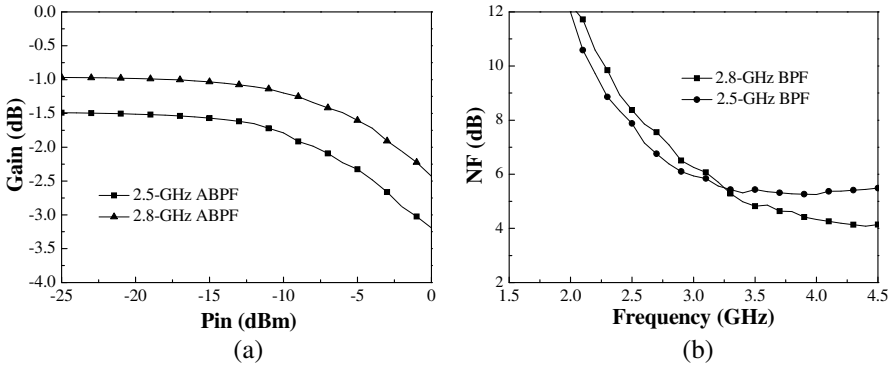

Figure 13. Measured (a) input $P_{1\text{dB}}$ and (b) NF of the tunable filter.

measured results demonstrate high $P_{1\text{dB}}$ characteristics as discussed before. Noise measurements were made with a spectrum analyzer equipped with noise power measurement software and a noise source. The measured NF of the 2.5-GHz and 2.8-GHz filter at theirs corresponding frequencies are 7.9 dB and 6.3 dB, respectively, as shown in Fig. 13(b).

A figure of merit (FOM) which allows comparison between RF bandpass filters is given as follows [15, 21]:

$$\text{FOM} = 10 \log \left(\frac{N \times P_{1\text{dBw}} \times f_o}{BW \times P_{DC} \times NF} \right). \tag{18}$$

where N is the order of filter, $P_{1\text{dBw}}$ is the in-band input compression

Table 1. Comparisons with the recently reported CMOS bandpass filters.

Reference	[16]	[15]	[21]	[9]	[22]	[18]	This Work	This Work
Process	0.25μm CMOS	0.18μm CMOS	0.25μm CMOS	0.5μm CMOS-SOI	0.35µm CMOS	0.18μm CMOS	0.18µm CMOS	0.18µm CMOS
Order (N)	3	4	2	2	2	3	2	2
f_o (GHz)	2.14	2	2.12	2.45	2.19	2.36	2.5	2.8
BW (MHz)	60	130	42	70	53.8	60	700	950
P_{DC} (mW)	5	16.6	65	15	5.2	8.8	5.6	2.4
NF (dB)	18.9	15	5.8	6	26.8	19	7.9	6.3
P_{1dB} (dBm)	−13.4	−6.6	−25	−15	−30	−20.4	−4	−2.5
Chip Size (mm^2)	1.89	1.21	0.4	2.5	0.1	2.25	0.63	0.63
FOM (dB)	74.3	77.1	64.4	79.6	48.6	65.6	83.1	89.6

point in Watt, f_o is the center frequency in Hertz, BW is the ratio of the 3-dB bandwidth and f_o, P_{DC} is the power consumption in Watt, and NF is the noise factor. Table 1 summarizes the previously reported CMOS bandpass filters. This work demonstrates the highest FOM due to its low-power consumption, low noise figure, and high linearity.

5. CONCLUSION

A fully-integrated bandpass filter using Q-enhanced and semi-passive inductors at S-band is design, implemented and verified experimentally in a standard 0.18-µm CMOS process. Electrical characteristics, stability, noise, and linearity analysis of the circuit are also described. The technique achieves high-Q inductors by using a tapped-inductor feedback to produce negative resistances. Compared with other Q-enhanced works, the proposed inductor not only compensates resistive losses with low-power consumption but also provides a high-inductance inductor which facilitates its potential use in RF filters. The tunable filter uses resonators built with the semi-passive inductors and accumulation-type varactors for frequency tuning. The 2-pole

Chebyshev series-C coupled bandpass filter provides a frequency tuning range of 300 MHz around 2.65 GHz, with low insertion loss, good return loss, and high linearity Compared with other CMOS bandpass filters, this work shows the highest FOM, mainly due to the low-power consumption, low noise figure, and high linearity. The demonstrated results of the filter shows the feasibility of designing low-power bandpass filters in mainstream CMOS technologies at S-band.

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