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ELECTROTHERMAL EFFECTS IN HIGH DENSITY THROUGH SILICON VIA (TSV) ARRAYS

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Abstract—Electrothermal effects in various through silicon via (TSV) arrays are investigated in this paper. An equivalent lumped-element circuit model of a TSV pair is derived. The temperature-dependent TSV capacitance, silicon substrate capacitance and conductance are examined for low-, medium-, and high-resistivity silicon substrates, respectively. The partial-element equivalent-circuit (PEEC) method is employed for calculating per-unit-length (p.u.l.) resistance, inductance, insertion loss and characteristic impedances of copper and polycrystalline silicon (poly-Si) TSV arrays, and their frequency- and temperature-dependent characteristics are treated rigorously. The modified time-domain finite-element method (TD-FEM), in the presence of a set of periodic differential-mode voltage pulses, is also employed for studying transient electrothermal responses of 4- and 5-TSV arrays made of different materials, with their maximum temperatures and thermal crosstalk characterized thoroughly.

1. INTRODUCTION

Through silicon via (TSV) technology is now playing more and more important role in the realization of high-density integrated 3-D systems with high functionality and high performance [1, 2]. Much efforts is now being devoted to the development of various fabrication technologies for achieving TSVs with high aspect ratio, low parasitic effect and good reliability [3].

TSV interconnects are usually made of damascene copper, and their electrical characteristics have been studied by some researchers

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more recently. For example, lumped-element circuit models of single-layer TSVs are derived in [2, 4] and [5], respectively, and some closed-form equations are given to determine their parasitic parameters and time delay of the transmitted signal. Slow-wave characteristics of a pair of TSVs used for power delivery in 3-D chip package are examined in [6], electromagnetic modeling of TSV interconnections using cylindrical modal basis functions is performed in [7], reduction technique of TSV capacitance is proposed in [8], with temperature dependent electrical characteristics of TSV interconnects studied in [9]. On the other hand, impact of thermo-mechanical stress on copper TSV reliability is investigated in [10], and multiphysics characterization of transient electrothermomechanical responses of multi-layered single copper, polycrystalline silicon and tungsten (W) TSVs applied with a periodic voltage pulse is performed in [11].

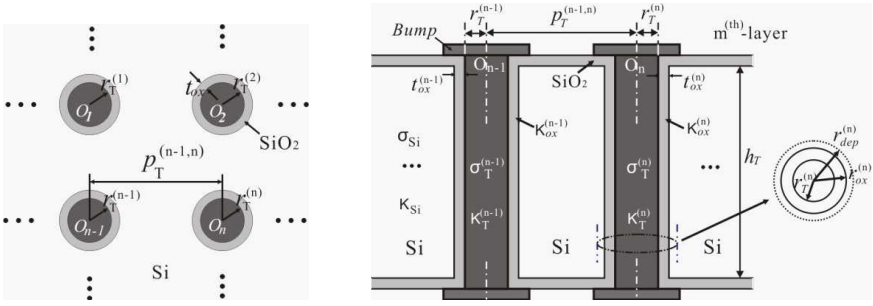
Although single TSV geometry is relatively simple, there are still some unsolved fundamental problems associated with high density TSV arrays, such as the derivation of their lumped-element circuit models, and fast extraction of their distributed parameters and characteristic impedances, etc. It is undoubtedly that high density TSV array integration will result in electromagnetic as well as thermal mutual couplings through silicon substrate, which will further degrade the transmitted signal quality and the performance of integrated 3-D systems. An appropriate treatment of self-heating effect among TSV arrays requires overall electrothermal analysis, optimization and management. On the other hand, it should be noticed that tungsten (W), the composite of poly-Si/W, and even carbon nanotube [5] can also be used for fabrication high density TSV arrays, which are different in material properties from that of damascene copper, respectively.

In this paper, our attention is focused on electrothermal effects in high density TSV arrays made of copper, poly-Si or tungsten (W) material, with their distributed parameters, insertion loss, characteristic impedance, transient electrothermal responses and thermal crosstalk all characterized numerically. The organization of this paper is as follows. In Section 2, the geometry of an arbitrary single-layered TSV array is given. In Section 3, an equivalent lumped-element circuit model of a TSV pair is derived, and the effects of frequency and temperature on the TSV capacitance, substrate capacitance and conductance are examined for low-, medium-, and high-resistivity silicon materials, respectively. In Section 4, partial-element equivalent-circuit (PEEC) method is implemented for calculating distributed parameters, insertion loss and characteristic impedances of some TSV arrays, with both frequency and temperature effects taken into account rigorously. In Section 5, time-domain

finite-element method (TD-FEM) is used for getting their transient maximum temperature in the presence of a set of periodic differential-mode voltage pulses, and thermal crosstalk among different TSVs are examined and compared for different cases. Some conclusions are drawn in Section 6.

2. DESCRIPTION OF HIGH DENSITY TSV ARRAYS

Figures 1(a) and (b) show the top and cross-sectional views of single-layered TSV array embedded into a silicon substrate characterized by resistivity ρ_{Si} ($\rho_{\mathrm{Si}} = 1/\sigma_{\mathrm{Si}}$) and thermal conductivity κ_{Si}. It is known that poly-Si enables us to fabricate TSV arrays with higher density, and copper and tungsten are suitable for interconnects with low electrical resistance required [1]. So, without loss any generality, such a TSV array in Fig. 1 can be made of copper, tungsten (W), poly-Si, and even the composite of poly-Si/W, respectively.



(a) (b)

Figure 1. (a) Top and (b) cross-sectional views of a single-layered high density TSV array embedded into a silicon substrate.

Here, we neglect the little difference between the top and bottom diameters of the high aspect ratio of TSV (aspect ratio10). The TSV cylinder, denoted by $n^{(th)}$, is described by the radius $r_T^{(n)}$, height h_T, electrical conductivity $\sigma_T^{(n)}$, and thermal conductivity $\kappa_T^{(n)}$ ($n = 1, \ldots,$ and N), respectively. For high density integration, we usually have $1\,\mu\mathrm{m} \leq 2r_T^{(n)} \leq 5\,\mu\mathrm{m}$, $10\,\mu\mathrm{m} \leq h_T \leq 5\,\mu\mathrm{m}$, and the TSV density will reach and even exceed $10^4/\mathrm{mm}^2$. The surrounding silicon oxide layer thickness of the $n^{(th)}$-TSV is denoted by $t_{ox}^{(n)}$, which is about hundreds of nanometers. It should be noted that the depletion layer radius $r_{dep}^{(n)}$ ($\leq r_{\max}^{(n)}$) around the $n^{(th)}$-TSV in Fig. 1(b) is voltage-

dependent [2, 4, 5, 8]. The pitch between $(n-1)^{(th)}$- and $n^{(th)}$-TSV is denoted by $p_T^{(n-1,n)}$. As $r_T^{(n-1)} = r_T^{(n)}$ and $t_{ox}^{(n-1)} = t_{ox}^{(n)}$, we have $p_T^{(n-1,n)} > 2(r_T^{(n)} + t_{ox}^{(n)})$. On the other hand, it should be pointed out that at each TSV end, one microbump must be introduced additional capacitive coupling among adjacent microbumps.

As the substrate is a p-type bulk silicon, the hole mobility at room temperature is a function of dopant impurity concentration, and given by [12]

$$\mu_p(300\,\mathrm{K}) = \frac{\mu_{\max} - \mu_{\min}}{1 + (N_a/N_{ref})^{\alpha}} + \mu_{\min} \tag{1}$$

where $\mu_{\max} = 495\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$, $\mu_{\min} = 47.7\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$, $\alpha = 0.76$, and $N_{ref} = 6.3 \times 10^{16}\,\mathrm{cm}^{-3}$. The parameter N_α represents the concentration of substrate dopant impurity, and the carrier mobility at high temperature is calculated by [13]

$$\mu_p(T) = \mu_p(T = 300\,\mathrm{K}) \cdot (T/300)^{-3/2} \tag{2}$$

Therefore, the temperature-dependent silicon conductivity is determined by

$$\sigma_{\mathrm{Si}}(T) = 1.602 \times 10^{-17} N_a \mu_p(T)\,(\mathrm{S/m}) \tag{3}$$

3. ELECTROTHERMAL PROPERTIES OF TSV PAIRS

For a TSV pair ($N = 2$), when $r_T^{(1)} = r_T^{(2)}$, $t_{ox}^{(1)} = t_{ox}^{(2)}$, $\sigma_T^{(1)} = \sigma_T^{(2)}$, and $\kappa_T^{(1)} = \kappa_T^{(2)}$, its equivalent lumped-element circuit model can be easily derived [14], as shown in Fig. 2, and

$$Z_{1\pm} = Z_{2\pm} = R_T + j\omega L_T = R_T + j\omega(L_s \pm M_{12}) \tag{4a}$$

$$Z_{12} = \frac{4G_{\mathrm{Si}}C_1 + j2\omega C_2}{-\omega^2(C_{ox}C_dC_{\mathrm{Si}} + 2C_{p1}C_2) + j\omega G_{\mathrm{Si}}(C_{ox}C_d + 4C_{p1}C_1)} \tag{4b}$$

$$Z_{21} = \frac{4G_{\mathrm{Si}}C_1 + j2\omega C_2}{-\omega^2(C_{ox}C_dC_{\mathrm{Si}} + 2C_{p2}C_2) + j\omega G_{\mathrm{Si}}(C_{ox}C_d + 4C_{p2}C_1)} \tag{4c}$$

where $C_1 = C_d + C_{ox}$, and $C_2 = C_dC_{ox} + 2C_dC_{\mathrm{Si}} + 2C_{ox}C_{\mathrm{Si}}$.

In Fig. 2, some explanations are given as follows.

1) The elements R_T and L_T represent the total resistance and inductance of the single TSV, respectively, and L_T includes both self (L_s) and mutual (M_{12}) inductances [15, 16].
2) The symbols "±" correspond to the cases of differential and common modes guided by the TSV pair, respectively.

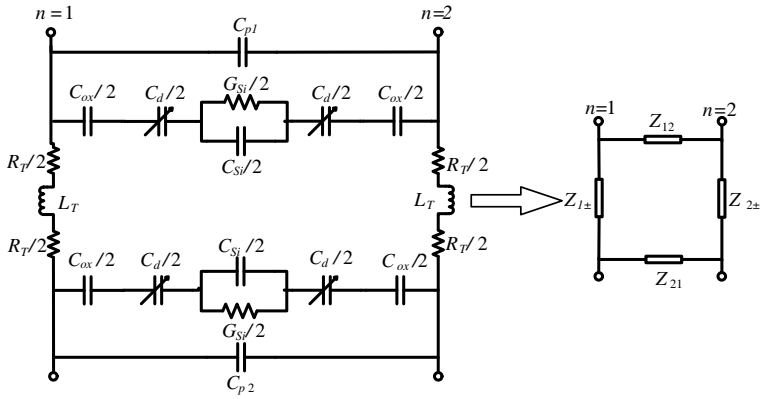


Figure 2. The equivalent lumped-element circuit model of a TSV pair consisting of both signal and ground vias.

3) The elements C_{p1} and C_{p2} are the capacitances of microbump to microbump at top and bottom ends of the TSVs, respectively, which can be very different from each other for real interconnection.
4) The elements C_{ox}, C_d and $C_{\rm Si}$ represent the capacitances of oxide isolation, depletion layer, and silicon substrate, respectively. They can be calculated by

$$C_{ox} = 2\pi\varepsilon_{ox}h_T/\ln\left[r_{ox}^{(1)}/r_T^{(2)}\right] \tag{5a}$$

$$C_d = 2\pi\varepsilon_{Si}h_T/\ln\left[r_{dep}^{(1)}/r_{ox}^{(2)}\right] \tag{5b}$$

and [5]

$$C_{\rm Si} = \pi\varepsilon_{\rm Si}h_T/\cosh^{-1}\left[0.5p_T^{(1,2)}/r_{dep}^{(1)}\right] \tag{5c}$$

5) The element $G_{\rm Si}$ is the substrate conductance determined by $G_{\rm Si} = \sigma_{\rm Si}C_{\rm Si}/\varepsilon_{\rm Si}$ [17].

It should be emphasized that R_T, C_d, $C_{\rm Si}$ and $G_{\rm Si}$ are all frequency- and temperature-dependent. To calculate R_T and L_T, a set of closed-form equations proposed in [5], can be employed. On the other hand, we know that, when the threshold point of the applied voltage of single TSV is reached, the radius $r_{dep}^{(1)}$ will get its maximum $r_{\rm max}^{(1)}$, and determined by

$$2V_t\ln\left(\frac{N_a}{n_i}\right) = \frac{qN_a}{2\varepsilon_{\rm Si}}\left[\left(r_{\rm max}^{(1)}\right)^2\ln\left(\frac{r_{\rm max}^{(1)}}{r_{ox}^{(1)}}\right) - \frac{\left(r_{\rm max}^{(1)}\right)^2 - \left(r_{ox}^{(1)}\right)^2}{2}\right] \tag{6}$$

where V_t is the thermal voltage, n_i is the intrinsic carrier concentration, and q is the electron charge.

Based on [4, 5] and (6), the effects of both applied voltage and operating temperature on the depletion radius $r_{dep}^{(1)}$ and p.u.l. capacitance C_T of a copper TSV are examined and plotted in Figs. 3(a) and (b), respectively, with $r_T^{(1)} = 0.75\,\mu\text{m}$, $h_T = 30\,\mu\text{m}$, $t_{ox}^{(1)} = 0.1\,\mu\text{m}$, and $N_a = 1.25\times10^{15}\,\text{cm}^{-3}$ for silicon substrate with medium resistivity. On the other hand, we would like to point out that in the fabrication of a copper TSV, a very thin barrier layer, such as Ta, TaN or TiN, must be introduced between copper and SiO_2, and its work function (Ta/TaN $\sim 4.25\,\text{eV}$) is different from that of copper ($\sim 4.7\,\text{eV}$), which is taken into account in our calculation.

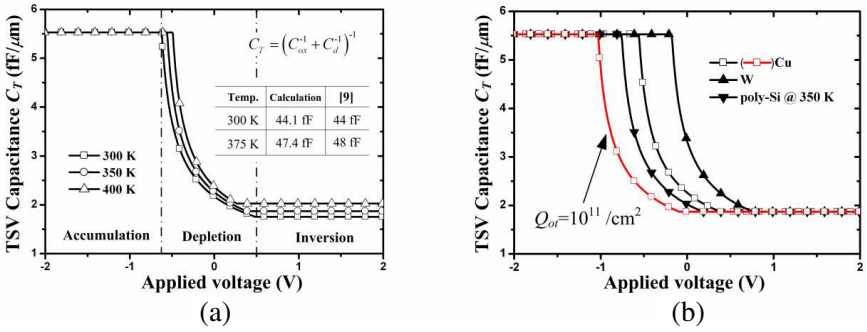


Figure 3. (a) P.u.l. capacitance C_T of a copper TSV as a function of its applied voltage V_a at different temperatures, respectively. (b) P.u.l. capacitances C_T of copper, tungsten (W) and poly-Si TSVs.

With respect to Fig. 3, some key points are explained as follows.

1) There are three distinct regions including accumulation ($V_a < V_{FB}$), depletion ($V_{FB} \le V_a \le V_{th}$) and inversion ($V_a > V_{th}$) regions, respectively.
2) There is only oxide capacitance C_{ox} in the accumulation region. As the value of V_a exceeds the flatband voltage V_{FB}, depletion capacitance C_d appears, which results in the decrease of C_T. When the applied voltage V_a exceeds the threshold voltage V_{th} in the inversion region, TSV capacitance C_T reaches its minimum.
3) Except in the accumulation region, the TSV capacitance C_T is sensitive to the variation of temperature. For example, in the inversion region, as temperature rises from 300 to 400 K, it is increased from 0.66 to 0.74 fF/μm. Also, both V_{FB} and V_{th} are sensitive to the variation of temperature.

4) The inset in Fig. 3(a) shows the comparison between our calculated results with the measured ones [9] at different temperatures, where the doping concentration is chosen to be an appropriate value of $3 \times 10^{15}\,\mathrm{cm}^{-3}$. We would like to say that good agreement is obtained here.
5) At $T = 350\,\mathrm{K}$, some comparisons in the value of C_T among copper, tungsten (W) and poly-Si TSVs are made in Fig. 3(b). For the same geometry given, the change in TSV material just shifts the voltages of V_{FB} and V_{th}, and it has little effect on the value of C_T.
6) Since the doping concentration N_p of poly-Si ($10^{19} \sim 10^{20}\,\mathrm{cm}^{-3}$) is much larger than $N_a (= 1.25 \times 10^{15}\,\mathrm{cm}^{-3})$ [18], the depletion layer thickness in the poly-Si TSV is only about several nanometers, which results in very large poly-Si depletion capacitance, and therefore, the poly-Si depletion effect can be excluded in the calculation of C_T.
7) For a copper TSV, as we take oxide charges at the Si/SiO2 interface etc. into account, the threshold voltage will be more negative than that of $Q_{ot} = 0$ case, where Q_{ot} represents the total oxide charge density [2].

As temperature varies, the total capacitance C_T of copper TSV with $V_a = 0.15\,\mathrm{V}$ is plotted in Fig. 4 for low, medium and high resistivity silicon (LRS, MRS and HRS) substrates, respectively. Two points are explained as follows.

1) At given temperature, the increase in ρ_{Si} $(= 1/\sigma_{\mathrm{Si}})$ means that the doping concentration N_a is reduced, which causes the increase of $r_{dep}^{(1)}$ and further the decrease of C_T.
2) As temperature increases from 300 to 400 K, the value of C_T for HRS case is increased slightly, while for LRS it is almost unchanged.

We know that the intrinsic concentration n_i is directly proportional to temperature. For HRS case, as temperature increases, the ratio of N_a/n_i is changed significantly, which further results in the increase of C_T. In Fig. 4, the relative increase ratios in C_T for LRS, MRS and HRS substrates are about 1.76, 11.46 and 19.33%, respectively.

Figure 5 shows the substrate capacitance C_{Si} and conductance G_{Si} as a function of temperature for different applied voltages, with (3) implemented for our calculation. It is shown that as V_a=1.0 V, the value of C_{Si} is reduced from 0.39 to $0.37\,\mathrm{fF/\mu m}$. As $V_a = 1.5\,\mathrm{V}$, it is reduced from 0.53 to $0.42\,\mathrm{fF/\mu m}$. Correspondingly, the value of G_{Si} is reduced from 36.2 to 21.8 S/m and from 48.9 to 25.1 S/m, respectively.

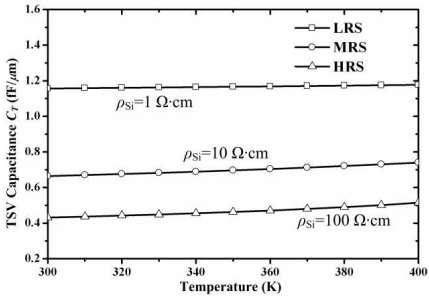


Figure 4. P.u.l. capacitance C_T of a copper TSV as a function of temperature for LRS, MRS and HRS substrates, respectively. The parameter N_a is unchanged here.

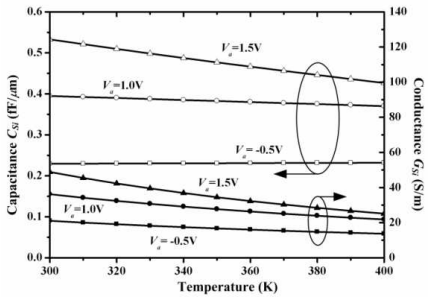


Figure 5. P.u.l. capacitance C_{Si} and conductance G_{Si} of copper TSV as a function of temperature for different applied voltages.

On the other hand, it should be noted that smaller diameter of TSV is better for the reduction of its parasitic capacitance as well as substrate conductance.

4. PARAMETER EXTRACTION OF TSV ARRAYS

4.1. Resistance and Inductance

For a TSV array of $N \geq 3$, there is no analytical equation for predicting its frequency- and temperature-dependent resistances and inductances; we must look for an appropriate numerical solution for them, in which mutual inductive couplings among all TSVs must be treated rigorously. Therefore, the partial-element equivalent-circuit (PEEC) method [19] is used to handle various TSV array ($N \geq 3$). The PEEC method is a numerical approach that meshes metallic TSV arrays into small filaments, and then solves them in a discrete manner. Its implementation for $N = 4$ case is plotted in Fig. 6. Some key points in its implementation are briefly summarized as follows.

1) The $n^{(th)}$-TSV is divided into $P_{fil}^{(n)}$ filaments, and $P_{fil}^{(n)}$ depends on the operating frequency and accuracy required. The higher the frequency, the larger number of $P_{fil}^{(n)}$ will be. As the radii of all TSVs are different, $P_{fil}^{(1)}$ can be different from $P_{fil}^{(2)}$, ..., and $P_{fil}^{(N)}$.
2) The current flowing through each TSV is a constant. As indicated in Fig. 6, $I_p^{(n)}$, $L_p^{(n)}$ and $R_p^{(n)}$ ($p = 1, \ldots,$ and $P_{fil}^{(n)}$; $n =$

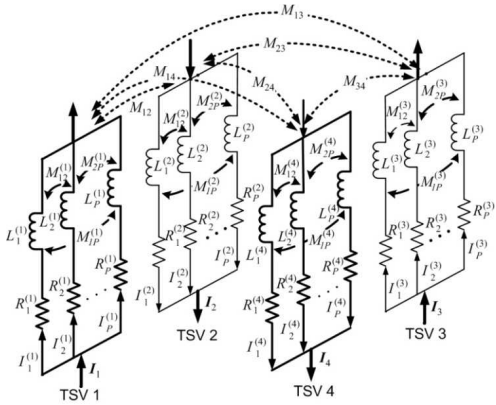


Figure 6. The PEEC model of a 4-TSV array with common mode transmission. Signal: TSV 1 and 3. Ground: TSV 2 and 4.

1, ..., and N) in each interconnect represent the flowing current, self inductance and resistance of the filament, respectively.

3) The mutual inductances between different filaments in the $n^{(th)}$-TSV in Fig. 6 are represented by $M_{mn}^{(n)}$, while the mutual inductance between the $m^{(th)}$- and the $n^{(th)}$-TSVs is denoted by M_{mn}.

According to the Ohm's law, the voltages and currents of all filaments in Fig. 6 can be expressed by

$$\begin{bmatrix} \mathbf{V}_1 \\ \mathbf{V}_2 \\ \vdots \\ \mathbf{V}_N \end{bmatrix} = \begin{bmatrix} \tilde{\mathbf{Z}}_{11}(f,T) & \tilde{\mathbf{Z}}_{12}(f,T) & \dots & \tilde{\mathbf{Z}}_{1N}(f,T) \\ \tilde{\mathbf{Z}}_{21}(f,T) & \tilde{\mathbf{Z}}_{22}(f,T) & \dots & \tilde{\mathbf{Z}}_{2N}(f,T) \\ \vdots & \vdots & \ddots & \vdots \\ \tilde{\mathbf{Z}}_{N1}(f,T) & \tilde{\mathbf{Z}}_{N2}(f,T) & \dots & \tilde{\mathbf{Z}}_{NN}(f,T) \end{bmatrix} \begin{bmatrix} \mathbf{I}_1 \\ \mathbf{I}_2 \\ \vdots \\ \mathbf{I}_N \end{bmatrix} \quad (7)$$

where $\{\mathbf{V_n}\}$ and $\{\mathbf{I_n}\}$ represent the voltage and current matrices of the $n^{(th)}$-TSV, and they are a $P_{fil}^{(n)}$-dimensional vector, respectively. $\tilde{Z}_{mn}(f,\ T)$ is an impedance matrix of $P_{fil}^{(m)} \times P_{fil}^{(n)}$, whose element is given by

$$Z_{mn}^{pq}(f,T) = \begin{cases} R_m^p(T) + j\omega L_m^p, & (m=n,\ p=q) \\ M_{mn}^{pq}, & \text{else} \end{cases} \quad (8)$$

where $R_m^p(T)$ and L_m^p represent the temperature-dependent DC resistance and inductance of the $p^{(th)}$-filament in the $m^{(th)}$-TSV,

respectively. M_{mn}^{pq} is the mutual inductance between the $p^{(th)}$-filament of the $m^{(th)}$-TSV and the $q^{(th)}$-filament of the $n^{(th)}$-TSV.

For each TSV in Fig. 6, we have

$$V_n = \mathbf{V}_n(p), \quad p = 1, \ldots, \quad \text{and} \quad P_{fil}^{(n)} \tag{9a}$$

$$I_n = \sum_{p=1}^{P_{fil}^{(n)}} \mathbf{I}_n(p) \tag{9b}$$

where V_i and I_i are the voltage and current of the TSV in the array, respectively. Inverting (7) and after some mathematical treatments, we can obtain each element in the $[Z]$-matrix. Further, the series resistance and inductance of the $m^{(th)}$-TSV are calculated by

$$R_m(f,T) = \mathrm{Re}\left\{\sum_{n=1}^{N}[Z_{mn}(f,T)(I_n/I_m)]\right\} \tag{10a}$$

$$L_m(f,T) = \mathrm{Im}\left\{\sum_{n=1}^{N}[Z_{mn}(f,T)(I_n/I_m)]\right\} \Big/ \omega \tag{10b}$$

It should be emphasized that because the electrical conductivity of silicon substrate is much smaller than that of copper or tungsten (W) materials, the impact of eddy current in silicon substrate on both resistance and inductance is excluded here [20], and (10a) and (10b) only represent the frequency- and temperature-dependent resistance and inductance of the TSV array itself.

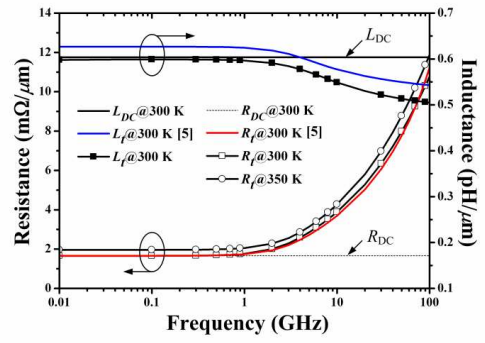


Figure 7. P.u.l. resistance $R_{pul}^{(\mathrm{Cu})}$ and inductance $L_{pul}^{(\mathrm{Cu})}$ of a TSV pair as a function of frequency at different temperature.

At $T = 300\,\mathrm{K}$, Fig. 7 shows the total p.u.l. resistance $R_{pul}^{(\mathrm{Cu})}$ and inductance $L_{pul}^{(\mathrm{Cu})}$ of a copper TSV pair carried with a set of differential-mode signals, and $r_T^{(1)}$=$r_T^{(2)} = 0.75\,\mu\mathrm{m}$, $t_{ox}^{(1)}$=$t_{ox}^{(2)} = 0.1\,\mu\mathrm{m}$, $p_T^{(1,2)} = 3.7\,\mu\mathrm{m}$, and $h_T = 30\,\mu\mathrm{m}$. It is evident that good agreement is obtained between the results obtained by the PEEC method and that of presented in [5]. The temperature effect on $R_{pul}^{(\mathrm{Cu})}$ of copper TSV pair is observable, and the DC case is also plotted for comparison. Based on some numerical experiments, it is found that $R_{pul}^{(\mathrm{Cu})}$ can be predicted by

$$R_{pul}^{(\mathrm{Cu})}(T) = R_{pul}^{(\mathrm{Cu})}|_{T_0=300\ \mathrm{K}}\,[1 + \alpha(f)(T - 300)] \tag{11}$$

where $\alpha(f)$ is the temperature coefficient of copper resistivity. At low frequencies, it is about 0.00370/K, which agrees well that given in [9]. At high frequencies, we have $\alpha|_{f=20\,\mathrm{GHz}} \approx 0.00237$/K and $\alpha|_{f=50\,\mathrm{GHz}} \approx 0.00161$/K approximately.

Further, Figs. 8(a) and (b) show the calculated $R_{pul}^{(\mathrm{Cu})}$ and $L_{pul}^{(\mathrm{Cu})}$ of 4- and 6-TSV arrays at different temperatures, respectively. The parameters used for calculation are the same as in Fig. 7, and the current flowing direction in each TSV indicated at its center. It is evident that, at a given frequency, the p.u.l. resistance increases significantly with temperature. For example, as temperature increases from 300 to 400 K, the relative increase in $R_{pul}^{(\mathrm{Cu})}|_{f=1\,\mathrm{GHz}}$ is about 31.2%. In particular, at high frequencies, both $R_{pul}^{(\mathrm{Cu})}$ and $L_{pul}^{(\mathrm{Cu})}$ change fast

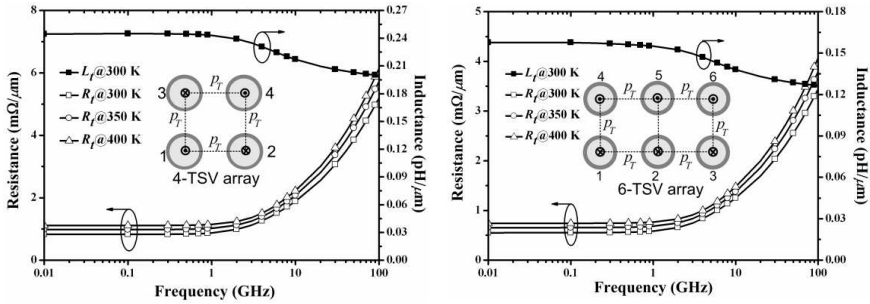


Figure 8. P.u.l. resistance $R_{pul}^{(\mathrm{Cu})}$ and inductance $L_{pul}^{(\mathrm{Cu})}$ of (a) 4- and (b) 6-TSV arrays as a function of frequency for different temperatures, respectively.

with frequency increasing.

Moreover, both $R_{pul}^{(\text{poly-Si})}$ and $L_{pul}^{(\text{poly-Si})}$ of a 4-TSV array made of poly-Si are plotted in Fig. 9 for comparison. Since the electrical conductivity of poly-Si is much smaller than that of copper, at the same frequency, we have $R_{pul}^{(\text{poly-Si})} \gg R_{pul}^{(\text{Cu})}$, and it is not sensitive to the variation of frequency from DC to several tens GHz. Similar to (11), we also get

$$R_{pul}^{(\text{poly-Si})}(T) = R_{pul}^{\text{poly-Si}}|_{T_0=300\text{ K}}\,[1+\alpha(T-300)] \tag{12}$$

where $\alpha \approx 0.001/\text{K}$.

4.2. Insertion Loss

The transmitted signal quality of a TSV array can be understood by seeing its insertion loss [21, 22], which is denoted by the magnitude of S_{21}-parameter and plotted in Fig. 10 at $T = 300\,\text{K}$ for LRS, MRS and HRS substrates, respectively, with $T = 400\,\text{K}$ case for MRS substrate also plotted for comparison.

In Fig 10, we choose $r_T^{(1)}{=}r_T^{(2)} = 2.5\,\mu\text{m}$, $t_{ox}^{(1)} = t_{ox}^{(2)} = 0.1\,\mu\text{m}$, $h_T = 50\,\mu\text{m}$, and $p_T^{(1,2)} = 15\,\mu\text{m}$. It is observed that, in particular for LRS case, the higher the operating frequency, the more serious of the TSV insertion loss will be. Good agreements are obtained between our results and those of commercial software CST. In CST, the TSVs are excited with lumped ports on their top and bottom surfaces, and the depletion regions are modeled as lossless dielectric, because

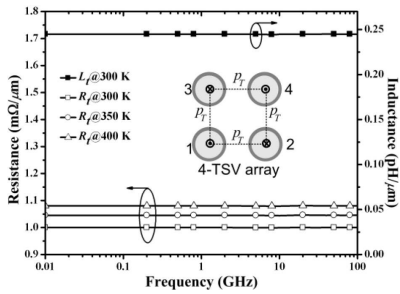


Figure 9. P.u.l. resistance $R_{pul}^{(\text{poly-Si})}$ and inductance $L_{pul}^{(\text{poly-Si})}$ of a 4-TSV array as a function of frequency at different temperatures.

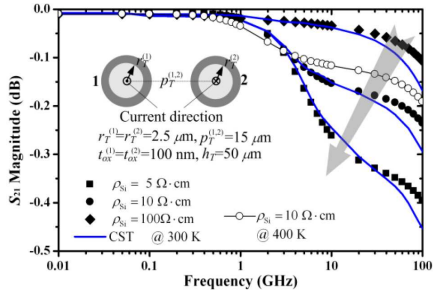


Figure 10. Magnitude of S_{21}-parameter of a TSV pair as a function of frequency for different silicon resistivities and temperatures.

these regions are depleted with mobile charge carriers [4]. The better flatness of S_{21}-parameter can guarantee small jitter of the transmission signal [6].

4.3. Characteristic Impedance

The characteristic impedance of a copper, poly-Si or tungsten TSV array above can be calculated by [22]

$$Z_0(f,\ T) = \mathrm{Re}(Z_0) + j\mathrm{Im}(Z_0) = \sqrt{\frac{R_{pul} + j\omega L_{pul}}{G_{pul} + j\omega C_{pul}}} \tag{13}$$

where R_{pul} and L_{pul} are also calculated using the above PEEC method. The C_{pul} of a square 4-TSV array, as shown in Fig. 11(a), can be determined by

$$C_{pul} = \mathrm{Im}\left\{[(j\omega 2C_T)^{-1} + (4Y)^{-1} + (j\omega 2C_T)^{-1}]^{-1}\right\}/\omega \tag{14}$$

where $Y = G_{\mathrm{Si}} + j\omega C_{\mathrm{Si}}$, and ω is the angular frequency. For the circular $2N$-TSV array (Fig. 11(b)), as it is embedded into the high-resistivity silicon substrate with the effect of silicon isolation layer excluded, its quasi-static characteristic impedance can be evaluated by [23]

$$\begin{aligned}\tilde{Z}_0 &= \sqrt{L_{pul}/C_{pul}} \\ &= 120\cosh^{-1}\left[1\Big/\sin\left(N\sin^{-1}(r_T^{(n)}/R)\right)\right]\Big/(N\sqrt{\varepsilon_{si}}),\ R \gg r_T^{(n)}\end{aligned} \tag{15}$$

where all TSVs have the same radius and the same pitch between two neighbors.

Figure 12 shows the frequency-dependent $\mathrm{Re}\,(Z_0)$ of the copper 4-TSV array at $T = 400$ K for different silicon resistivities, with

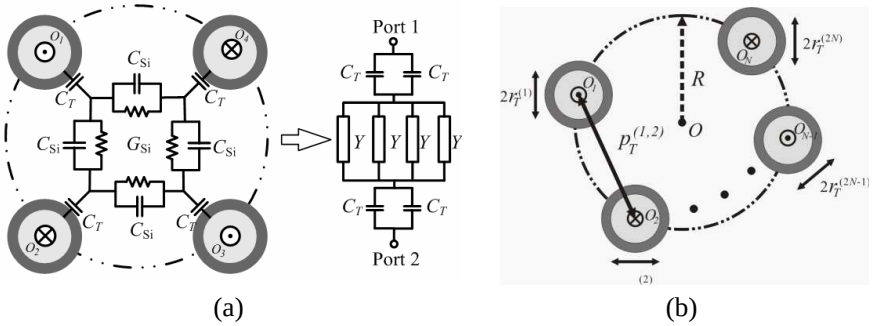


Figure 11. (a) Cross-sectional view of a square 4-TSV array with its simplified equivalent circuit model. (b) Circular $2N$-TSV array.

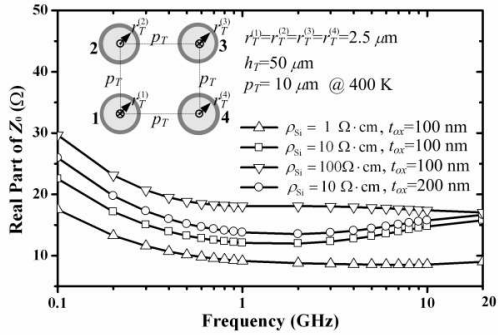


Figure 12. Real part of characteristic impedance of a copper 4-TSV as a function of frequency for different silicon resistivities.

$r_T^{(n)}$=2.5 µm, $t_{ox}^{(n)}$ = 0.1 µm (n = 1, 2, 3 and 4), h_T = 0 µm and p_T = 10 µm. It is observed that at a given frequency it increases with increasing the silicon resistivity.

5. TRANSIENT THERMAL RESPONSES OF TSV ARRAYS

Using our developed hybrid time-domain finite element method (TD-FEM) [11, 24, 25], both thermal responses and mutual coupling effects of some TSV arrays above can be obtained numerically, where the 3-D transient heat conduction equation is described by

$$\begin{cases} \rho c \frac{\partial T(\vec{r},t)}{\partial t} + \nabla \left[\kappa(T) \nabla T(\vec{r},t) \right] = f_1(\vec{r},T,t) \\ T|_{\Gamma_a} = T_a \\ \frac{\partial T}{\partial n}|_{\Gamma_q} = -h(T-T_a)|_{\Gamma_q} \end{cases} \tag{16}$$

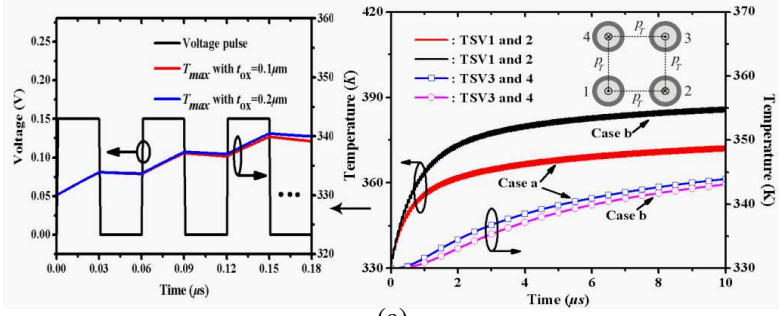
and all parameters related can be referred in [11]. The applied periodic voltage pulse $U_P(t)$ on the TSV array is assumed to be

$$U_P(t) = \sum_{k=0}^{n_k} U_0(t - kT_0) \tag{17}$$

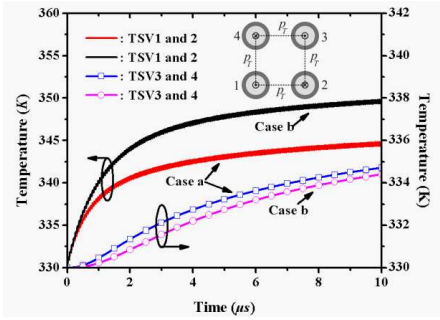
where T_0 is the pulse period, $k = 0, \ldots,$ and n_k. For the rectangular pulse case, we have

$$U_0(t) = \begin{cases} U_{0\max}, & 0 < t \le t_w \\ 0, & t_w < t < T_0 \end{cases} \tag{18}$$

where t_w is the single pulse width, and $U_{0\max}$ is the pulse magnitude.



(a)



(b)

Figure 13. The maximum temperatures of (a) a copper and (b) a tungsten (W) 4-TSV arrays for different values of $t_{ox}^{(i)}$ (i = 1, 2, 3 and 4), with $U_{0\,\max}^{(p)} = 0.15\,\mathrm{V}$, $t_w^{(p)} = 0.5T_0^{(p)} = 30\,\mathrm{ns}$ (p = 1 and 2). Case (a) $t_{ox}^{(i)} = 0.1\,\mu\mathrm{m}$, and Case (b) $t_{ox}^{(i)} = 0.2\,\mu\mathrm{m}$.

Figures 13(a) and (b) show the maximum temperatures of copper and tungsten 4-TSV arrays, respectively. Their geometries are the same as assumed above, and a couple of rectangular differential-mode voltage pulses are only applied on TSV 1 and 2 at the same time.

Some explanations for Figs. 13(a) and (b) are given as follows.

1) The maximum temperature of each TSV, denoted by $T_{\max}^{(i)}$ (i = 1, 2, 3 and 4),, tends to a steady-state oscillation with time increasing, respectively.
2) The thicker the silicon oxide layer, the higher temperature of the TSV 1 or 2 is reached, because the thermal conductivity of silicon oxide is much smaller than that of silicon. For both copper TSV 1 and 2, as $t_{ox}^{(i)} = 0.1$ and $0.2\,\mu\mathrm{m}$, $T_{\max}^{(1)} = T_{\max}^{(2)}$ =372.4 and 386.1 K at $t = 10\,\mu\mathrm{s}$, respectively. While for the tungsten 4-TSV array,

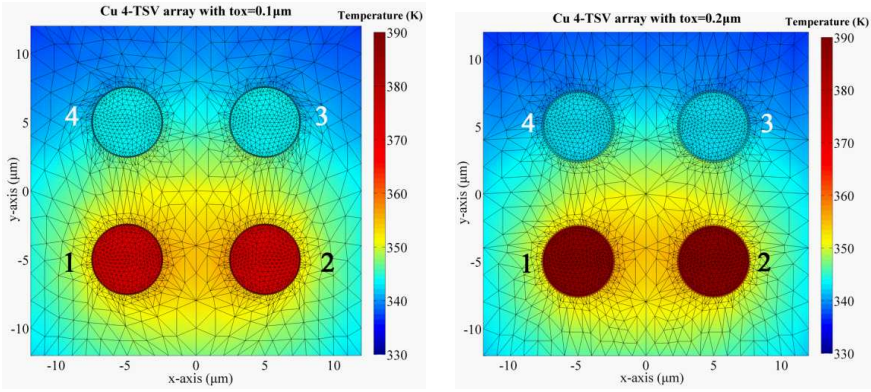


Figure 14. Temperature distributions of the copper 4-TSV arrays at $t = 10\,\mu s$, with (a) $t_{ox}^{(i)} = 0.1\,\mu m$ and (b) $t_{ox}^{(i)} = 0.2\,\mu m$ ($i = 1, 2, 3$ and 4).

we have $T_{\max}^{(1)} = T_{\max}^{(2)} = 344.7$ and $349.7\,K$, respectively.

3) The thermal crosstalk or thermal mutual coupling between TSV 1 & 2 and TSV 3 & 4 is observable as $t_{ox}^{(i)}$ ($i = 1$, 2, 3 and 4) are varied, as indicated above.

At $t = 10\,\mu s$, the temperature distributions of the above copper 4-TSV array are plotted in Figs. 14(a) and (b) for comparison, and the thermal crosstalk between TSV 1 & 2 and TSV 3 & 4 in each array is demonstrated clearly.

In comparison with Fig. 13, the maximum temperatures of a poly-Si 4-TSV array are plotted in Fig. 15. It should be emphasized that, although similar steady-state oscillations of the maximum temperatures are observed, the applied pulse voltage magnitude in Fig. 15 is much higher than that of copper or tungsten TSV array case. Also, they are sensitive to the variation of silicon oxide layer thickness.

Finally, the maximum temperatures of a copper 5-TSV array are plotted in Fig. 16, with a set of rectangular differential-mode voltage pulses applied on TSV 1 to 5 at the same time, $U_{0\max}^{(1)} = 4U_{0\max}^{(q)} = 0.15$ V ($q = 2,\ 3,\ 4$ and 5), $t_w^{(p)} = 0.5T_0^{(p)} = 30$ ns, and $t_{ox}^{(p)} = 0.1\,\mu m$ ($p = 1$ to 5). Due to the array symmetry, TSV 2, 3, 4 and 5 have the same maximum temperature.

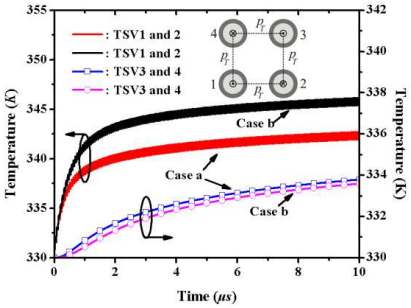


Figure 15. The maximum temperatures of a poly-Si 4-TSV array for different value of $t_{ox}^{(i)}$, with $t_w^{(p)} = 0.5T_0^{(p)} = 30$ ns, and $U_{0\max}^{(p)}$=2.5 V ($p = 1$ and 2).

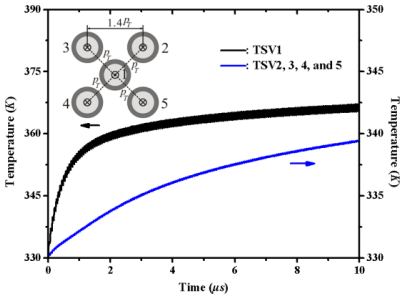


Figure 16. The maximum temperatures of a copper 5-TSV array with a set of rectangular differential-mode voltage pulses applied on TSV 1 to 5.

6. CONCLUSION

In this paper, electrothermal effects in various through silicon via (TSV) arrays made of damascene copper, polycrystalline silicon and tungsten are investigated numerically. Based on the equivalent lumped-element circuit model of TSV pair, the TSV capacitance, substrate capacitance and conductance for different temperatures and applied voltages are examined for low-, medium-, and high-resistivity silicon substrates, respectively. Further, the partial-element equivalent-circuit (PEEC) method is employed to calculated p.u.l. resistance, inductance and characteristic impedance of some typical copper and polycrystalline silicon TSV arrays, respectively. In the presence of a set of periodic differential-mode voltage pulses, the modified time-domain finite-element method (TD-FEM) is also implemented for predicting transient thermal responses of 4- and 5-TSV arrays made of different materials, and thermal crosstalk or thermal mutual coupling among TSVs are characterized thoroughly. The above study will be useful for further developing high density TSV interconnects with good electromagnetic as well as electrothermal compatibility. Of course, experimental study needs to be carried out so as to validate the above numerical results in detail, and even including mechanical effects on TSV performance, etc.

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