COPLANAR RING DIVIDER WITH WIDEBAND HIGH ISOLATION PERFORMANCE

C. Li[*], L. B. Lok, A. Khalid, and D. R. S. Cumming

MicroSystem Technology Group, School of Engineering, University of Glasgow, Glasgow G12 8LT, UK

Abstract—In this letter, the design and measurement of a new ring power divider exhibiting wideband high isolation is presented. Coplanar techniques are used to achieve a compact and truly uniplanar design. The design is demonstrated by a prototype, operating at K-band, that has been monolithically fabricated using a GaAs MMIC process with airbridge technology. The measured insertion loss is 0.6 dB at the center design frequency of 25 GHz. The output port isolation is better than 20 dB across a wide bandwidth from 10 MHz to 50 GHz. The output amplitude and phase balance is within ±0.5 dB and ±2°, respectively, in the bandwidth from 10 MHz to 43 GHz.

1. INTRODUCTION

Wilkinson dividers are elementary passive components that are extensively used for in-phase power splitting and combining applications. When combining active devices with high power, port isolation performance at frequencies in-band and out-of-band are very important in order to suppress unwanted feedback and avoid undesirable oscillations [1]. Unfortunately, the conventional Wilkinson divider has a port isolation performance that is narrowband.

A modified form of the Wilkinson divider to achieve a broadband isolation response was proposed by Xue et al. [2]. They replaced the single isolation resistor with a lumped-distributed network that comprised two quarter-wavelength transmission lines, a phase inverter, and two resistors. The topology was demonstrated using parallel striplines (PS) and made use of two through substrate vias to form the phase inverter. The tapered baluns also required in the design

---

occupied a large proportion of the overall circuit area. Two uniplanar implementations were later realized using slotline and asymmetric coplanar stripline [3]. The disadvantage of these is the greater occupied area due to the quarter-wavelength radial stubs used in the design.

In this paper, we propose a new compact ring divider design using a combination of symmetrical coplanar striplines (SCPS) and coplanar waveguides (CPW). This enables the phase inverter to be realized using an airbridge cross-over [4] that twists the signal and ground paths of a coplanar stripline. Compared to other implementations, this results in minimal parasitics and no significant penalty of increased circuit area. The proposed coplanar design can therefore be fabricated with a smaller size. More reliable performance is expected.

2. DESIGN

2.1. Synthesis

A simplified layout of the proposed ring power divider is shown in Figure 1. It comprises four quarter-wave coupled lines that are connected in a ring configuration. The transition to coplanar waveguide ports are accomplished by compact dual baluns [5] that are formed by two CPW to SCPS tee-junctions [6]. The phase inverter is implemented using a single airbridge cross-over. Three other airbridges
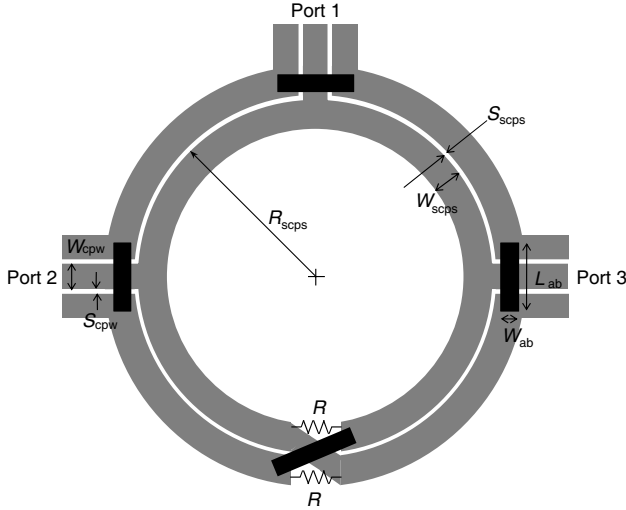
Figure 1. Simplified layout view of the SCPS ring divider.

are used to equalize the ground potentials in the CPW-to-SCPS balun transition.

The odd and even mode impedances of the ideal coupled-lines are given by:

$$Z_{0o} = Z_0^{\text{SCPS}} \sqrt{\frac{1-k}{1+k}} \tag{1}$$

$$Z_{0e} = Z_0^{\text{SCPS}} \sqrt{\frac{1+k}{1-k}} \tag{2}$$

where Z_0^{SCPS} is the characteristic impedance of the SCPS, and k is the coupling coefficient. The four quarter-wavelength coupled lines must satisfy the following condition

$$Z_0^{\text{SCPS}} = \sqrt{2}Z_0 \tag{3}$$

where Z_0 is the single-ended port termination impedance, and the value of the resistors required to obtain output isolation is given by

$$R = 2Z_0 \tag{4}$$

The radius of the ring divider core is given by

$$R_{\text{SCPS}} = \frac{\lambda_g}{2\pi} \tag{5}$$

where λ_g is the guided wavelength of the center design frequency.

Figure 2 shows the simulated even and odd-mode characteristic impedances and coupling coefficient as a function of the SCPS conductor width (W_{scps}) and spacing (S_{scps}). For a $50\,\Omega$ design, the required characteristic impedance of the SCPS lines is $70.7\,\Omega$ and odd-mode impedance is approximately $35.3\,\Omega$ [5]. The CPW trace width
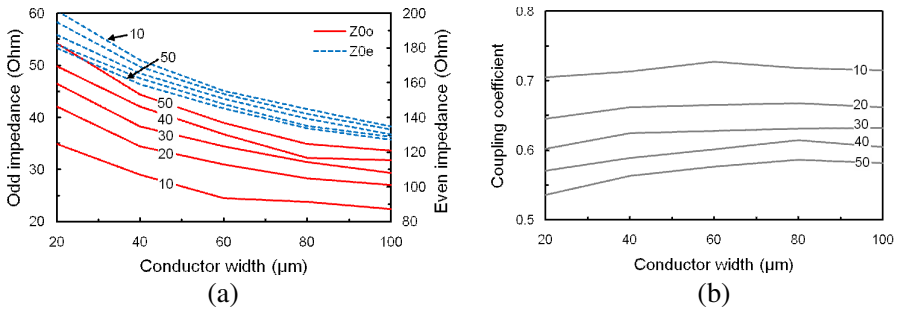
Figure 2. Simulated (a) even and odd-mode characteristic impedance, and (b) coupling coefficient versus the SCPS conductor width (W_{scps}) for different values of conductor spacing (S_{scps}).

was chosen to be 60 μm for a compatibility with on-wafer measurement probes. Using this same value for the SCPS width, the required spacing of the SCPS transmission lines was synthesized to be 24 μm according to Figure 2. The corresponding even-mode impedance and the coupling factor are 151 Ω and 0.65, respectively. The simulations of the ring divider were performed using the Ansoft HFSS$^{\text{TM}}$ electromagnetic (EM) modeling tool. Physical dimensions of the final optimized design are given in Table 1.

2.2. Cross-over Phase Inverter

The phase inverter design is based on a SCPS airbridge cross-over. The dimension of the airbridge cross-over is 50 μm × 200 μm that was optimized for low loss and good matching using the HFSS simulation

Table 1. Dimensions (in microns) for the optimized ring divider.

| Parameters	Description	Value
W_{SCPS}	Conductor width of SCPS	60
S_{SCPS}	Gap between SCPS conductors	24
R_{SCPS}	Radius of the ring	672
W_{CPW}	Center conductor width of CPW	60
S_{CPW}	Gap between center and ground conductors of CPW	40
G_{CPW}	Ground conductor width of CPW	60
W_{AB}	Width of the airbridges	50
L_{AB}	Length of airbridges	200
H_{AB}	Height of airbridges	4
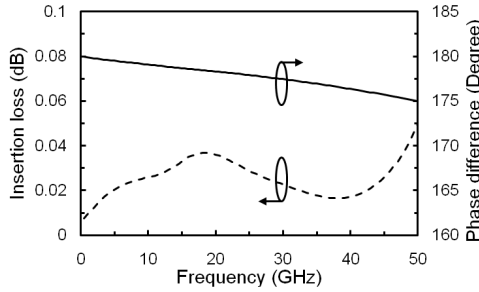
Figure 3. Simulated extra loss and phase difference for an SCPS airbridge cross-over compared with a uniform SCPS of the same physical length.

tool. The simulation results shown in Figure 3 indicate that the SCPS cross-over has less than 0.05 dB extra loss and 180° phase shift with approximately 5.5° phase difference up to 50 GHz when compared with a uniform SCPS of same physical length. This performance is better suited for millimeter-wave frequency operation in comparison to the via-based phase inverter implementation reported in [2] because the elevated airbridge cross-over has lower parasitic inductance.

2.3. Effect of Resistor Tolerance

The output isolation response and output port matching of the ring divider are sensitive to the tolerance of the on-chip resistors. To investigate this, a parametric analysis was performed using Ansoft HFSS to vary the resistivity value of the isolation resistors. The simulated variation in the output isolation response and output reflection coefficient is shown in Figure 4. The response for S_{22} and S_{33} are similar to each other. It can be clearly seen from Figure 4(a) that the port isolation improves as the unit resistor values increase but begin to degrade at higher frequencies as the unit resistor values increase above 60 Ω/□. This indicates that a typical tolerance of ±10 Ω/□ from the theoretical optimum resistor value, calculated using Equation (4), can provide a good isolation performance across a wide bandwidth. However, Figure 4(b) indicates that higher unit resistor values improve output port matching.
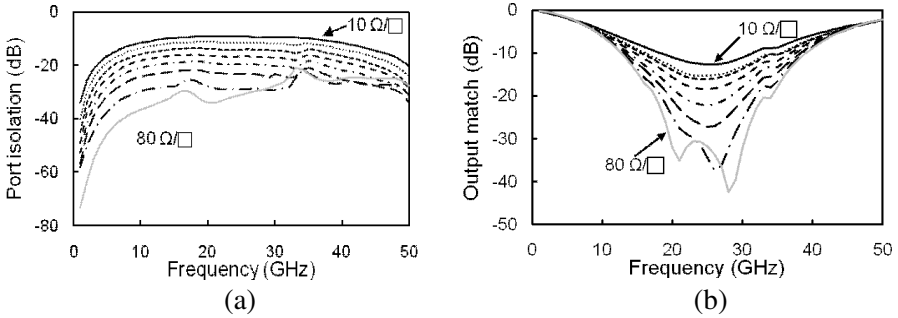
Figure 4. Simulated (a) variation of output port isolation $|S_{32}|$, and (b) output port match $|S_{22}|$ for different unit resistor values (in 10 Ω/□ steps).

3. EXPERIMENTAL RESULTS

To validate the proposed concept, a ring divider design operating at K-band was fabricated on a semi-insulating GaAs substrate of
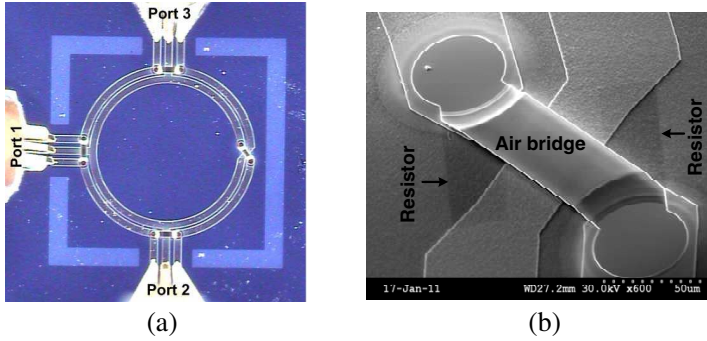
Figure 5. (a) Microphotograph of the fabricated ring divider under test, and (b) SEM image of the airbridge cross-over section.

620 µm thickness. The metal conductor patterns in gold were defined using electron beam lithography techniques with an evaporated gold thickness of 0.5 µm. The isolation resistors were formed using nichrome. The airbridges connecting the CPW ground conductors and forming the SCPS cross-overs were also defined by electron-beam lithography and fabricated using a dry etch process. A microphotograph of a divider under test and a scanning electron microscope (SEM) image of the airbridge cross-over are shown in Figure 5. The chip size, including the probe pad feeds, is 1.9 mm × 1.9 mm.

Scattering parameter measurements were performed using the Short-Open-Load-Reciprocal Thru (SOLR) method of calibration [8] with a commercial alumina impedance standard substrate (P/N CS-15). Since the ports of the divider are orthogonal to each other, three separate calibrations were carried out on a standard probe station with two probes while a third probe was used as the broadband load. The scattering parameters of the ring divider were reconstructed based on the three sets of two-port scattering parameter measurements. By choosing the SOLR calibration technique we avoid the need to fabricate replica devices that have the added constraint of only having in-line port layouts. This not only saves on costly chip area, but the resultant scattering parameters are measured from a single device to give a true indication of its output balance performance.

Figure 6 shows the measured results that are in good agreement with the simulations. It can be seen that port isolation better than 20 dB is achieved across the bandwidth from 10 MHz to 50 GHz as predicted. The in-band insertion loss and port return losses are 0.6 dB and 15 dB over the frequency range from 15 GHz to 32 GHz,
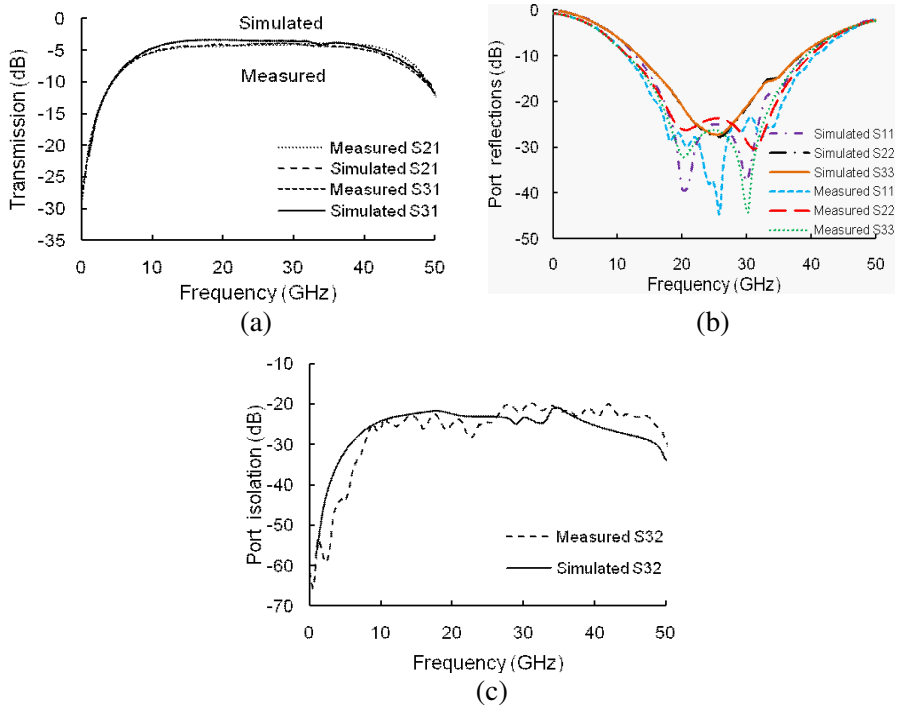
Figure 6. Frequency response of the ring divider: magnitude of (a) transmission, (b) port return losses, and (c) output port isolation.
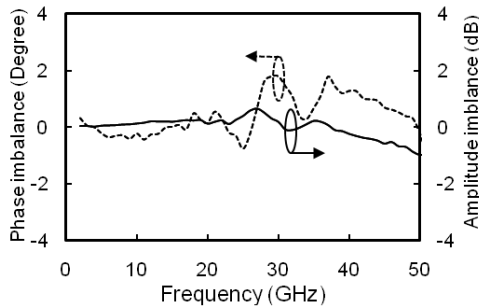
Figure 7. Measured amplitude $|S_{31}/S_{21}|$ and phase (S_{31}/S_{21}) balance response.

respectively. Slight discrepancies in the output port matching are seen in Figure 6(b). This difference may come from either the fabrication tolerance of the isolation resistors, as discussed in Section 2.3, or a

slight error in positioning the probes during measurement.

The measured amplitude and phase balance of the ring divider is shown in Figure 7. These indicate that the output amplitude and phase balance are within ± 0.5 dB and $\pm 2°$, respectively, in the bandwidth from 10 MHz to 43 GHz.

Table 2 summarizes the performance of our proposed divider compared to recently published work by other authors. It can be seen that the proposed divider demonstrate the combined advantages of a compact size, wideband high isolation, and uniplanar fabrication characteristics. Devices with comparatively smaller size demonstrate

Table 2. Comparison of performance characteristics of power dividers with broadband isolation implemented using different technologies and techniques.

Reference	Centre Frequency (f_0)	Bandwidth ($\Delta f/f_o$)		
		Reflection > 15 dB	Transmission < 4 dB	Isolation > 20 dB
[2]	2 GHz	75%	120%	234%
[3]	0.75 GHz	69%/79%	105%/123%	168% /240%
[9]	30 GHz	< 100%	†	107%
[10]	15 GHz	12%	< 10%	‡
[11]	~ 10 GHz	~ 110%	140%	150%
This work	25 GHz	68%	76%	> 200%
Reference	Size	Technology	Fabrication	-
[2]	$0.52\lambda_g$ $\times 0.73\lambda_g$	Parallel-Strip lines	Double-sided	-
[3]	$0.46\lambda_g$ $\times 0.64\lambda_g$	ACPS Slotlines	Uniplanar	-
[9]	$0.13\lambda_g$ $\times 0.29\lambda_g$	Microstrip & CPW	Multilayer	-
[10]	$> 3\lambda_g$ $\times 1.3\lambda_g$	SIW	Vias required	-
[11]	$\sim 0.42\lambda_g$ $\times 0.14\lambda_g$	Multiple wafer -level packaging	Multilayer	-
This work	$0.45\lambda_g$ $\times 0.45\lambda_g$	CPW & SCPS	Uniplanar	-

†Transmission loss is greater than 5 dB;
‡Isolation is less than 15 dB.

lower isolation bandwidth and require more complicated multilayer fabrication processes [9, 11].

4. CONCLUSIONS

A new design of the ring power divider has been successfully demonstrated using a GaAs MMIC process with airbridge technology. The proposed design uses entirely coplanar techniques that make the divider compact in size and suitable for integration with active GaAs MMIC devices.

ACKNOWLEDGMENT

REFERENCES

1. Wong, S. W. and L. Zhu, "Ultra-wideband power divider with good in-band splitting and isolation performances," *IEEE Microw. Wireless Components Lett.*, Vol. 18, No. 8, 518–520, Aug. 2008.

2. Chiu, L. and Q. Xue, "A parallel-strip ring power divider with high isolation and arbitrary power-dividing ratio," *IEEE Trans. Microw. Theory Tech.*, Vol. 55, No. 11, 2419–2426, Nov. 2007.

3. Wong, K. W., L. Chiu, and Q. Xue, "Uniplanar power dividers using asymmetric coplanar striplines and slotlines," *Proc. 38th European Microw. Conf.*, 337–340, Amsterdam, The Netherlands, Oct. 2008.

4. Yang, N., C. Caloz, and K. Wu, "Wideband phase-reversal antenna using a novel bandwidth enhancement technique," *IEEE Trans. Antennas Propagation*, Vol. 58, No. 9, 2823–2830, Sep. 2010.

5. Chang, C.-Y., C.-W. Tang, and D.-C. Niu, "Ultra-broadband doubly balanced star mixers using planar Mouw's hybrid junction," *IEEE Trans. Microw. Theory Tech.*, Vol. 49, No. 6, 1077–1085, Jun. 2001.

6. Hirota, T., Y. Tarusawa, and H. Ogawa, "Uniplanar MMIC hybrids — A proposed new MMIC structure," *IEEE Trans. Microw. Theory Tech.*, Vol. 56, No. 6, 576–581, Jun. 1987.

7. Simons, R. N., *Coplanar Waveguide Circuits, Components and Systems*, John Wiley & Sons, Inc., Vol. 6, 163–165, 1997.

8. Basu, S. and L. Hayden, "An SOLR calibration for accurate measurement of orthogonal on-wafer DUTs," *IEEE MTT-S Digest*, 1335–1338, Denver, CO, USA, Jun. 1997.

9. Sun, Y. and A. P. Freundorfer, "Broadband folded Wilkinson power combiner/splitter," *IEEE Microw. Wireless Components Lett.*, Vol. 14, No. 6, 295–297, Jun. 2004.

10. Kim, K., J. Byun, and H.-Y. Lee, "Substrate integraged waveguide Wilkinson power divider with improved isolation performance," *Progress In Electromagnetics Research Letters*, Vol. 19, 41–48, 2010.

11. Lan, X., P. Chang-Chien, F. Fong, D. Eaves, X. Zeng, and M. Kintis, "Ultra-wideband power divider using multi-wafer packaging technology," *IEEE Microw. Wireless Components Lett.*, Vol. 21, No. 1, 46–48, Jan. 2011.