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IMPROVING SILICON INTEGRATED ANTENNAS BY SUBSTRATE MICROMACHINING: A STUDY OF ETCHING PATTERNS

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Abstract—One of the main drawbacks of antenna integration on standard CMOS silicon substrates are the low radiation efficiency levels obtained due to the high silicon losses. This paper studies the use of micromachining techniques to remove silicon beneath the antenna as a solution to improve radiation efficiency. Several etching patterns are analyzed for different etching depths through simulations and measurements in order to find out which are the best ones for the micromachining process. Results are verified in two operating scenarios.

1. INTRODUCTION

In recent years there has been an important evolution in wireless communication systems with new applications that require small and cheap devices. The integration of all the system (including the antenna) in a single chip is an interesting option to achieve these requirements.

In literature we can find different examples of silicon integrated antennas for intra chip and inter chip communications [1]. [2, 3] and [4] show integrated antennas operating at frequencies higher than

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60 GHz, [5] and [6, 7] study the performance of integrated antennas near the 24 GHz ISM band, and [8] presents a fully integrated transmitter with an on-chip dipole antenna at the same frequency.

The aforementioned examples operate at frequencies higher than 10 GHz, however in some applications like in implantable devices [9–11], lower frequencies are desirable to reduce propagation losses. At lower frequencies the radiating elements are larger, and hence, more difficult to integrate, therefore, miniaturization techniques must be applied [12]. Some examples of integrated antennas working at frequencies lower than 10 GHz can be found in [12–14] where the 5.8 GHz ISM band is typically used.

In order to reduce fabrication and packaging costs and obtain real system on-chip devices, it is desirable to make the antenna fabrication process compatible with the standard CMOS technologies. The fabrication of the antenna and the electronic circuits in the same chip reduces the assembly costs and eliminates the need for external transmission line connections [13]. One of the main drawbacks of the high losses silicon substrates typically used in standard CMOS technologies is that the antenna radiation efficiency decreases drastically. Furthermore this efficiency degradation is emphasized when miniaturization techniques are applied to reduce antenna dimensions [12].

Different solutions to improve the radiation efficiency have been reported. For instance, in [15] the thickness of the insulation layer between the silicon and the antenna is increased to reduce losses, and in [6] the silicon substrate thickness is reduced to improve the on-chip antenna efficiency. Another solution is the use of micromachining techniques to eliminate silicon of the back side of the antenna, like in [14] where a micromachining process is used to improve the efficiency of a dipole antenna in the 5.8 GHz band.

In previously reported designs [14, 16], a single rectangular shaped mask has been used for the selective silicon etching process. In this paper, we will carry out a comparative study of several etching patterns in order to maximize the gain improvement without a significant increase in the antenna fragility. Simulations and measurements of the fabricated prototypes will be shown.

The antenna performance will be also analyzed in different operating scenarios to prove that similar gain improvement can be expected in real applications, like in sensor networks or body implanted monitoring systems.

2. ANTENNA DESIGN AND FABRICATION

The radiating element is a meandered dipole designed to work at frequencies near 5 GHz (Figure 1(a)). This antenna can be easily connected to differential ended active circuits without the need for a balun. Chip dimensions are 1.9 mm × 5.25 mm, therefore meandered lines are used to reduce the dipole dimensions according to the available area [12, 17–20].

As mentioned in the introduction, one solution to improve the low radiation efficiency of silicon integrated antennas is the use of micromachining techniques to selectively etch the silicon at the back side of the antenna substrate. The best option would be to remove all the silicon under the antenna, however the etching of large areas is problematic because the resulting membrane structure is fragile and can be easily broken. Etching an array of smaller areas, similar gain improvement can be obtained without compromising the mechanical robustness of the structure.

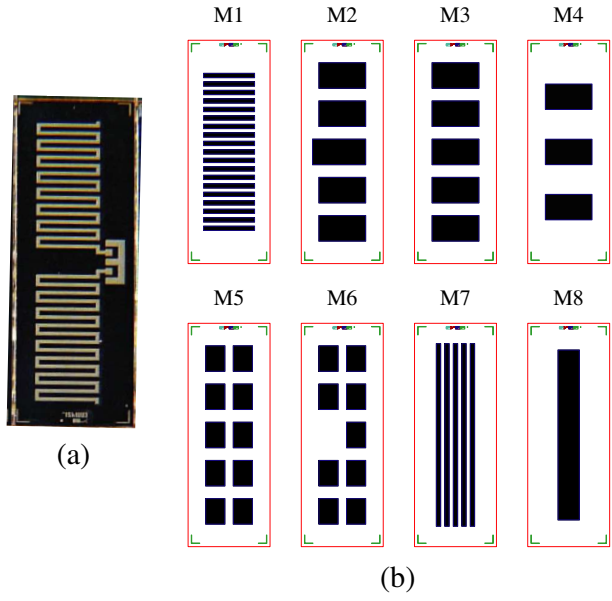


Figure 1. Design of the fabricated prototype antennas. (a) Image of the fabricated meandered dipole antenna. (b) Schematic representation of the different patterns used for the micromachining process. Black rectangles indicate the areas where the silicon is etched.

For this reason in this paper we present several etching configurations where cavities with different sizes, shapes and distributions are micromachined in order to study which patterns give the best improvement in gain. The different configurations under study are shown in Figure 1(b). All the etching patterns avoid the elimination of a large, continuous silicon area, keeping silicon walls to guarantee the robustness of the structure.

Antennas fabrication started with p-type silicon wafers having 20 Ohm·cm resistivity and 500 µm thickness. A 2 µm-thick layer of SiO_2 was grown with a wet oxidation process and a 4 µm-thick SiO_2 was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). The resulting thickness of SiO_2 (6 µm) is similar to the effective thickness of the dielectric stack that some CMOS processes have under the top metal level, therefore the results of the present study can be used in the design of integrated antennas fabricated with standard CMOS technologies.

Next, a 2-µm thick aluminum (Al) was deposited by sputtering. The Al layer was patterned by standard photolithography and wet etch. On the back side of the wafers, a 1-µm thick Al layer was deposited and patterned in the same way as above. Subsequently, a dry etching process was used to remove the SiO_2 from the back side and a Deep-Reactive Ion Etching (DRIE) process was used to partially remove the silicon beneath the antenna structures. The fabrication was finished by removing the back side Al with a wet etching process. More information about the different fabrication processes can be found in [21].

3. MEASUREMENTS AND SIMULATION RESULTS

Antenna measurements were carried out using a Picoprobe GSGSG differential probe [22] in a M150 Cascade Microtech probe station [23]. A 1 cm PolyVinyl Chloride (PVC) support was used to separate the antenna from the probe station metallic chuck. The PVC support was mechanized to transmit the vacuum to the antenna and avoid unwanted movements during the measurement process. A photograph of the measurement setup is shown in Figure 2. Simulations that emulate the measurement setup were carried out with FEKO [24] simulation software. A dielectric PVC block was located under the antenna to represent the PVC support, and a Perfect Electric Conductor (PEC) surface was used to model the effects of the probe station metallic chuck.

Vector Network Analyzers (VNA) have single ended ports, therefore, a balun is required for S_{11} parameter measurements using

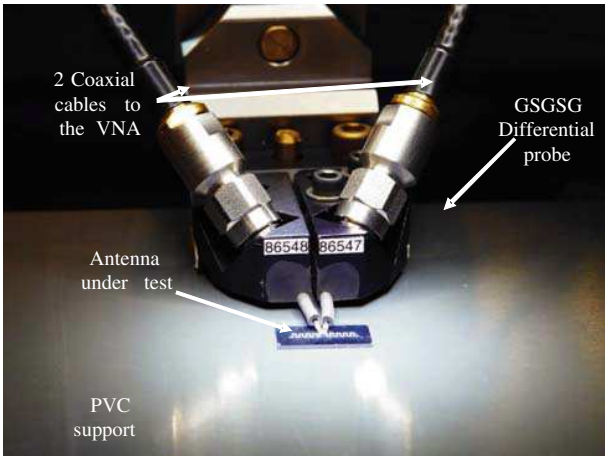


Figure 2. Antenna measurement setup. Measurements are carried out inside the probe station. A PVC support is used to separate the antenna from the probe station metallic chuck.

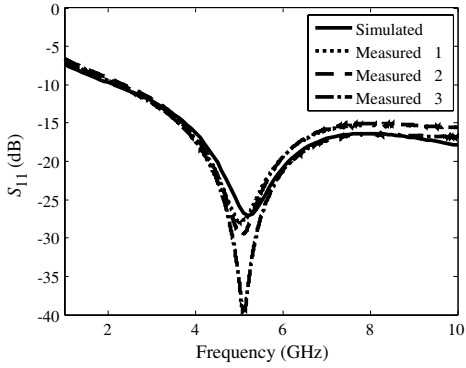


Figure 3. Input reflection coefficient of the proposed dipole fabricated on a silicon substrate without micromachining. Solid line shows the simulated results. Dashed lines show the measured results of three identical antennas fabricated on different wafers. A 100 Ω impedance is used as differential reference impedance.

1 port. However, baluns are usually limited in bandwidth thus preventing broadband measurements. In our case, the use of a balun was avoided using a 2 single ended ports measurement and the mixed mode S parameters [25].

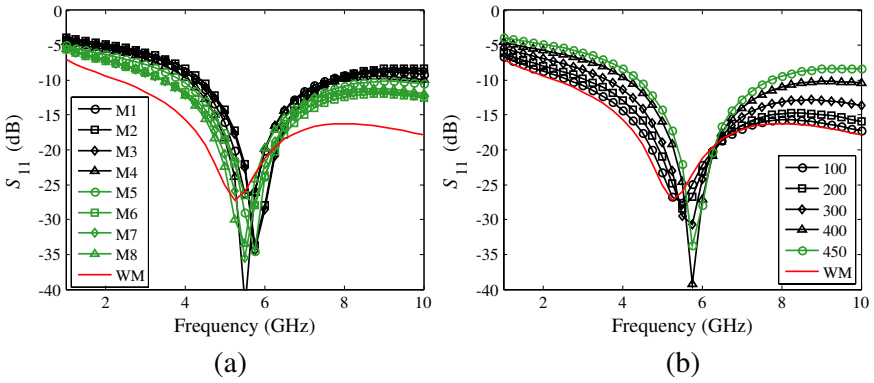


Figure 4. Simulated input reflection coefficient. (a) Different micromachining configurations are applied. The etching depth is 450 µm. (b) Different etching depths (µm) are applied. The M2 pattern is used for the micromachining process. The wafers thickness is 500 µm. WM = Without Micromachining.

Figure 3 shows the differential input reflection coefficient of a meandered dipole antenna without micromachining when a reference impedance of 100 Ω is used. The simulated results are plotted with solid line and the measured results with dashed lines. It can be seen as there is a good agreement between simulations and measurements. Furthermore, three identical antennas from different wafers were measured, proving the good repeatability of the fabrication process and measurements. The measured antennas have an optimal matching point near 5 GHz and broadband matching is observed. This is mainly due to the high losses of the silicon substrate. These results prove that in these structures the main problem are not the matching levels but the efficiency levels.

In Figure 4(a) the input reflection coefficient of the antenna with different etching patterns is plotted. A slight frequency shift to higher frequencies can be seen due to the fact that the elimination of silicon reduces the effective relative permittivity of the substrate. When micromachining is applied impedance curves also become sharper due to the lower losses levels, reducing the matching bandwidth of the antenna. The effects of the different micromachining configurations on the input parameters are similar. Figure 4(b) shows the input reflection coefficient as a function of the etching depth for a specific etching pattern (M2). It can be seen as the above mentioned effects become more important when the etching depth is increased.

Figure 5(a) shows the simulated radiation efficiency as a function

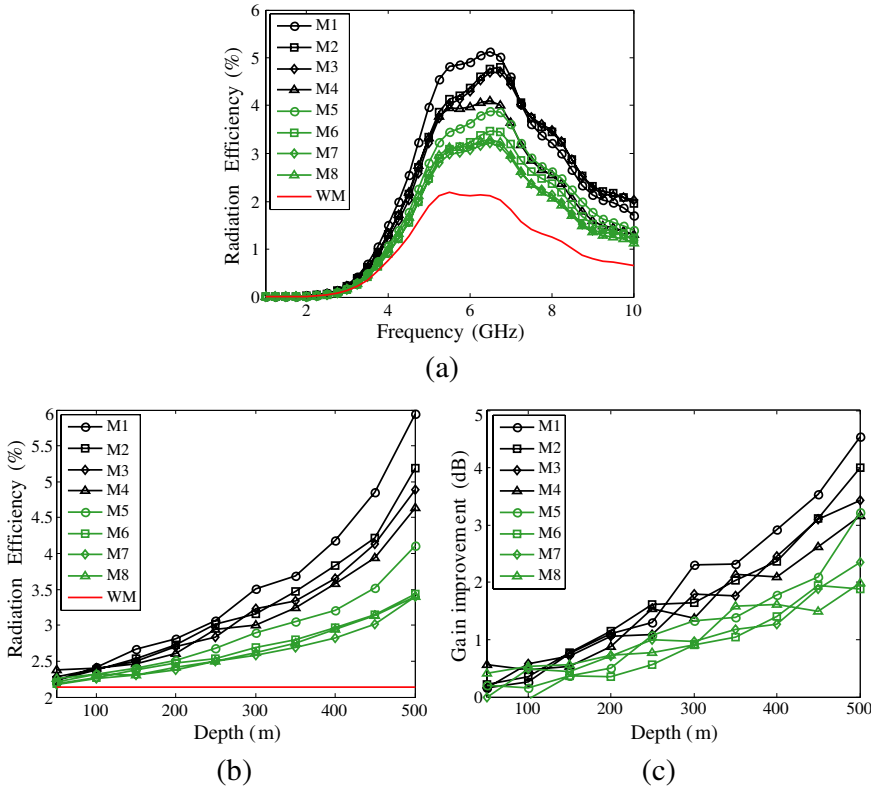


Figure 5. Simulated radiation parameters when micromachining techniques are applied. (a) Radiation efficiency as a function of frequency. The etching depth is 450 µm. (b) and (c) Radiation efficiency and gain improvement as a function of the etching depth. The operating frequency is 5.8 GHz and the wafers thickness is 500 µm. The reference gain for the gain improvement plot is the gain of the antenna without micromachining (−19 dBi). WM = Without Micromachining.

of frequency for the different etching patterns. It is important to point out that our band of interest (5.8 GHz) is near the efficiency maximum. In this plot the effects of micromachining can be clearly seen because an improvement of the efficiency is observed for all the configurations. Depending on the geometry used in the micromachining, this improvement can be higher than a factor of 2.

Figure 5(b) shows the efficiency at 5.8 GHz for the different etching configurations as a function of the etching depth. The wafers

thickness is 500 μm for all cases. The efficiency improves when the depth is increased, and again, this improvement also depends on the geometry of the etched areas. Similar conclusions can be obtained from Figure 5(c). Gain improvement up to 4 dB can be achieved in the normal direction with the best etching configuration (M1). For the same etching depth (i.e., 450 μm), the gain improvement can range from 1.5 dB to 4 dB depending on the etching pattern used in the micromachining process. Simulated normalized radiation patterns (not shown) do not significantly change when micromachining is applied.

To verify the previous simulations, gain improvement measurements of the fabricated prototypes were carried out using the setup shown in Figure 6. Measurements were performed in the probe station, trying to maximize the clearance area near the antenna and with a clear line of sight between the transmitting and the receiving antennas. A 5.8 GHz balun was used to convert the single ended signal generated by the signal generator into the differential signal necessary to feed the dipole antennas. As receiving antenna, a microstrip patch fabricated on Rogers RO-4003C substrate was used. An antenna with no micromachining was used as transmitting reference antenna.

The measured and simulated gain improvements are summarized in Table 1. Although measured gains are slightly higher than simulator predictions there is a good agreement in the trends. With an etching depth of 450 μm measured gain improvements near 4 dB are obtained. The use of higher etching depths would improve the gain even more,

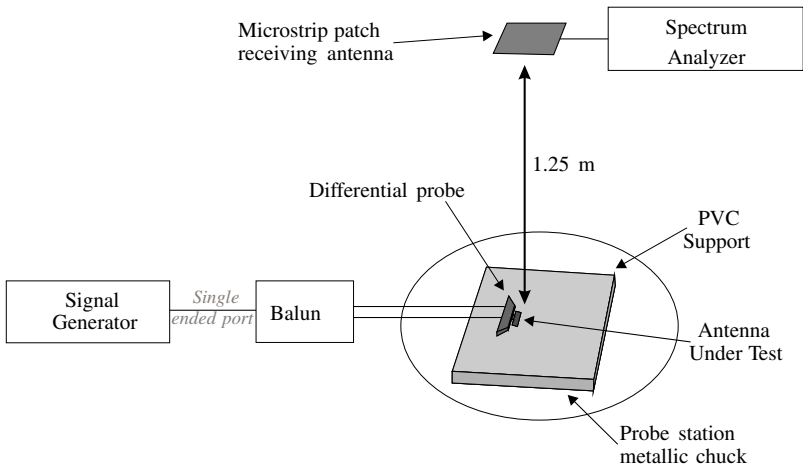


Figure 6. Propagation measurements setup used for the gain measurement of the fabricated prototypes.

Table 1. Measured and simulated gain improvement for the different etching patterns. The last column shows the etched area. The etching depth is 450 µm and the wafers thickness is 500 µm.

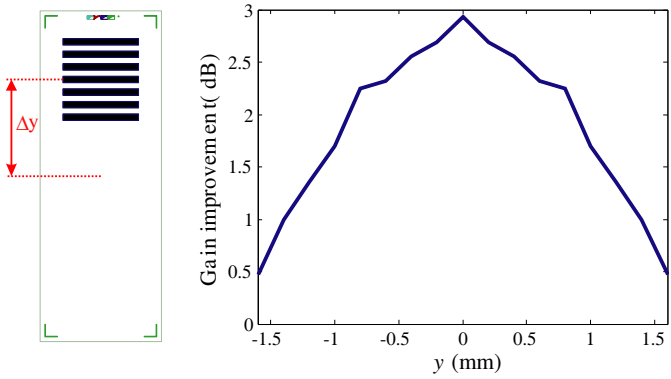
Etching pattern	Simulated Gain Improvement	Measured Gain Improvement	Etched Area (mm^2)
M1	3.5	3.9	2.3
M2	3.1	3.6	3.4
M3	3.1	3.3	3.3
M4	2.6	2.8	2.0
M5	2.1	2.6	2.7
M6	1.9	2.4	2.4
M7	1.9	2.0	2.2
M8	1.5	1.8	2.0

but the resulting structures would be more fragile. With 50 µm of silicon in the cavities, the resulting structures are strong enough to withstand the measurements in the probe station without the need to fill the cavities with another dielectric material. We tried to completely remove the silicon from the patterns but in some of the prototypes the remaining dielectric membrane supporting the antenna broke, probably due to mechanical internal stress in the oxide layers.

Intuitively, it could be thought that the best etching pattern is the one that eliminates more silicon area under the antenna. However, this is partially true because the geometry used for the etching process is also important. According to Table 1, the geometry with higher gain improvement is not the one that eliminates more silicon. The amount of silicon etched in M2 is a 50 % higher than in M1 but the measured gain improvement in M1 is 0.3 dB better than in M2. In a similar way, the amount of silicon etched in M4 and M8 is nearly the same, but M4 gain improvement is 1 dB better than M8.

Based on these results, some general guidelines for the use of micromachining techniques can be given in order to maximize the gain improvement of silicon integrated dipole antennas. First of all, structures with horizontal (normal to the dipole orientation) trenches have better performance than structures with vertical ones. This is a reasonable result because horizontal trenches limit the current circulation in the substrate.

In the second place, it is better to eliminate silicon near the feeding area, where currents and fields are stronger, than in the areas far away from the feeding point. This can be verified in Figure 7, where only a small part of the silicon chip around the position Δy is etched. When



(a) (b)

Figure 7. Simulated gain improvement as a function of the position of the etched area. (a) Pattern used in the micromachining process. (b) Gain improvement. The reference gain is the gain of the antenna without micromachining (−19 dBi).

the etched area is under the feeding, the gain is up to 2 dB better than when it is under the ends of the antenna.

4. MICROMACHINED ANTENNAS IN A FREE SPACE SCENARIO

In the previous section the micromachining effects have been analyzed through simulations and measurements carried out inside the probe station. One could think that the obtained results only apply in that particular case. In this section, simulations are used to assess the antenna performance in free space.

Figure 8(a) shows the S_{11} parameter in a free space scenario. Comparing it with the previous results, the main difference is a slight frequency shift to higher frequencies. This is related to the fact that, in the probe station scenario, the antenna is on a supporting material with a relative permittivity higher than one, which tends to reduce the resonant frequency of the structure.

Figure 8(b) shows the gain improvement at 5.8 GHz with respect to an antenna without micromachining. The improvement is similar to the values obtained in the probe station scenario. Comparing Figure 5 and Figure 8, it can be seen as, if the different etching patterns are sorted according to their gain improvement, the same results are obtained in both scenarios. Therefore, it is expected that

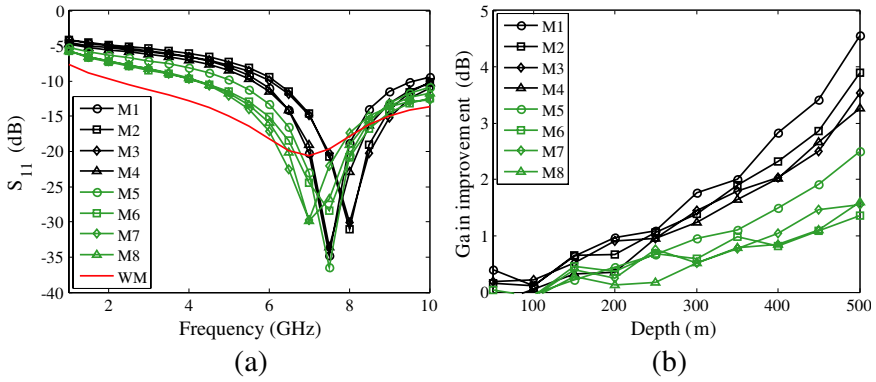


Figure 8. Performance improvement due to micromachining in a free space scenario. (a) Simulated input reflection coefficient. The etching depth is 450 µm. (b) Gain improvement as a function of the etching depth. The operating frequency is 5.8 GHz and the wafers thickness is 500 µm. WM = Without Micromachining.

these improvements will also be valid in the real operating scenario of the antenna which will depend on the final application.

5. CONCLUSIONS

In this paper we have analyzed the performance of integrated antennas with substrate micromachining. A standard CMOS technology has been used in order to reduce fabrication and packaging costs. Several etching geometries have been studied, showing that the pattern used for the etching process is important.

It has been shown that the micromachining effects are more important in the radiation parameters than in the input parameters. Antenna gain improvements near 4 dB have been measured for an etching depth of 450 µm. The higher is the etching depth, the better is the efficiency improvement. However, when completely etching away the silicon in the patterns, the structure becomes fragile and can break.

These gain improvements are relevant. If these antennas were used in a wireless sensor network, the power required for the communication between nodes (keeping the same system performance) could be reduced more than a fifty percent thus increasing the batteries lifetime.

With reference to the pattern used in the micromachining process, it has been shown that not only the total amount of etched silicon is important, the geometry used for the etching process is also significant.

It is advisable to eliminate silicon near the feeding area and use horizontal trenches that limit the current circulation in the substrate.

Finally, it is important to point out that all the measurements were carried out inside a probe station, however the validity of these results in a free space operating scenario has also been proved through numerical simulations. Therefore, it is expected that the observed trends will be the same in the real operating scenario.

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