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DEVICE SIMULATION OF EFFECTS OF MICROWAVE ELECTROMAGNETIC INTERFERENCE ON CMOS RS FLIP-FLOPS

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Abstract—The study on effects of microwave electromagnetic interference on CMOS RS flip-flops is reported in this paper. Using device simulation method, the relation between the susceptibility of CMOS RS flip-flops and microwave electromagnetic interference frequency as well as pulse width has been analyzed. It is found that the effects of microwave electromagnetic interference get suppressed gradually with increasing frequency. Furthermore, the interference power threshold is inversely proportional to the pulse width, and the interference energy threshold is directly proportional to the pulse width conversely. In addition, because of the difference in the structure of these two categories of CMOS RS flip-flops, they have different susceptibility to microwave electromagnetic interference.

1. INTRODUCTION

In recent years, growing attention has been paid to the threat posed by microwave electromagnetic interference, which can couple into electronic devices intentionally from microwave sources or unintentionally due to the proximity to general environmental RF signals [1–3]. The effects of these microwave interferences on electronic devices might result in permanent physical damage [1]. Although, EM shielding can mitigate the effects of direct irradiation on the devices, the microwave electromagnetic fields can still cause system upsets through unprotected inputs and outputs of the system, imperfections or apertures of EM shields, pins of the packaged chips, connecting

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wires, power cables, printed circuit board (PCB) traces and bonding interconnects. In addition, the actual antennas in wireless and mobile devices intended to communicate with the external environment could not easily be shielded against microwave radiation without losing or severely degrading their function [1]. These can incur the EMI signal coupling and conducting into individual circuit units inside the system leading to system upsets.

Such a system-level upset can be understood by investigating and identifying the effects of EMI on the operational parameters of the fundamental devices in CMOS ICs [4]. Nowadays, most researches are primarily focused on CMOS inverters [4–6], CMOS AND devices and CMOS NAND devices [7]. However, flip-flops, which are fundamental building blocks in electronic systems, are seldom investigated the effects under microwave electromagnetic interference. Wallace et al. [8] reported the radiated susceptibility of D-type flip-flops implemented in various CMOS and TTL logic technologies. The study reveals that these devices are susceptible only during certain time intervals during an operational cycle. The particular interval during which a flip-flop is susceptible is dependent on the logic state of the data input line, the implementation technology of the flip-flop and the amplitude of the disturbing signal. The results of the upset of a ripple counter constructed from D-type flip-flops, by transient pulses are presented by Kashyap et al. [9]. The results show that coupling of a transient pulse to one of the traces that connects the Q output of one stage to the clock input of the next stage of the counter can cause upset of the counter. If the clock input is low, the D-input is high and the transient pulse has positive polarity, then upset occurs. Although these studies provide useful information, there are distinguishable differences between microwave electromagnetic interference (e.g., high power microwave) and general microwave interference as well as electro-static discharge (ESD). Effects of microwave electromagnetic interference on CMOS RS flip-flops need to be studied. Beside the characterization of electronic devices susceptibility, modeling of these effects has been investigated. Chahine et al. [10–12] developed a robust mathematical method to predict the susceptibility of a CMOS inverter to conducted disturbance by applying the direct power injection (DPI) method. This model is based on artificial neural networks and is validated up to 1 GHz. In addition, a complete simulation model of a direct power injection (DPI) setup, used to measure the immunity of integrated circuits to conducted continuous-wave interference is reported based on equivalent circuit method [13]. Generally, electronic devices studied in these works are treated as black box which means the effects of microwave electromagnetic interference are speculated according to the

input and relevant output characteristics. From the macroscopic point of view, black box method is useful and suitable for these studies. On the other hand, the method used in this paper might be complementary to those of previous works from the perspective of microscopic view.

In this paper, device simulation studies on the effects of CMOS RS flip-flops under microwave electromagnetic interference are presented. The MOS devices in CMOS RS flip-flops are modeled by solving a set of semiconductor equations according to Drift-Diffusion Theory in order to study the effects on the electronic devices under microwave electromagnetic interference in the essence of carrier distribution and conduction.

2. SIMULATION MODEL

There are two categories of CMOS RS flip-flops in the simulation, CMOS RS flip-flop composed of two cross-coupled NOR gates and two cross-coupled NAND gates. Their schematics are shown in Figures 1(a) and (b), respectively. To facilitate the description, these two categories of CMOS RS flip-flops are denoted as "flip-flop 1" and "flip-flop 2". T_1, T_2, T_3, T_4 in Figure 1 are PMOS devices made of silicon and T_5, T_6, T_7, T_8 are NMOS devices made of silicon. V_{DD} is power supply voltage, which is equal to 5 V in the simulation. "S" and "R" stand for set and reset pin, respectively. "Q" and "$\overline{Q}$" represent outputs of CMOS RS flip-flops.

All silicon NMOS devices in the simulation are identical as well as PMOS devices. The geometrical and process parameters of NMOS devices and PMOS devices are shown in the Table 1.

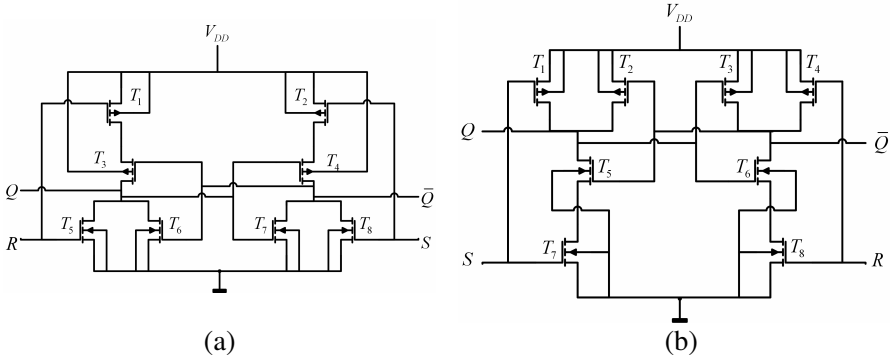

Figure 1. Schematic of CMOS RS flip-flops. (a) Flip-flop composed of two cross-coupled NOR gates (flip-flop 1). (b) Flip-flop composed of two cross-coupled NAND gates (flip-flop 2).

Table 1. Various parameters of MOS devices used in the simulation.

	NMOS	PMOS
Channel length/μm	2	2
Channel width/μm	1.5	3
Channel doping/m^{-3}	2×10^{22}	2×10^{22}
Source and Drain doping/m^{-3}	2×10^{26}	2×10^{26}
Oxide thickness/nm	25	25

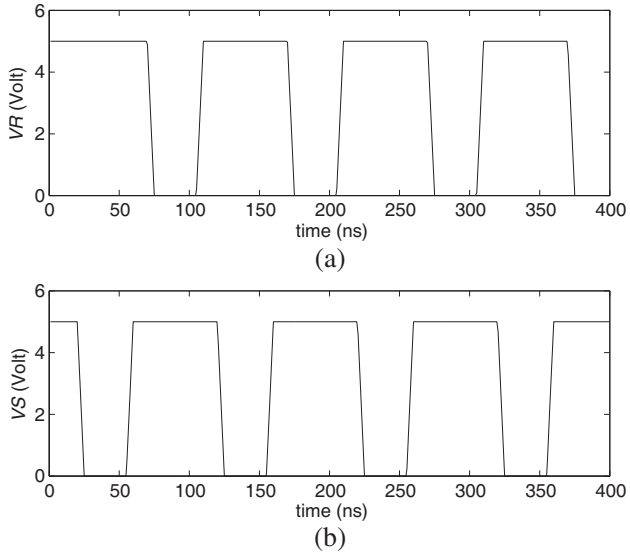

Figure 2. Input waveforms. (a) Reset pin, (b) set pin.

In the simulation, microwave electromagnetic interference is injected from reset pin and normal operation signal inputs from set pin. Effects of microwave electromagnetic interference on CMOS RS flip-flops are studied by varying parameters of microwave electromagnetic interference pulse. Furthermore, to avoid the occurrence of the race condition to affect the investigation of effects of microwave electromagnetic interference, the forbidden state (i.e., R and S inputs are high simultaneously for flip-flops 1 while R and S inputs are both low for flip-flops 2) is not allowed in the simulation.

Our home-developed simulator SDS [14] used in this paper consists of two parts, circuit simulator and semiconductor device simulator which combine with each other using coupling algorithm.

Meanwhile, the simulator also takes the thermal radiation, air cooling and behaviors of semiconductor under high temperature as well as intense field in consideration.

3. VERIFICATION OF SDS

The validity of SDS is verified using commercial software MEDICI [15] before investigating the effects on CMOS RS flip-flops. Flip-flop 2 (as shown in Figure 1(b)) is modeled and simulated identically in MEDICI and the simulator, where the structures of MOS devices are presented in Table 1. Input waveforms of set and reset pin are given in Figure 2. Figure 3 illustrates that these simulated results match quite well with each other, which demonstrate the qualification of the simulator. Thus, we utilize this simulator to research effects of microwave electromagnetic interference on CMOS RS flip-flops.

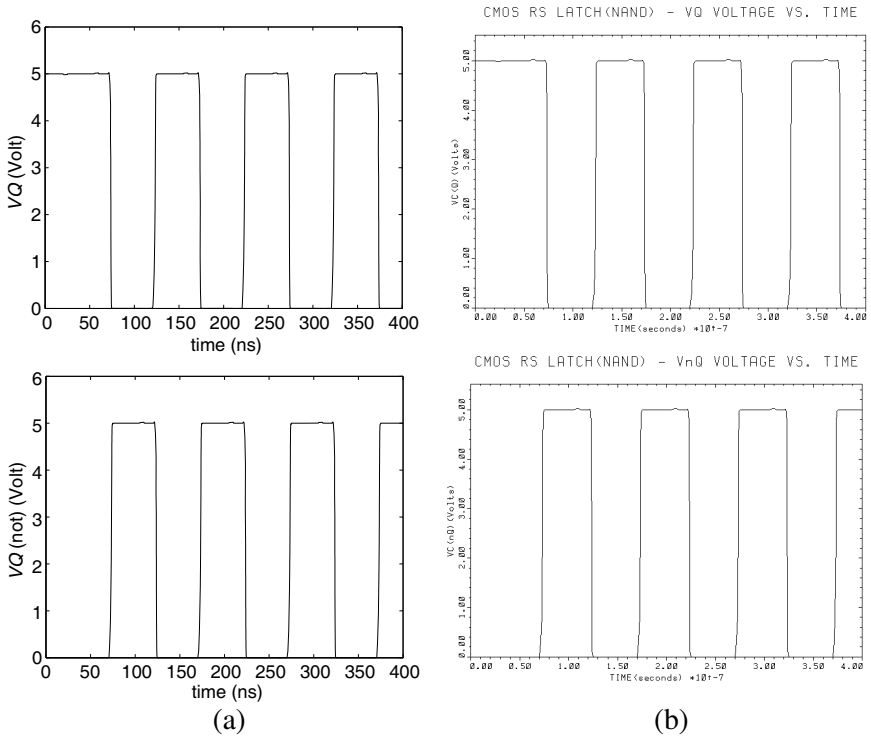

Figure 3. Output waveform of flip-flop 2. (a) Simulated result of the simulator. (b) Simulated result of MEDICI.

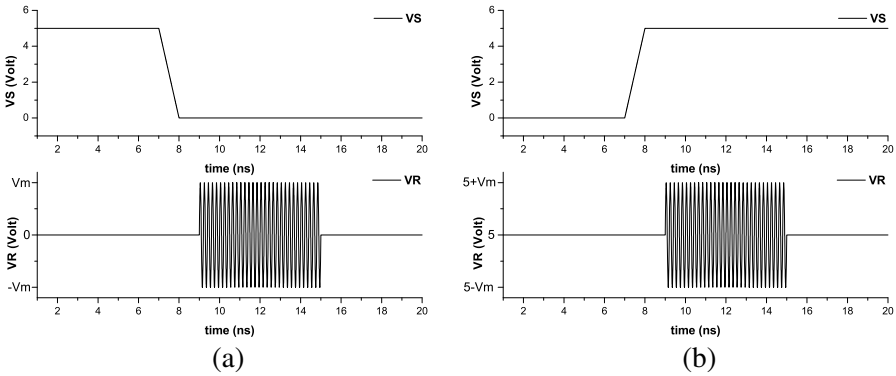

Figure 4. Input waveform of set and reset pin in the simulation. (a) Input waveform of flip-flop 1. (b) Input waveform of flip-flop 2.

4. RESULTS AND DISCUSSION

This section discusses the effects of microwave electromagnetic interference on CMOS RS flip-flops from the aspects of frequency and pulse width by examining the input/output characteristics and the behaviors of carriers in MOS devices. In the simulation, input waveforms of set and reset pin are displayed in Figure 4, where VS is the input waveform of set pin and VR is the input waveform of reset pin, respectively. Moreover, input power level is controlled to avoid the breakdown of MOS devices.

4.1. Effect of Frequency

The frequency of microwave electromagnetic interference varies from 1 GHz to 20 GHz. At the same time, the amplitude is maintained at 5 V and the pulse width is fixed at 6 ns in the simulation. Simulated results of flip-flop 1 and flip-flop 2 are depicted in Figures 5 and 6 respectively.

Both curves in Figure 5 and 6 show the identical trend which flip-flops maintain the output state without bit error at higher frequency. In the meantime, the fluctuation of outputs goes smaller, which implies that the effects of microwave electromagnetic interference get suppressed at higher frequency and the susceptibility of CMOS RS flip-flops to microwave electromagnetic interference is inversely proportional to the frequency. Furthermore, it is observed from the simulated results that flip-flop 2 doesn't switch its output state at the frequency of 5 GHz but flip-flop 1 does, which implies that the immunity of flip-flop 2 to microwave electromagnetic interference is stronger than that of flip-flop 1.

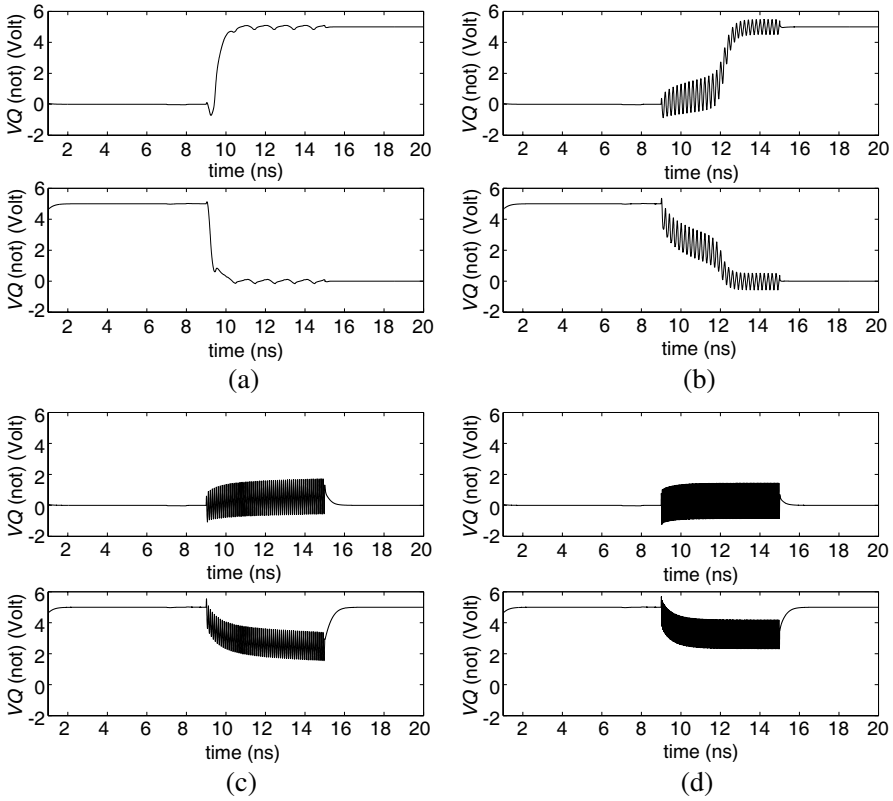

Figure 5. Simulated results of flip-flop 1 output waveform versus frequency. (a) 1 GHz. (b) 5 GHz. (c) 10 GHz. (d) 20 GHz.

Table 2. States of MOS devices in flip-flop 2 before microwave electromagnetic interference turns on.

	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
State	OFF	ON	OFF	OFF	OFF	ON	ON	ON

We consider the schematics of CMOS RS flip-flops as shown in Figure 1 to analyze the simulated results. For instance, considering flip-flop 2, the states of MOS devices in flip-flop 2 are given typically as Table 2 before microwave electromagnetic interference turns on. If flip-flop 2 changes its output state after injected microwave electromagnetic interference turns off, the states of MOS devices in flip-flop 2 are given as Table 3. Otherwise, MOS devices remain the previous state.

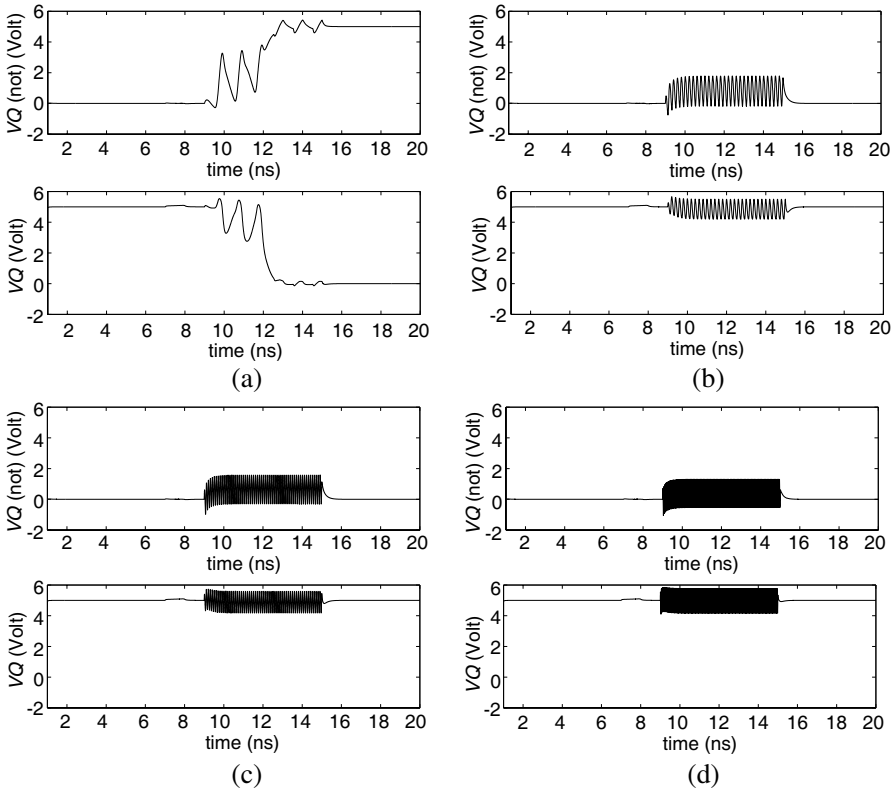

Figure 6. Simulated results of flip-flop 2 output waveform versus frequency. (a) 1 GHz. (b) 5 GHz. (c) 10 GHz. (d) 20 GHz.

Table 3. States of MOS devices in flip-flop 2 when it changes its output state.

	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
State	OFF	OFF	ON	OFF	ON	OFF	ON	ON

To demonstrate the analyses above, an example NMOS device of T_6 is selected. Electron distribution in the channel of T_6 is extracted at the time of 8 ns, 9 ns, ..., 16 ns while the frequency of microwave electromagnetic interference is 1 GHz (flip-flop 2 changes its output state at 1 GHz as shown in Figure 6(a)) and 5 GHz (flip-flop 2 don't change its output state as shown in Figure 6(b)), respectively. Furthermore, taking equilibrium electron distribution as reference, electron distributions are drawn in Figures 7 and 8.

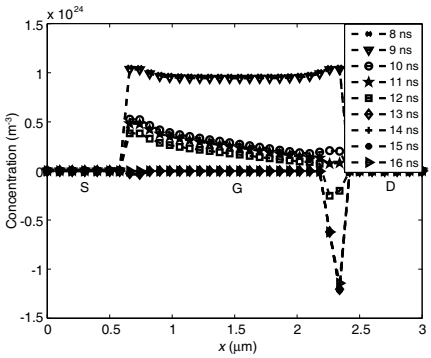

Figure 7. Electron distribution in the channel of T_6 versus time at 1 GHz.

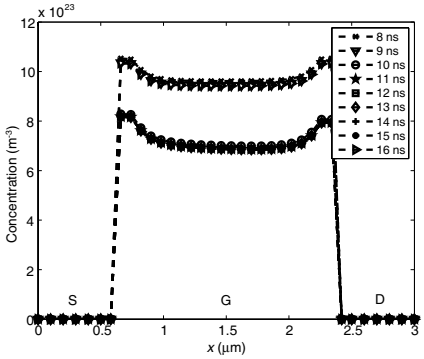

Figure 8. Electron distribution in the channel of T_6 versus time at 5 GHz.

It is observed from Figure 7 clearly that the electron concentration in the channel of T_6 decreases gradually to the level of equilibrium electron distribution finally, which means that T_6 turns from "ON" state to "OFF" state gradually under microwave electromagnetic interference at 1 GHz. Nevertheless, Figure 8 illuminates that the electron concentration remains almost the same level throughout. That implies T_6 maintains "ON" state all the time under microwave electromagnetic interference at 5 GHz. This is in accordance with the previous analysis and demonstrates that the susceptibility of CMOS RS flip-flops to microwave electromagnetic interference is inversely proportional to the frequency from the perspective of behaviors of carriers in MOS devices. The reason that the effects of microwave electromagnetic interference are suppressed at higher frequency is believed to be due to the capacitive by-pass path effect from gate to source and gate to body where the intrinsic small signal capacitances are the largest, providing a low impedance by-pass path to the ground for the pulsed interference at the higher frequency [16]. Therefore, only a part of microwave electromagnetic interference couples into the interior of CMOS RS flip-flops and causes little effects at higher frequency.

4.2. Effect of Pulse Width

In Figure 5(b), the output voltage under microwave electromagnetic interference could be divided into two stages. In the first stage (from 9 ns to about 12.5 ns), the state of outputs remains the same, although it shows the trend toward the opposite state. The second stage is

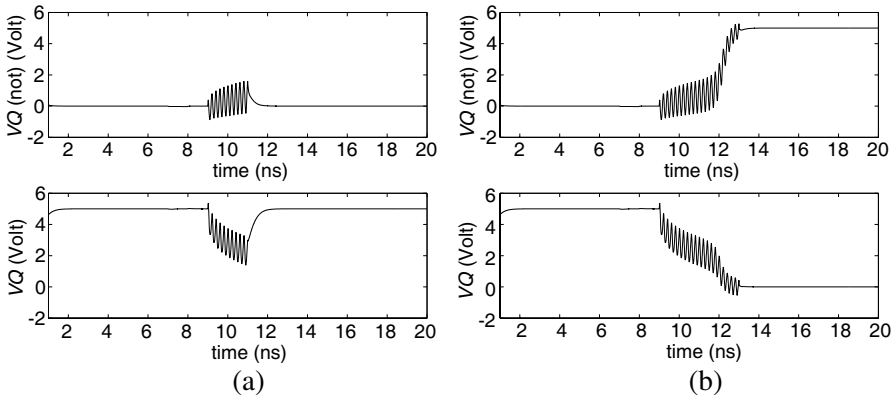

Figure 9. Simulated results of flip-flop 1 output voltage versus pulse width. (a) 2 ns. (b) 4 ns.

from 12.5 ns to 15 ns in which the state of outputs changes sharply and keeps the abnormal state even at the end of the injected microwave electromagnetic interference. Hence, if the pulse width is shortened, flip-flop 1 might not change its output state. Thus the effect of pulse width on flip-flop 1 has been studied.

First, two discrete pulse widths as 2 ns and 4 ns are selected, while the amplitude maintains at 5 V and the frequency fixes at 5 GHz in the simulation. Simulated results are exhibited in Figure 9.

It is clearly found that microwave electromagnetic interference with 5 V at 5 GHz is unable to switch the output state of flip-flop 1 as the pulse width is fixed at 2 ns, while the pulse width of 4 ns presents a similar result as shown in Figure 5(b). In [17], Fang mentioned that interference power threshold decreases with pulse width increasing when the other parameters of microwave electromagnetic interference keep the same. However, there is an inflection point, that is, the pulse width exceeding this point has little to do with power threshold obviously. Likewise, Wang [6] also referred to a related characteristic that the injected RF pulse power is inversely proportional to the pulse width. Therefore, inferring from the simulated result, the pulse width of 2 ns might be within the inflection point, that is to say, power level should increase to give rise to changes in the output state. On the other hand, the pulse width of 4 ns and 6 ns probably goes beyond the inflection point. Thus, their power threshold is believed to be identical.

Next, as the frequency is fixed at 5 GHz, pulse widths vary from 1 to 6 ns by step 1 ns and the amplitude starts from 0 V with the increment of 0.5 V. Under such circumstances, the power of microwave

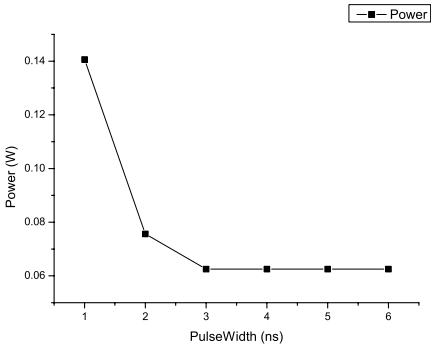

Figure 10. Interference power threshold versus pulse width.

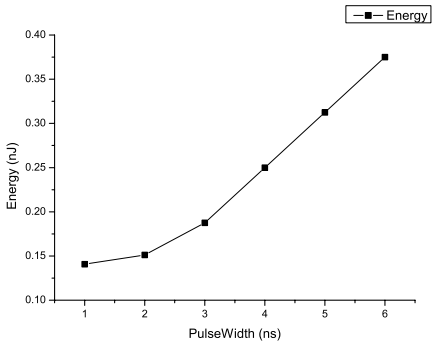

Figure 11. Interference energy threshold versus pulse width.

electromagnetic interference pulse P is given by

$$P = \frac{V_p^2}{8Z_s}, \tag{1}$$

where V_p is the amplitude in Volt and Z_s is the source impedance supposed to be 50 Ohm in this paper. Figure 10 shows the simulated result. It is found that the power of microwave electromagnetic interference is inversely proportional to the pulse width as stated above and 3 ns is determined to be so-called inflection point, which also verify the previous inference.

Further, the energy of microwave electromagnetic interference pulse E can be expressed from the power P

$$E = P \times \tau, \tag{2}$$

where τ is the pulse width. Simulated result is presented in Figure 11. Comparing simulated results in Figures 10 and 11, it is concluded that as the pulse width increases, the power threshold decreases steadily and once the pulse width exceeds the inflection point, the power threshold keeps almost the same, while the interference energy threshold increases significantly.

5. CONCLUSION

Simulated results of susceptibility of two categories of CMOS RS flip-flops to microwave electromagnetic interference have been reported. The method used in this paper might be complementary to those of previous works, which would improve the understanding of effects of microwave electromagnetic interference. This research

mainly concentrates on the relation between parameters of microwave electromagnetic interference and the susceptibility of CMOS RS flip-flops. Simulated results indicate that 1) the susceptibility of CMOS RS flip-flops to microwave electromagnetic interference is inversely proportional to the frequency, 2) the interference power threshold is inversely proportional to the pulse width and conversely the interference energy threshold is directly proportional to the pulse width, 3) amplitude, frequency and pulse width ought to be selected appropriately to bring about changes in the output state.

In addition, comparing the simulated results of these two categories of CMOS RS flip-flops, CMOS RS flip-flops composed of NAND gates have lower susceptibility to microwave electromagnetic interference than that of CMOS RS flip-flops composed of NOR gates. Thus, designers should choose CMOS RS flip-flops composed of NAND gates in the design of electronic systems to reinforce electromagnetic compatibility of the whole system.

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