

5 GHz LTCC-BASED APERTURE COUPLED WIRELESS TRANSMITTER FOR SYSTEM-ON-PACKAGE APPLICATIONS

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Abstract—A novel System-on-Package (SoP) implementation is presented for a transmitter (TX) module which makes use of electromagnetic coupling between the TX chip and the package antenna. The TX chip is realized in 0.13 μm CMOS process and comprises an on-chip antenna, which serves as the oscillator's inductor as well. The TX chip is housed in a Low Temperature Co-fired Ceramic (LTCC) package with a patch antenna. The on-chip antenna feeds the LTCC patch antenna through aperture coupling, thus negating the need for RF buffer amplifiers, matching elements, baluns, bond wires and package transmission lines. This is the first ever demonstration of wireless-interconnect between on-chip and package antennas which increases the gain and range of the TX module manyfold with respect to the on-chip antenna alone. Though the range of the TX SoP increases considerably, power consumption remains the same as that of the TX chip only. A simple analytical model for the new wireless-interconnect has been developed which helps determine the optimum position of the chip with respect to the aperture in the ground plane.

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1. INTRODUCTION

This era of miniaturized RF electronics requires innovative designs to achieve compact yet efficient wireless systems. Much of the recent RF research is focused on the System-on-Chip (SoC) and the System-on-Package (SoP) solutions [1, 2]. In the SoP domain, LTCC can offer numerous advantages like arbitrary number of layers which can not only embed passives but can also realize vertical integration of RF modules. Moreover, the low loss LTCC substrates are very suitable for efficient antenna design. Recently, a V-band RF front end has been implemented in LTCC with an integrated package antenna [3]. Though the SoC is a more size efficient approach, the on-chip antennas are usually very inefficient because of the lossy nature of the Si substrates. Since the RF chip has to be packaged anyways, designers tend to rely on integrated package antennas. A few successful demonstrations of RF circuit integration with LTCC antennas have been reported in the recent past [4, 5]. Generally, the RF circuits are connected to the feed line of an LTCC antenna through bond wires or solder balls. Typically, this arrangement requires an isolating buffer amplifier and bond pads on the chip. Moreover, these antennas are matched to the RF circuits through matching elements. This approach not only adds to the number of design steps, cost and overall power consumption, but the presence of bond wires also makes the module less attractive.

Obviously, the best approach to overcome the above limitations is to establish a wireless connection between the RF circuit and the LTCC antenna. Aperture coupling is a well established technique for non-contact or wireless feeding of microstrip patch antennas [6, 7]. Lately, an active integrated patch antenna fed with the aperture coupling technique has been demonstrated [8]. In addition, a silicon based aperture coupled patch antenna is demonstrated in [9]; however they both utilize a conventional microstrip feed line. This only eliminates the physical connection between the feed line and the antenna; the connections and components required between the integrated circuit (IC) and the antenna feed line cannot be removed. In [10], a parasitic coupling approach is demonstrated to couple an array of patches to the IC; however this is done through a hypothetical IC and antenna. The measured results in [10] are obtained using a microstrip feed and via combination, which does not reflect the complexities of real chip-to-package coupling. Our previous work [11] alleviated the above problems by proposing a novel SoP concept, which employs a wireless interconnect between the RF chip and the LTCC antenna. The design makes use of electromagnetic coupling from the on-chip loop antenna, which also acts as an inductor for the Transmitter (TX)

Voltage Controlled Oscillator (VCO), to a slot in the ground plane and eventually to the LTCC patch antenna. It requires neither a buffer amplifier and connecting bond pad on the chip, nor matching elements or feed lines on the package. It also eliminates the requirement for a balun to connect differential circuits to the single ended antennas or vice versa. This paper furthers the work by describing the challenges associated with the physical implementation of the concept. It also presents a simple analytical model to support the new concept. The wireless interconnect between the on chip and package antenna occurs over a very short distance. This means that the two antennas are located in the reactive near field region of each other and thus their wireless link is governed by a much more complex relationship as compared to the radiating near-field or far field wireless links. Developing a full analytical model for such a reactive near field wireless link is not practical. In this paper, we have addressed this issue by simulating the effect of the coupling with the LTCC antenna on the inductance (L) and quality factor (Q) of the TX VCO inductor (which has a strong relation to input impedance of the on-chip antenna) using finite element method simulator HFSS. In parallel, we have developed a simple analytical model based on the near magnetic field components of an electrically small antenna to show the effect of the LTCC antenna on the on-chip antenna using a physical model. With the help of the equations shown, designers can predict the optimum position of the TX chip with respect to the slot in the ground plane.

To the author's best knowledge, this is the first ever LTCC aperture coupled patch antenna implementation with direct feeding from a TX on-chip antenna. The on-chip antenna coupling to the LTCC patch antenna improves the TX module gain and range manyfold in comparison to the on-chip antenna alone. The proposed chip to patch coupling strategy not only reduces the number of components, cost, and power consumption but also simplifies the design process for future RF SoP modules.

2. ANALYTICAL MODEL

The aperture-coupled technique to feed a microstrip patch antenna has been proposed by Pozar [6]. This feeding mechanism utilizes coupling of electromagnetic energy from a microstrip line to a slot in its ground plane. The slot, also typically known as aperture, couples the power to the patch antenna. The initial model developed by Pozar made use of the cavity model of the patch antenna. In the cavity model, the microstrip patch is considered to be a cavity bounded by four magnetic and two electric walls, with the magnetic current source to

be located in the aperture [12]. The magnetic current is assumed to be uniform in the volume above the slot, whereas the electric field components near the slot are considered through the reactive power evaluation. The coupling between the microstrip line magnetic field and the slot electric field can be considered to be through an inductive link. Therefore the inductance L and quality factor Q of the TX VCO inductor is strongly related to the coupling strength. For example, a reduction of Q actually means increase in the radiation resistance, which in turn results in stronger coupling of power to the slot and eventually to the antenna. This effect has been discussed in detail in Section 4.

Besides the cavity method, the aperture coupled patch antenna fed through a microstrip line has been modeled via other techniques as well. Pozar demonstrated an analytical model based on the reciprocity method [13]. This was followed by many investigations based on different methods like the moment method [14], modal expansion method [15] and transmission line analysis [16]. A simple analytical model is described in [17] employs an optimization technique and can be a starting point for more rigorous analyses. A full wave analysis using the spectral domain approach was reported in [18]. However, all these models deal with a microstrip feed of the aperture-coupled patch, which is not the case here. In order to model the coupling through an on-chip loop antenna instead of a microstrip line, a simple analytical method is derived here. The principle of the method is similar to the reciprocity theorem.

The fields from the on-chip loop couple to the slot in the ground plane and from the slot they couple to the patch antenna. The latter coupling is identical to previous implementations and thus the new analytical model need not investigate it. The coupling between the on-chip loop antenna and the slot in the ground plane is the focus of this analysis. The goals are to 1) find the effect of a slot opening in the ground plane on a conducting loop near it, 2) obtain an expression to quantify the coupling from the loop to the slot, and 3) determine the optimum position of the loop with respect to the slot for best coupling.

Consider a conducting loop near a ground plane, with an excitation current J_1 . It is enclosed in a hemisphere with surface S and volume V as shown in Figure 1. Let us assume that the electric and magnetic fields in the hemisphere, due to source J_1 , are E_1 and H_1 respectively. For this case, it is assumed that there is no slot in the ground plane as shown in Figure 1(a). Let the length of source J_1 to be denoted as Δl . Since Δl is quite small, J_1 is assumed to be equal to a constant current density J_o . For the second case (shown in Figure 1(b)), a slot of length l_s and width w_s is present in the ground

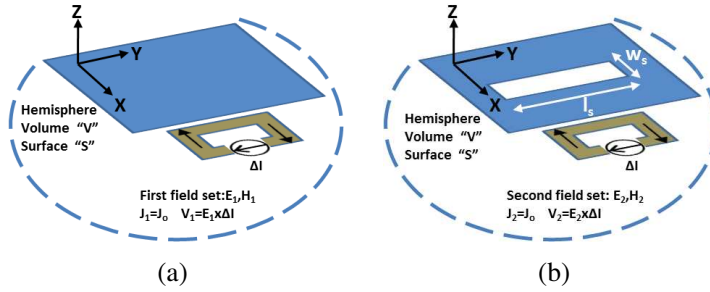


Figure 1. Problem definition (a) Case 1 with no slot, (b) Case 2 with slot.

plane. The electric and magnetic fields, due to excitation source J_2 , are denoted as E_2 and H_2 respectively. Consistent with the first case, J_2 is assumed to be equal to J_0 .

Applying Maxwell equations to both cases,

Case 1

$$\nabla \times E_1 = -j\omega\mu H_1 \quad (1)$$

$$\nabla \times H_1 = j\omega\varepsilon E_1 + J_1 \quad (2)$$

Case 2

$$\nabla \times E_2 = -j\omega\mu H_2 \quad (3)$$

$$\nabla \times H_2 = j\omega\varepsilon E_2 + J_2 \quad (4)$$

Multiplying both sides of (1) with H_2 and (2) with E_2 :

$$H_2 \cdot (\nabla \times E_1) = -j\omega\mu H_1 \cdot H_2 \quad (5)$$

$$E_2 \cdot (\nabla \times H_1) = j\omega\varepsilon E_1 \cdot E_2 + J_1 \cdot E_2 \quad (6)$$

Similarly multiplying both sides of (3) with H_1 and (4) with E_1 :

$$H_1 \cdot (\nabla \times E_2) = -j\omega\mu H_2 \cdot H_1 \quad (7)$$

$$E_1 \cdot (\nabla \times H_2) = j\omega\varepsilon E_2 \cdot E_1 + J_2 \cdot E_1 \quad (8)$$

Subtracting (8) from (5), and (7) from (6) and using well known vector equations:

$$-\nabla \cdot (E_1 \times H_2) = j\omega\varepsilon E_2 \cdot E_1 + J_2 \cdot E_1 + j\omega\mu H_1 \cdot H_2 \quad (9)$$

$$-\nabla \cdot (E_2 \times H_1) = j\omega\varepsilon E_2 \cdot E_1 + J_1 \cdot E_2 + j\omega\mu H_1 \cdot H_2 \quad (10)$$

Subtracting (10) from (9):

$$-\nabla \cdot (E_1 \times H_2 - E_2 \times H_1) = J_2 \cdot E_1 - J_1 \cdot E_2 \quad (11)$$

Equation (11) is consistent with reciprocity theorem, without the magnetic sources [19]. Applying this to the complete hemisphere

$$\int_s (E_1 \times H_2 - E_2 \times H_1) \cdot ds = \int_v (E_1 \cdot J_2 - E_2 \cdot J_1) dv \quad (12)$$

where $S = S_\infty + S_g + S_{slot}$.

The integral over the remaining surface (S_∞) and the ground (S_g) is zero. Also E_1 is zero over the slot surface (S_{slot}) because the slot is not present in the first case. Therefore (12) can be simplified as follows.

$$\int_{slot} (-E_2 \times H_1) \cdot ds = \int_v (E_1 \cdot J_2 - E_2 \cdot J_1) dv \quad (13)$$

Since the analysis is based on the assumption that the source current density stays constant ($J_1 = J_2 = J_o$), the coupling between the slot in the ground plane and the conducting loop will be reflected as a change in the source voltage. Let us assume that V_1 represents the source voltage in case 1 and V_2 the source voltage in case 2, and the change in the voltage is denoted as ΔV . Since the excitation current is only defined over the feed gap and is zero elsewhere, the volume integral is limited to the area of the feed gap Δl . Equation (13) can now be written as

$$\begin{aligned} \int_{slot} (-E_2 \times H_1) \cdot ds &= E_1 \Delta l \cdot \Delta s J_1 - E_2 \Delta l \cdot \Delta s J_2 \\ \int_{slot} (-E_2 \times H_1) \cdot ds &= E_1 \Delta l \cdot I_1 - E_2 \Delta l \cdot I_2 \end{aligned}$$

where I_1 and I_2 are the currents in case 1 and case 2 respectively, and are equal to a constant current I_o . Δs represents the surface area of the loop feed gap. Now the loop terminal voltages are found through:

$$\begin{aligned} \int_{slot} (-E_2 \times H_1) \cdot ds &= (V_1 - V_2) I_o \\ \int_{slot} (-E_2 \times H_1) \cdot ds &= \Delta V I_o \\ \frac{1}{I_o} \int_{slot} (-E_2 \times H_1) \cdot ds &= \Delta V \end{aligned} \quad (14)$$

This is an important conclusion as it relates the electric field of the slot in the ground plane to the loop's change in the voltage due to the coupling between them. In (14), H_1 can be found by applying image theory to the fields of case 1, as shown in Figure 2. This field is proportional to J_o and is a function of the position of the loop. The electric field over the slot can be represented by (15), where E_o is the amplitude of slot's electric field [19].

$$E_2 = E_o \cos(\pi y/l_s) \hat{x} \quad (15)$$

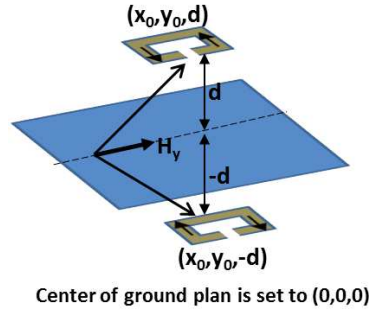


Figure 2. Image theory for case 1 (with no slot).

Since ds is in the z direction, (15) can be written as:

$$\int_{slot} (-E_0 \cos(\pi y/l_s) \hat{x} \times H_1) \cdot ds = \Delta V I_o$$

$$\int_{slot} (-E_0 \cos(\pi y/l_s) H_y) \cdot ds = \Delta V I_o \quad (16)$$

H_y varies with the position of the loop and therefore (16) can evaluate the optimum relative position of the loop with respect to the slot for best coupling. From (16), it is clear that the position of the loop with respect to the slot must be unsymmetrical in order to have better coupling. If the loop is symmetrically located above the slot, the opposite directed fields would cancel each other out. So it is better to have a non-symmetrical position for the loop, preferably near the edges of the slot. This is an interesting result which is totally different from the microstrip fed aperture coupled antenna where the microstrip feed must be in the centre of the slot to achieve best coupling [6]. This difference can be explained through Figure 3, where the fields for both cases 1) microstrip feed, and 2) the loop antenna feed are shown over the slot in the ground plane. It can be seen in Figure 3(a) that the fields induced in the slot through the microstrip are in the same direction and hence a symmetrical position of the microstrip line with respect to the slot will enhance the fields. In contrast, Figure 3(b) depicts that the loop antenna induces oppositely directed fields in the slot and hence a symmetrical position with respect to the slot will cancel these fields. The best position is almost near the edge of slot, which has also been observed in HFSS simulations. Details of HFSS simulation model are presented in Section 4.

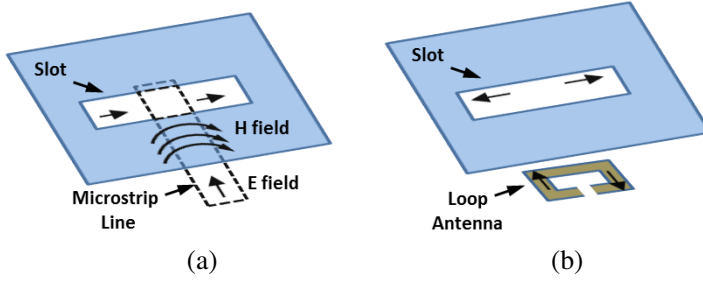


Figure 3. Comparison of coupling between a microstrip feed and a loop antenna feed.

The near magnetic field of a small loop is the same as that of a short magnetic dipole and is well known [19].

$$\begin{aligned}
 H_y &= H \cdot \hat{y} \\
 H_y &= \frac{I_o s}{2\pi} e^{-jkr} \left(\frac{jk}{r^2} + \frac{1}{r^3} \right) \cos \theta \sin \theta \sin \phi \\
 &\quad + \frac{I_o s}{4\pi} e^{-jkr} \left(\frac{-k^2}{r} + \frac{jk}{r^2} + \frac{1}{r^3} \right) \sin \theta \cos \theta \sin \phi \\
 H_y &= \frac{I_o s}{4\pi(x^2 + y^2 + z^2)^{1/2}} e^{-jk(x^2 + y^2 + z^2)^{1/2}} \\
 &\quad \times \left[3jk(x^2 + y^2 + z^2)^{1/2} + 3 - k^2(x^2 + y^2 + z^2) \right] (zy)
 \end{aligned} \tag{17}$$

where $I_o s$ is the magnetic moment, s is the area of the loop. Let us assume that d is the vertical distance of the slot from the loop and it is placed at the coordinates shown in Figure 2. Employing image theory, it is assumed that a similar current source is present on the other side of the ground plane. The total field on the slot will be the superposition of the fields from both the loop and its image. If the H field due to the loop is H_{yl} and due to its image is H_{yi} , the total magnetic field H_{Ty} on the slot is given as:

$$\begin{aligned}
 H_{Ty} &= H_{yl} + H_{yi} \\
 H_{Ty} &= 2H_y
 \end{aligned} \tag{18}$$

If x_o , y_o and d are the coordinates of the loop, then the relative distance between the loop and any position along the slot can be expressed as

$(x-x_o, y-y_o, z-d)$. Inserting H_y of (17) into (18) yields:

$$H_{T_y}(x, y, z) = \frac{2I_o s}{4\pi[(x-x_o)^2 + (y-y_o)^2 + d^2]^{5/2}} e^{-jk[(x-x_o)^2 + (y-y_o)^2 + d^2]^{1/2}} \\ \times \left[3jk[(x-x_o)^2 + (y-y_o)^2 + d^2]^{1/2} + 3 \right. \\ \left. - k^2[(x-x_o)^2 + (y-y_o)^2 + d^2] \right] (d(y-y_o)) \quad (19)$$

Inserting this magnetic field in (15) yields:

$$I_o \Delta V = \int_{slot} (-E_0 \cos(\pi y/l_s)) \frac{2I_o s}{4\pi[(x-x_o)^2 + (y-y_o)^2 + d^2]^{5/2}} \\ \times e^{-jk[(x-x_o)^2 + (y-y_o)^2 + d^2]^{1/2}} \times \left[3jk[(x-x_o)^2 + (y-y_o)^2 + d^2]^{1/2} \right. \\ \left. + 3 - k^2[(x-x_o)^2 + (y-y_o)^2 + d^2] \right] (d(y-y_o)) ds \quad (20)$$

The current I_o cancels out from both sides of (20). Inserting the design values of d , s and l_s in (20) and plotting ΔV against varying positions across the length of the slot, results in Figure 4. It can be seen that the maximum coupling happens close to the edges of the slot and the coupling goes to zero when the loop is exactly at the centre of the slot. HFSS simulation results of the same structure are also plotted for comparison. A good match between the two curves is obtained, which validates the simple analytical model. Many approximations (loop geometry, uniform current distribution) have been used in this model, which can explain the discrepancy in Figure 4. Nonetheless, the model can provide a very good initial estimate of the on-chip antenna optimum position with respect to the slot in the ground plane.

3. RF TRANSMITTER WITH ON-CHIP ANTENNA

The RF TX comprises a VCO with an on-chip antenna realized in $0.13 \mu\text{m}$ CMOS process [20]. The TX is designed for the unlicensed 5.2 GHz Unlicensed National Information Infrastructure (UNII) indoor band. The inductor of the VCO tank is optimized to perform double duty, acting as the on-chip antenna as well. Since the antenna serves as an inductor for the TX VCO, full 3-D electromagnetic simulations using the High Frequency Structure Simulator (HFSS) are employed to obtain the required inductance “ L ” and quality factor “ Q ” while optimizing the radiation efficiency. A lumped element model is then derived for the antenna/inductor. This model allows circuit simulation of the complete antenna/TX combination.

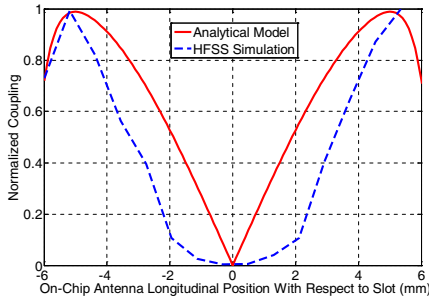


Figure 4. Comparison of coupling between the loop and the slot through HFSS and analytical model.

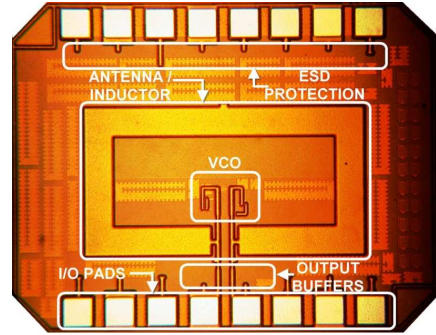


Figure 5. TX VCO chip microphotograph.

The loop antenna is a natural candidate for an antenna/inductor design as it is inherently inductive in nature and exhibits a broad radiation pattern. Moreover, since it is a differential antenna, it can be integrated with differential circuitry directly without needing a balun. Finally, its geometry allows placement of the active TX circuitry in the centre of the loop. The simulation model includes the bond pads for testing the inductor/antenna. The VCO is placed in the centre of the loop through feed lines with microsurgery (lasering) points. These bond pads can be removed through a laser trimming technique for normal operation of the VCO connected to the antenna. The on-chip antenna/inductor provides an L of 1.3 nH with a Q of 19 at 5.2 GHz and demonstrates a gain of -34 dBi with the maximum radiation along the plane of the loop.

The TX makes use of open loop direct VCO modulation. An inductor capacitor (LC) cross-coupled differential VCO topology has been chosen for this work. The VCO outputs are buffered through cascaded inverters. The three stage buffer on either side of the differential VCO ensures minimum loading on the VCO. A separate bias line for the buffers ensures that they are turned on only when required. The buffers are included for measurements and connection to external antennas. The TX chip can independently operate through the on-chip antenna with limited range [20]. In this situation, the buffers remain off. The complete TX chip microphotograph is shown in Figure 5. The VCO draws an average current of 2.8 mA and consumes 3.3 mW of power from a 1.2 V supply.

4. LTCC PACKAGE WITH ANTENNA

By incorporating the TX chip into an LTCC package with an antenna, the transmission range can be greatly increased as highly efficient antennas can be realized in the LTCC medium. However, the use of an off-chip antenna requires the buffer amplifiers to isolate the VCO from any loading. Our previous work [11] clearly demonstrates that the power consumption of the TX module increased to 38 mW with a conventional connection to an off-chip antenna. On the contrary, a wireless connection such as the proposed aperture coupled technique can avoid this additional power consumption.

Aperture coupling is employed here, mainly, because it will allow direct coupling of the TX on-chip antenna to the LTCC patch antenna without the need of a microstrip feed line. In addition, the buffer circuits can remain off. Moreover, the common ground plane between the radiating antenna and the circuits [21, 22], can act as a shield for the TX circuits. However, a limitation of this technique is that the slot in the ground plane can radiate considerably in the backward direction. This unwanted radiation can be minimized by choosing the optimum slot length with respect to the patch size.

The Ferro A6-S LTCC tape system is employed in this design. Each layer has a fired thickness of 100 μm . The substrate is 8 layers thick and it houses a 300 μm thick RF chip in a cavity. The cavity thickness is chosen to be 600 μm to accommodate the chip and the biasing bond wires. The LTCC fabrication rules require a minimum of two layers beneath the cavity, thus resulting in a total substrate thickness of 800 μm . The superstrate which will contain the antenna can be of any other material, however for simplicity the same LTCC tape system is used for the antenna as well.

The design procedure is as follows. First, a conventional aperture coupled patch antenna with a microstrip feed line is simulated in HFSS. This determines the approximate size of the patch antenna at 5.2 GHz, the feed location and the slot dimensions. Next, the microstrip line is replaced with the TX chip. The design is optimized in terms of air gap thickness for maximum coupling between the on-chip antenna and the LTCC patch antenna through the slot in the ground plane. This increases the overall gain of the TX module; however there are many other parameters which can be tuned to increase the gain further. The thicknesses of the air gap and the superstrate determined this way are an initial estimate of the design and will change during the final optimization. The patch antenna dimensions of 1.7 cm $\times$ 1.7 cm are obtained in simulations. The substrate, superstrate and ground plane dimensions are 2 cm $\times$ 2 cm.

The chip is placed in a cavity sized $4.8\text{ mm} \times 3.8\text{ mm}$ at the same location where the microstrip line fed the patch. The size of the cavity is chosen so as to leave enough room for the power routing and bond wires after placing the chip in the cavity. The cavity size remains the same for the lower four layers, however it is made the same width as that of the slot in the ground plane for the top two layers. This is done to avoid fabrication complexities. The patch antenna is on the bottom-most layer of the superstrate. The air gap is realized through four corner posts made of the same LTCC tape system as the substrate. The layer by layer layout of the aperture coupled module along with the final dimensions is shown in Figure 6.

The front view of the module is shown in Figure 7. The power and ground pads in the cavity connect to the pads on the bottom of the substrate through vias. The bottom pads are utilized to connect to the contacts of the battery. The battery can be simply glued to the bottom of the substrate as shown in Figure 7.

The design is sensitive to a number of parameters, the most important being the location, length, and width of the slot in the ground plane. Other important parameters are the air gap and superstrate thicknesses. Extensive parametric simulations are required to optimize many parameters at the same time. The goal is to maximize the gain of the module by efficient coupling between the on-

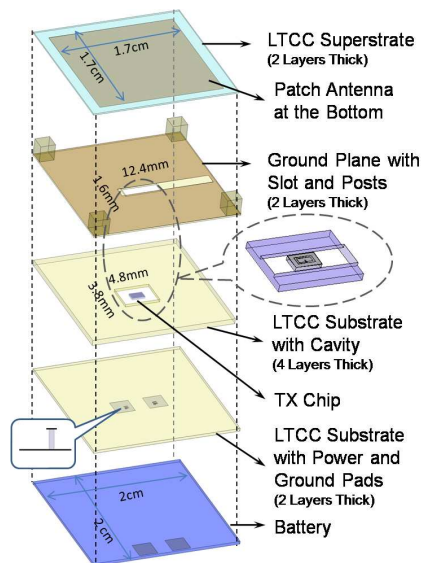


Figure 6. Layer by layer description of the complete LTCC TX module.

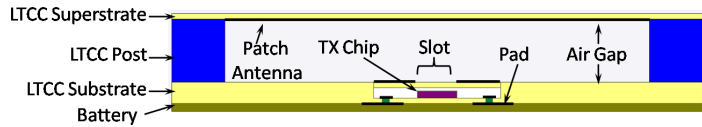


Figure 7. Cross-sectional view of the complete LTCC TX module.

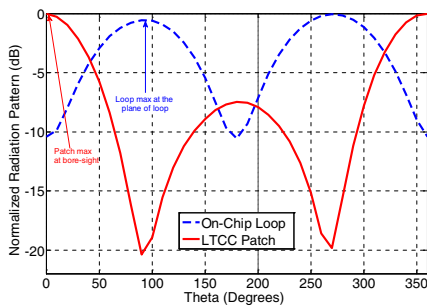


Figure 8. Radiation pattern transformation from on-chip loop to LTCC patch.

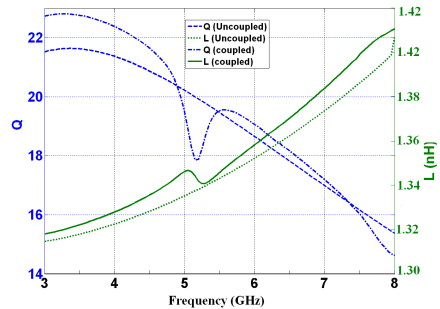


Figure 9. TX VCO inductor performance with and without aperture coupling.

chip antenna and the LTCC antenna through the slot in the ground plane, without affecting the RF properties of the circuit. Initially, keeping the slot length and width the same as that of the microstrip fed case, the thicknesses of the air gap and superstrate are optimized. After achieving a reasonable gain value, the thicknesses are kept constant and the slot length and width are optimized. It is observed in simulations that maximum coupling between the on-chip antenna and slot occurs when the former is near the edge of the slot, which is consistent with the analytical model as has been shown in Figure 4. Finally, the thicknesses of the air gap and superstrate are optimized again with the new slot dimensions. It is worth mentioning here that this technique works on the near field coupling and thus the far field radiation pattern of the on-chip antenna is insignificant here.

A combination of air gap thickness of 2 mm and superstrate thickness of 1.8 mm increases the gain of the module from the on-chip antenna gain of -34 dBi to 0.5 dBi. This remarkable result is achieved without any physical connection or elaborate matching of the RF circuit to the external antenna. However, the superstrate thickness of 1.8 mm (18 LTCC layers) is not an economically viable solution because it does not contain any other passives except the patch antenna.

Therefore the design is re-optimized for a thinner superstrate by compromising somewhat on the gain. The final superstrate thickness of 0.2 mm, with an air gap thickness of 2.4 mm, yields a gain of -2.3 dBi. This gain is still 32 dB more than that of the on-chip antenna gain. Figure 8 shows the normalized radiation pattern of both the on-chip loop antenna and the LTCC aperture coupled patch antenna.

The transformation of the radiation pattern to a bore-sight maximum (typical patch antenna pattern) from a plane of the antenna maximum (typical small loop pattern) confirms the successful operation of the aperture coupled module. The back lobe in case of LTCC patch is reduced to a level approximately 10 dB lower than the front lobe by optimizing the slot length. The on-chip antenna/inductor's RF performance has been affected slightly but is still within acceptable operational limits of the TX module. Figure 9 compares the L and Q of the on-chip inductor with and without coupling to the slot and the patch antenna. A clear notch can be seen in both the L and Q curves at the frequency of interest, which shows the coupling; however, the deviation from the nominal values is not detrimental.

5. LTCC MODULE FABRICATION & MEASUREMENTS

Since the aperture coupled module requires the TX chip to be placed in a cavity embedded underneath two layers and a ground plane, it cannot be fabricated as a single piece without subjecting the TX chip to high firing temperatures. Also the fabrication complexities do not allow simultaneous firing of the LTCC layers with the ground plane, the four posts and the superstrate with integrated patch antenna. Therefore the module is fabricated in four parts, (1) the 6 substrate layers with a cavity, (2) the 7th and 8th substrate layers with ground plane, (3) the four corner posts, and (4) the two superstrate layers with patch antenna.

The next step is to place the TX chip in the cavity. This is done by utilizing silver epoxy in the cavity and baking the substrate with the TX chip at 150°C . The TX chip is now wire bonded to the bias pads. After the placement of the chip and wire bonding, the remaining substrate layers with ground plane are placed on top of the chip in the cavity. Then the LTCC posts are positioned on the four corners of the ground plane and the superstrate with patch antenna is supported on these posts. All the bonding between the different parts of the modules is achieved through the silver epoxy and baking process. The individual components, the sequence of their integration and the final module are shown in Figure 10.

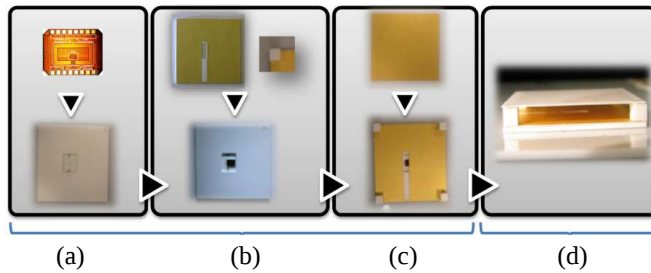


Figure 10. TX aperture coupled SoP (a) TX chip placed in LTCC substrate, (b) ground plane with slot and LTCC post placed on substrate with the TX chip, (c) superstrate with patch antenna placed on the rest of the module, (d) complete SoP module.

In order to measure the relative increase in gain for the LTCC aperture coupled module as compared to the TX chip with on-chip antenna, the latter is placed in cavities of two similar LTCC substrates. One of them is left open from the top (i.e., Figure 10(a)) whereas the other has all the parts of the module in place (i.e., Figure 10(d)). A horn is employed as the receive antenna and is connected to a spectrum analyzer. First, the received power is measured from the module with the on-chip antenna radiating into free space, and then the same is done for the module where the on-chip antenna radiates into the slot that couples to the patch antenna. The difference in the measured power levels indicates that the aperture coupled module has 10 dB more gain as compared to the TX chip alone. The radiation pattern of the module is measured manually by rotating the receive antenna around the TX SoP and recording the level of power at different angles. The normalized radiation pattern (drawn through the interpolation of measured data points) is shown in Figure 11. The measured radiation pattern shows a bore-sight maximum which is expected if the patch mode is excited. Consistent with simulations, the module which contains the uncovered TX chip demonstrates the maximum radiated power to be along the chip edges or 90° from the bore-sight. However, the same module, when covered with the rest of the SoP components displays the maximum radiated power to be at bore-sight. This shift in radiation pattern confirms the desired operation of the aperture coupled patch antenna. The most attractive feature of this design is that the 10 dB increase in the TX SoP radiated power as compared to that of the TX chip alone comes without any increase in DC power consumption. It was observed in measurements, that both designs, TX chip alone and aperture coupled LTCC SoP, consume 3.3 mW of DC power.

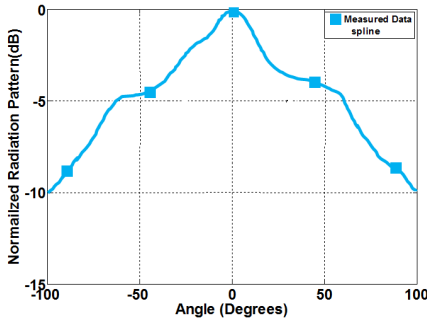


Figure 11. TX SoP measured radiation pattern.

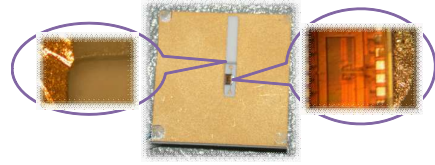


Figure 12. TX SoP zoomed in view of fabrication tolerances.

6. FABRICATION AND POST PROCESSING TOLERANCES SENSITIVITY ANALYSIS

Though the measured relative gain is less than what is observed in simulations, a number of factors explain this result. It has been observed in simulations that the design is sensitive to many parameters, like the thickness of the air gap, length and width of the slot, placement of the chip with respect to the slot and the position of the posts on the ground plane. Close inspection and thickness measurements of the fabricated modules revealed that there are many things, which are not according to the simulation model. Firstly, the substrate thickness is approximately $60\text{ }\mu\text{m}$ less than the simulated $800\text{ }\mu\text{m}$. The four posts height, which is responsible for the air thickness, varies between 2.2 to 2.3 mm instead of 2.4 mm. Moreover, the slot width is not uniform for the entire length as can be clearly seen in Figure 12. The slot becomes wider over the cavity as compared to the regular substrate. The cavity itself has rounded corners, contrary to the original design. Furthermore, the deposition of silver epoxy is done manually, so the thickness and uniformity could not be controlled as shown in Figure 12. It not only reduces the distance between the on-chip antenna and the slot but also causes the chip to be slightly tilted. Similar issues are observed in the manual placement and gluing of the four posts. Finally, this particular fabricated TX chip is working at 5.3 GHz, which is different from the LTCC package design frequency of 5.2 GHz.

The above-mentioned tolerances in fabrication and post processing have been analysed in post measurement simulations and the results are shown in Figure 13. As can be seen from Figures 13(a) and (b), the gain is severely affected by the slot dimensions. The original width of the slot 1.6 mm has been varied in simulations by 2.5 mm in steps

of 0.5 mm (from -0.5 mm till 2 mm), where 0 represents the original slot width in Figure 13(a). As the width of the slot starts to increase the SoP gain reduces considerably. This simulation is done for slot width on either side of the chip and the results have been consistent. The result not only shows the effect of varying slot width but also captures the effect of chip positioning error with respect to the slot width. Figure 13(b), on the other hand, demonstrates that decreasing slot length (from its original length of 12.4 mm represented as 0) at one end while keeping the other end static with respect to the chip reduces the gain as well. This simulation confirms that the resonant length of the slot is important for this particular feed mechanism, in addition to the longitudinal placement of the chip. From the simulations, it is clear that the chip must be placed right at the edge of the slot, however physically it is not possible to do it very accurately. This effect has

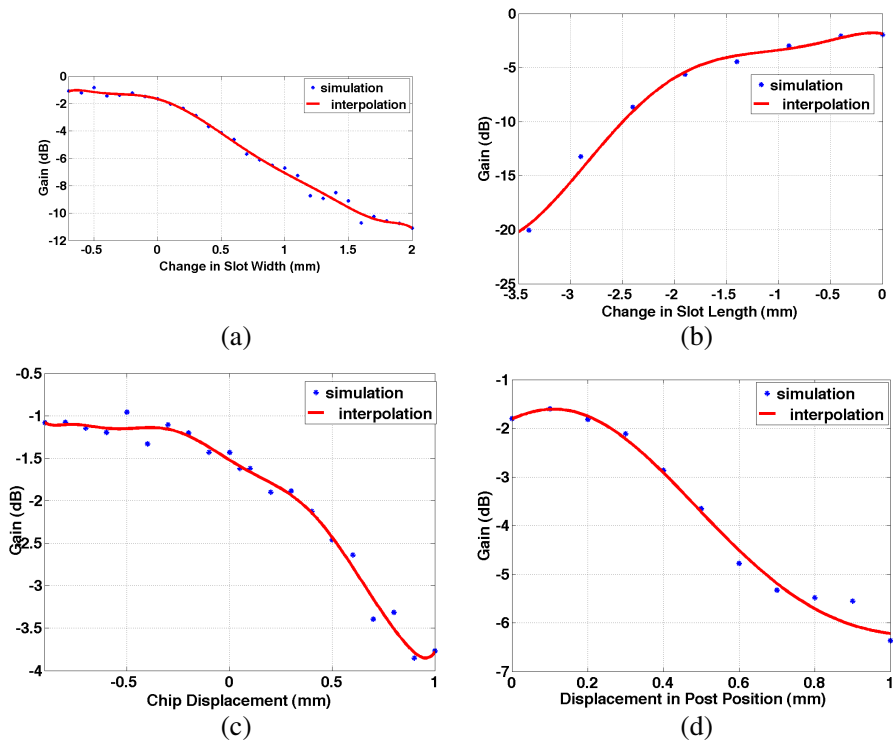


Figure 13. Aperture coupled SoP Gain versus (a) change in slot width, (b) change in slot length, (c) chip longitudinal displacement with respect to slot edge, (d) corner posts displacement with respect to ground plane edges.

been demonstrated in Figure 13(c), where the chip is displaced with respect to the slot edge (original position of the chip is at 0 mm and the slot edge is at -0.9 mm) and has reduced the gain by 3 dB for a mere 1 mm chip displacement. Another interesting result, shown in Figure 13(d), highlights the sensitivity of the posts placement on the ground plane to realize the air gap. The posts initially designed to be uniformly placed at the ground plane edges (represented by 0 mm displacement), cause the gain to reduce by approximately 5 dB for an error of 1 mm in their positioning.

Other simulations investigating the lower measured gain included the non-accurate substrate and air gap thickness and the shift of chip operating frequency. However, these errors result in minor gain reduction. Due to the simulation complexity, the tilt of the chip due to uneven epoxy underneath could not be simulated. When all the above-mentioned discrepancies are included in the simulation model simultaneously, a gain 17 dB lower than the initially simulated value is achieved. Though this result is not exactly similar to the measured result, it is quite close to it and indicates that the fabrication and post processing tolerances are the major contributors towards the lower gain value in measurements. The issue of LTCC tolerances is critical for aperture coupled designs and has also been reported in [23]. This means that by adequately addressing the tolerance issues in fabrication and automating the post-processing, the optimum results predicted in simulations can be achieved with ease. Continuing maturity of LTCC fabrication processes should remedy this situation.

7. CONCLUSION

A novel LTCC based TX SoP implementation has been demonstrated which makes use of on-chip antenna to LTCC package antenna coupling through an aperture in the ground plane. The strategy is useful as it eliminates the need of isolating buffers, bond pads, bond wires, matching elements, baluns and transmission lines. It not only reduces the number of components and simplifies SoP design but also consumes lower power. Since the cost of such LTCC modules increases almost linearly with the increasing number of layers and components, the design presented in this work brings in great cost reductions as compared to a conventional approach of wire bonding the RF chip to an off-chip antenna. The chip coupling to LTCC patch antenna improves the TX module gain and range considerably as compared to the on-chip antenna alone, without affecting the RF circuit performance and power consumption. A simple analytical method is described to model the new coupling between the on-chip antenna and the slot in the ground plane.

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