

AN ANN-BASED SMALL-SIGNAL EQUIVALENT CIRCUIT MODEL FOR MOSFET DEVICE

N. Li¹, X. P. Li^{1,*}, and S. G. Quan²

¹School of Electronic Engineering, Beijing University of Posts and Telecommunications, Beijing 100876, China

²Department of Electronic Engineering, Namseoul University, 331-707, Korea

Abstract—An ANN-based small-signal equivalent circuit model for 130 nm MOSFET device is proposed in this paper. The proposed model combines the conventional small-signal equivalent circuit model and artificial neural networks (ANNs) to achieve higher accuracy. Good agreement is obtained between proposed model and measured results confirming the validity and effectiveness of proposed model.

1. INTRODUCTION

In recent years, CMOS technology has been adopted in radio frequency integrated circuit (RFIC) design, because of its low cost, low power and high integration related to other technologies. In addition, continuously scaling down of gate length and the consequently increased of operation frequency have made MOSFET devices be the attractive candidate in RFIC application (LNA, mixer, etc.) [1–4, 26], and then much attention has been paid to radio frequency integrated circuit based on CMOS processes. To predict the accurate performance of the circuit at required frequency bands and also reduce the design cycle, device models are very critical in circuit design session [5–7, 27, 28].

Artificial Neural Networks (ANNs) are information processing systems that have been widely applied in the RF and microwave modeling tasks as an unconventional alternative. Through a process called training, ANNs have the ability of fitting any nonlinear behavior of passive and active component/circuit from experimental data and

Received 21 September 2011, Accepted 2 November 2011, Scheduled 14 November 2011

* Corresponding author: Xiuping Li (xpli@bupt.edu.cn).

generating an ANN model function that can be used to describe the port-characters of component/circuit [8–12]. Compared to other conventional modeling techniques, such as numerical modeling method, which could be computationally expensive, or analytical method, which could be different to obtain for new devices, or empirical modeling solution, whose range and accuracy could be limited [8], the ANNs modeling technique is more efficient. In addition, under the condition of the urgent need of developing models for new device [19], ANNs modeling method could supply a way of fast model development.

In this paper, a new small-signal modeling approach that combined the conventional equivalent circuit model and artificial neural networks (ANNs) is proposed. Each intrinsic circuit element in the conventional equivalent circuit model of MOSFET device is regarded as a sub-artificial neural network (SANN). Good agreement is obtained between trained model results and measured data under different bias conditions.

The organization of the paper is as follows: the artificial neural network modeling technique is introduced in Section 2; the proposed ANN-based small-signal equivalent circuit model for MOSFET is described in Section 3; the experimental results and discussion are given in Section 4; finally, the conclusion is presented in Section 5.

2. ANN MODELING TECHNIQUE INTRODUCTION

An artificial neural network (ANN) is a distributed information processing system whose network configuration is a critical characteristic. It is widely used in the optimization of passive components and microwave nonlinear device modeling [13–18]. The multiplayer perceptron (MLP) is a popularly applied neural network structure [8]. The basic processing unit/element called neuron is grouped into layer in MLP structure. Three kinds of layers are defined in MLP structure, the first and last layers are called input and output layer, respectively. The layers that are between input and output layers are called hidden layers [29]. The hidden layers are the core part of a neural network, the complexity of hidden layers determine the complexity of the nonlinear behavior that the neural network can be trained to learn. In general, the more complicated the nonlinear behavior is, the more hidden layers and neurons will be added. Typically, a kind of widely used MLP structure consists of one input layer, one output layer and one hidden layer, referred to as a three-layer MLP (or 3LP). The structure is shown in Fig. 1.

The interconnections between the neurons shown in Fig. 1 are called links or synapses. The arrow indicates the propagation direction

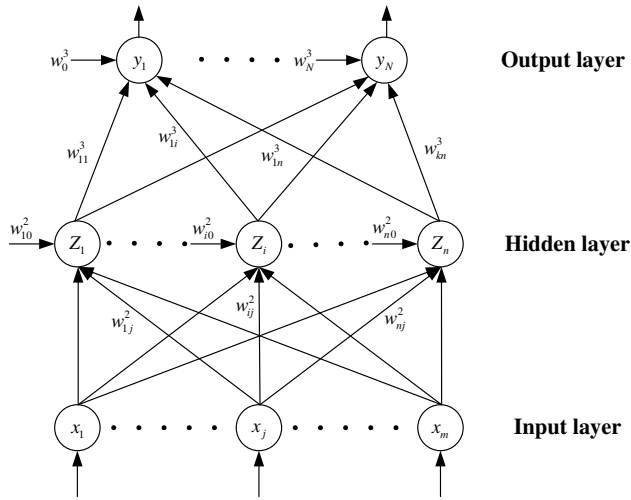


Figure 1. The three-layer MLP (3LP) neural network structure.

of signals between the neurons. A weight parameter w is allocated to each link. Accordingly, w_{ij}^l represents the weight parameter of link between the j th neuron of the $(l-1)$ th layer and i th neuron of the l th layer. w_k^3 and w_{i0}^2 are the biases of each neuron of hidden and output layers.

For a given vector $\vec{x} = (x_1, x_2, \dots, x_m)^T$, the output vector $\vec{y} = (y_0, y_1, \dots, y_N)^T$ of a three-layer MLP neural network can be computed by:

$$y_k = w_k^3 + \sum_{i=1}^n w_{ki}^3 \sigma \left(w_{i0}^2 + \sum_{j=1}^m w_{ij}^2 x_j \right), \quad k = 0, 1, 2 \dots N \quad (1)$$

where $\sigma(\cdot)$ represents the activation function, which is set for each neuron. The typical activation function is the sigmoid function given by

$$\sigma(x) = \frac{1}{(1 + e^{-x})} \quad (2)$$

In modeling task, the artificial neural network is then trained to learn electrical behavior that is described by input-output sample pairs, also called training data. Specifically training is to determine the neural model parameters, i.e., neural network weights w_{ij}^l , such that the ANN model predicted output best matches that of the training data. The testing data (new input-output samples) is used to test the accuracy of the ANN model.

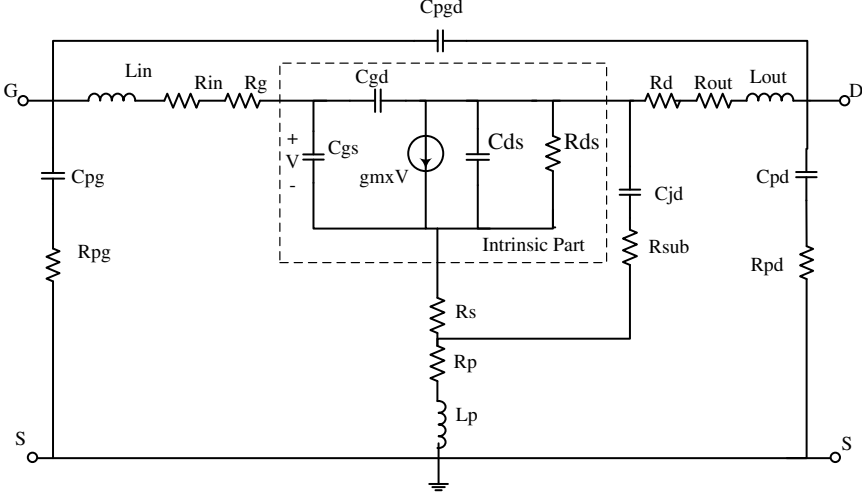


Figure 2. The small-signal equivalent circuit model for MOSFET device.

3. PROPOSED MODEL AND MODELING METHOD

3.1. Equivalent Circuit Model

The small-signal equivalent circuit model considering the substrate parasitic effects and pad parasitic effects for silicon-based MOSFET device is shown in Fig. 2 [3, 12, 20]. The electrical elements in equivalent circuit can be divided into two parts: the intrinsic parts (in dotted box) and extrinsic parts, respectively.

The intrinsic parts are bias-dependent, the C_{gs} represents the capacitance of gate-channel, and the gate-source overlap; C_{gd} represents the gate-drain overlap capacitance; C_{ds} is the drain-source capacitance. The extrinsic parts are often bias-independent, the capacitances C_{pg} and C_{pd} in series with R_{pg} and R_{pd} are used to model the pad coupling effects and substrate losses. C_{pgd} models the coupling effects between two signal pads. R_g is used to model the distributed effect at gate channel. The R_d and R_s represent the drain and source resistances, respectively, which are mainly caused by the lightly doped extensions of the drain and source diffusions. g_m is the transconductance, R_{ds} is the drain resistance. To consider the substrate parasitic effects, a substrate network consisting of a series connection of C_{jd} and R_{sub} is adopted.

The parasitic elements of pad and interconnection line can be

determined by using formulas as follow:

$$C_{pg} = \frac{\text{Im} \left(Y_{11}^{\text{open-pad}} + Y_{12}^{\text{open-pad}} \right)}{2\pi f} \quad (3)$$

$$C_{pd} = \frac{\text{Im} \left(Y_{22}^{\text{open-pad}} + Y_{21}^{\text{open-pad}} \right)}{2\pi f} \quad (4)$$

$$R_{pg} = \text{Re} \left(\frac{1}{Y_{11}^{\text{open-pad}} + Y_{12}^{\text{open-pad}}} \right) \quad (5)$$

$$R_{pd} = \text{Re} \left(\frac{1}{Y_{22}^{\text{open-pad}} + Y_{21}^{\text{open-pad}}} \right) \quad (6)$$

$$C_{pgd} = \frac{-\text{Im} \left(Y_{12}^{\text{open-pad}} \right)}{2\pi f} \quad (7)$$

$$R_{in} = \text{Re} \left(Z_{11}^{\text{short-pad}} - Z_{12}^{\text{short-pad}} \right) \quad (8)$$

$$L_{in} = \frac{\text{Im} \left(Z_{11}^{\text{short-pad}} - Z_{21}^{\text{short-pad}} \right)}{2\pi f} \quad (9)$$

$$R_{out} = \text{Re} \left(Z_{22}^{\text{short-pad}} - Z_{21}^{\text{short-pad}} \right) \quad (10)$$

$$L_{out} = \frac{\text{Im} \left(Z_{22}^{\text{short-pad}} - Z_{12}^{\text{short-pad}} \right)}{2\pi f} \quad (11)$$

$$R_p = \text{Re} \left(Z_{12}^{\text{short-pad}} \right) \quad (12)$$

$$L_p = \frac{\text{Im} \left(Z_{21}^{\text{short-pad}} \right)}{2\pi f} \quad (13)$$

where the open-pad indicates the measurement data of opened pad dummy device, and short-pad indicates the measurement data of shorted pad dummy device after de-embedding the pad parasitic.

The another extrinsic resistances R_g , R_d , R_s and substrate network R_{sub} and C_{jd} can be analytically determined [21, 22].

3.2. Proposed Modeling Method

3.2.1. ANN-based Small-signal Modeling Technique

Compared with extrinsic elements in equivalent circuit model shown in Fig. 2, which is bias-independent, the intrinsic elements are mainly

affected by V_{gs} and V_{ds} . Conventionally, the empirical function in which V_{gs} and V_{ds} are two independent variables is applied to characterize the nonlinear relationship between element values and bias conditions, such as Angelov model [23]. Analytically directly extract the intrinsic elements is based on multi-bias S parameters measured by vector network analyzer. Although the values of intrinsic elements can be determined directly at different bias condition by a series of analytical closed function [5, 16], the extracted values of these intrinsic elements remain some variations with frequency [16]. To store all the values at each frequency points will pay the price of using much storage memory and making the models run slowly. Optimization methods are often applied to find an optimum value among the extracted values, the accuracy of the optimization methods can vary depending upon initial value and optimization methods, therefore, may result in non-physical and non-unique solutions.

In [24, 25], Sirakawa et al. have proposed a multiplayer perceptron structure for large signal model of HEMT. For the proposed ANN-based small-signal modeling approach in this paper, a sub-ANN (SANN) for each intrinsic element is adopted, the modeling idea is illustrated in Fig. 3. The frequency variable is adopted in characterizing the variations with frequency; the SANNs for each intrinsic element can be formulated by function of bias conditions and frequency, shown in formulas (14)–(18):

$$C_{gs} = f_{ANN}^{C_{gs}}(V_{gs}, V_{ds}, Freq) \quad (14)$$

$$C_{ds} = f_{ANN}^{C_{ds}}(V_{gs}, V_{ds}, Freq) \quad (15)$$

$$C_{gd} = f_{ANN}^{C_{gd}}(V_{gs}, V_{ds}, Freq) \quad (16)$$

$$r_{ds} = f_{ANN}^{r_{ds}}(V_{gs}, V_{ds}, Freq) \quad (17)$$

$$g_m = f_{ANN}^{g_m}(V_{gs}, V_{ds}, Freq) \quad (18)$$

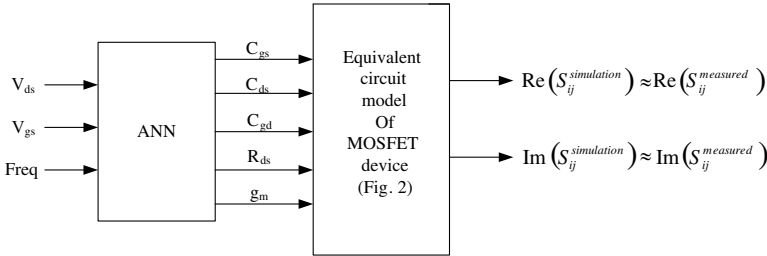


Figure 3. The ANN-based small-signal modeling configuration for MOSFET device.

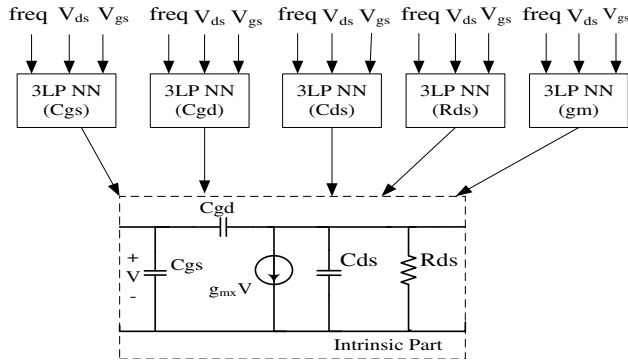


Figure 4. The ANN-based small-signal modeling approach for MOSFET device.

The S -parameter of equivalent circuit model shown in Fig. 2 is divided into two parts, real part and imaginary part, respectively. Fig. 3 shows the configuration that is used to model the real and imaginary parts of S -parameter of the equivalent circuit model together. The ANN part shown in Fig. 3 is the core part in the proposed modeling approach. The concrete ANN-based modeling technique for intrinsic part of equivalent circuit model is illustrated in Fig. 4. As for ANN in Fig. 3, a SANN, which is a three layer perceptron structure, where only one hidden layer is used, is applied for each intrinsic element.

3.2.2. The Training Strategy

The training process is an optimization procedure, the weight values and bias values in neural network are adjusted in order to make the outputs of neural network fit to the particular nonlinear behavior. Unlike the conventional training process [8, 11, 12], the output data of the adopted neural networks is not available, in the proposed modeling procedure, the outputs of the neural networks will be sent to the intrinsic part of equivalent circuit and conduct the S -parameter simulation with the whole equivalent circuit. As for the whole ANN-based equivalent circuit MOSFET model, the inputs are bias conditions and frequencies, the outputs are the S -parameter of equivalent circuit.

In the proposed modeling approach, the training process is illustrated by a flow chart in Fig. 5.

The whole training process consists of ANNs' training and S -parameter simulation of equivalent circuit. The Quasi-Newton algorithm is used for ANNs' training. The whole error of real and imaginary parts of S -parameter will be evaluated by using formulas

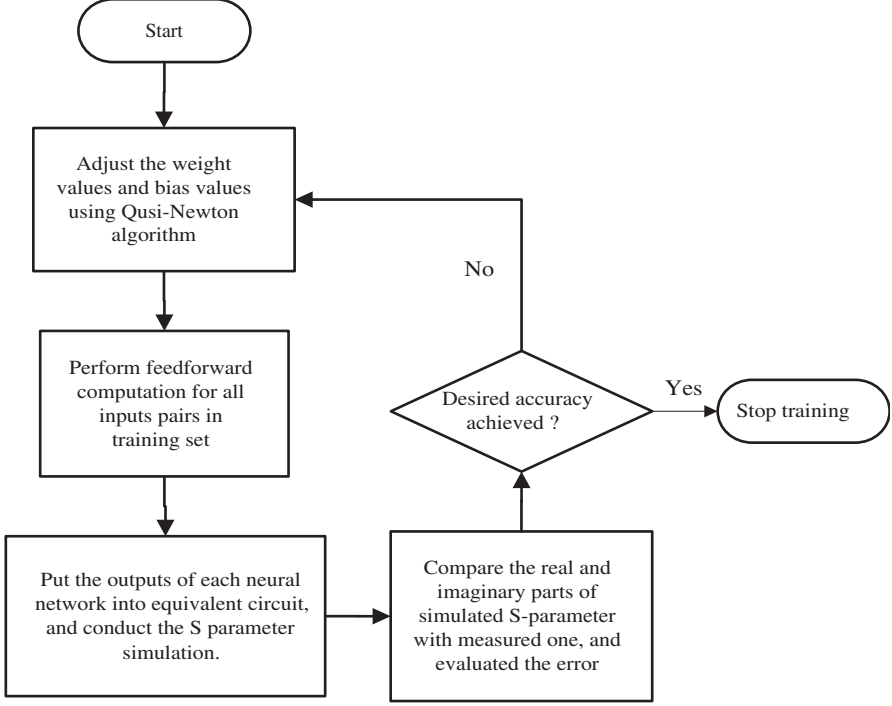


Figure 5. The flow chart demonstrating the training process in proposed modeling approach.

(19) and (20) in proposed training process, respectively.

$$E_{Training}(w) = \frac{1}{n} \sum_{k=1}^n \left(\text{Re} \left(S_{ij,k}^{model} \right) - \text{Re} \left(S_{ij,k}^{measured} \right) \right)^2 \quad (19)$$

$$E_{Training}(w) = \frac{1}{n} \sum_{k=1}^n \left(\text{Im} \left(S_{ij,k}^{model} \right) - \text{Im} \left(S_{ij,k}^{measured} \right) \right)^2 \quad (20)$$

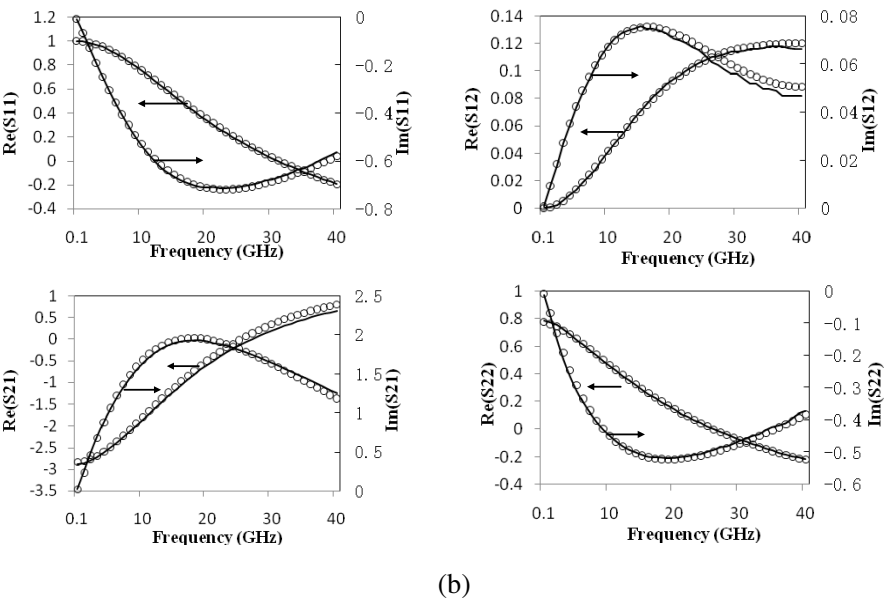
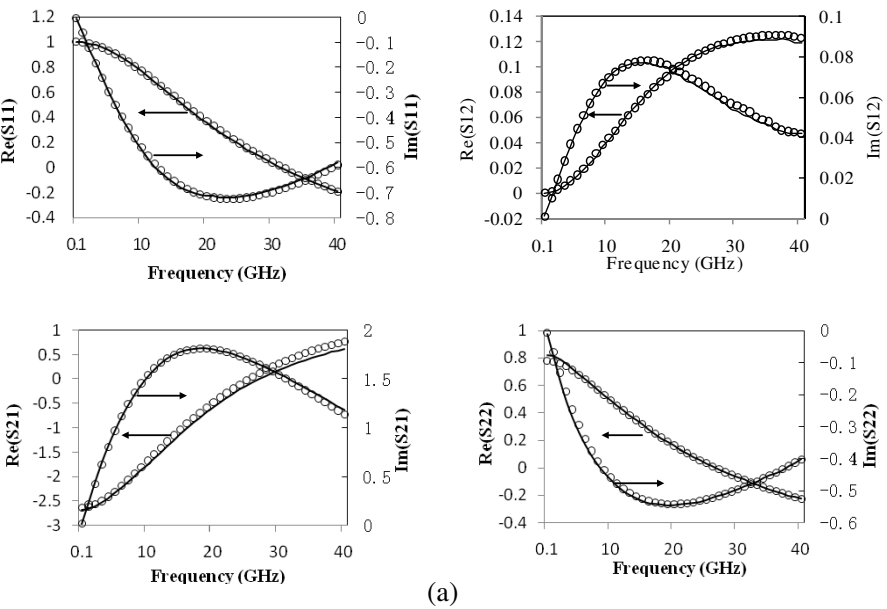
where the model represents the S -parameter simulation outputs of trained ANN-based model, the measured represents the measured S -parameter data.

4. EXPERIMENT RESULTS AND DISCUSSION

130 nm channel length, 5 μm channel width per figure and 8 figures SMIC 130 nm-process manufactured MOSFET device is applied as object to be modeled. The S -parameter is measured from 100 MHz

to 40 GHz by VNA under the bias conditions V_{gs} and V_{ds} voltages from 0.2 v to 1.2 v in the step value of 0.2 v.

The extracted extrinsic element values of the equivalent circuit



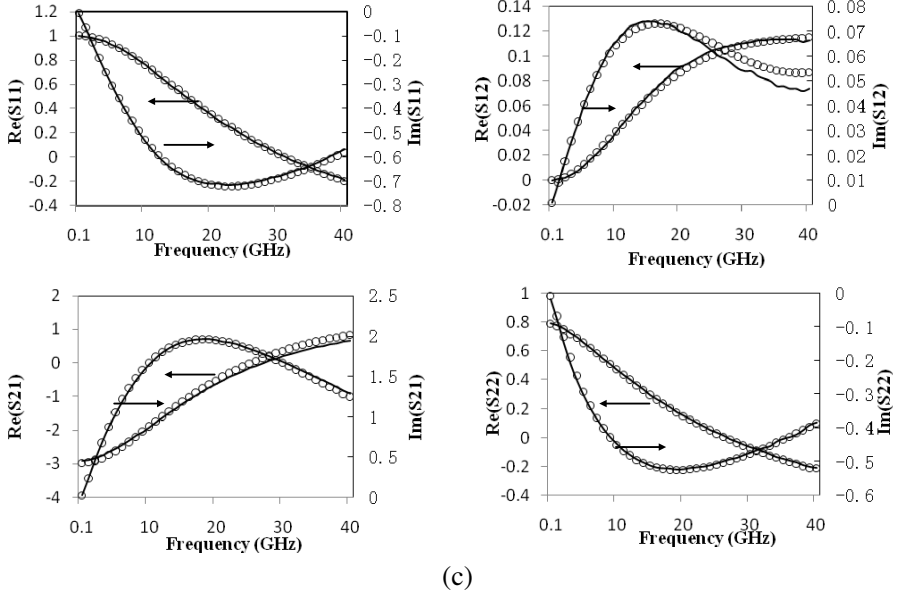


Figure 6. Comparison of S -parameters between measured data (—) and proposed model results (o). (a) $V_{gs} = 0.8\text{ v}$, $V_{ds} = 0.6\text{ v}$, (b) $V_{gs} = 1\text{ v}$, $V_{ds} = 0.8\text{ v}$, (c) $V_{gs} = 1.2\text{ v}$, $V_{ds} = 1.2\text{ v}$.

are listed in Table 1. The value of transconductance delay time is considered as constant value, $\tau = 0.27\text{ ns}$. The number of hidden neuron of applied three-Layer Perceptron neural networks in proposed model is shown in Table 2. The training data set is chosen from measured S -parameter of the MOSFET device biased at saturation region. The remained measured S -parameter of bias conditions $V_{gs} = 0.8\text{ v}$ and $V_{ds} = 0.6\text{ v}$, $V_{gs} = 1\text{ v}$ and $V_{ds} = 0.8\text{ v}$ and $V_{gs} = 1.2\text{ v}$ and $V_{ds} = 1.2\text{ v}$ will be used to test the interpolation and extrapolation of trained proposed model.

The trained proposed model results have been compared with measured data in Fig. 6. Good agreement is obtained between measured data and proposed model results under different bias conditions over the frequency range of 100 MHz–40 GHz. The demonstrated comparisons indicate the interpolation and extrapolation ability of proposed model. The errors between model results and measured data are evaluated by error function:

$$E_{ij} = \frac{1}{N-1} \sum_{n=1}^N \left| \frac{S_{ij}^{\text{measured}} - S_{ij}^{\text{model-results}}}{S_{ij}^{\text{measured}}} \right|, \quad (i, j = 1, 2) \quad (21)$$

where the N is the number of sampling points. Table 3 gives the errors of S -parameter between proposed model results and measured data under the three different bias conditions.

Table 1. The extracted extrinsic elements.

	Parameter	Value
Pad parasitic parameters	R_{pg}	$28\ \Omega$
	R_{pd}	$28\ \Omega$
	C_{pg}	$20.45\ \text{fF}$
	C_{pd}	$20.80\ \text{fF}$
	C_{pgd}	$1.15\ \text{fF}$
Feedline parasitic parameters	R_{in}	$0.56\ \Omega$
	R_{out}	$0.43\ \Omega$
	R_p	$0.046\ \Omega$
	L_{in}	$64.46\ \text{pH}$
	L_{out}	$58.27\ \text{pH}$
	L_p	$31.49\ \text{pH}$
Extrinsic resistances	R_g	$6.6\ \Omega$
	R_d	$5.91\ \Omega$
	R_s	$4.14\ \Omega$
Substrate parasitic parameters	R_{sub}	$507.62\ \Omega$
	C_{jd}	$26.58\ \text{fF}$

Table 2. The number of hidden neuron in the three-Layer Perceptron neural networks.

C_{gs}	C_{gd}	C_{ds}	r_{ds}	g_m
25	25	25	28	25

Table 3. The average relative errors of S -parameter under different bias condition (%).

Bias conditions	S_{11}	S_{12}	S_{21}	S_{22}
$V_{gs}=0.8\ \text{V}, V_{ds}=0.6\ \text{V}$	1.2	2.8	5.8	1.2
$V_{gs}=1.0\ \text{V}, V_{ds}=0.8\ \text{V}$	1.3	2.5	5.8	1.8
$V_{gs}=1.2\ \text{V}, V_{ds}=1.2\ \text{V}$	0.9	3.7	6.1	1.4

5. CONCLUSION

ANN-based small-signal equivalent circuit model and relative modeling approach is proposed for 130 nm MOSFET device in this paper. The proposed model and modeling approach provide a way of fast and accurate modeling development. Through proposed training strategy, the trained model results show a good agreement between measured data confirming the validity and effectiveness of proposed model and modeling approach, also a high accuracy of proposed model is achieved.

ACKNOWLEDGMENT

This work is supported by the project 61072009 from National Nature Science Foundation of China (NSFC), Beijing Nova Program 2008A050 and program for new Century Excellent Talents 2007 (NECT-07-0108). Funding for this paper was provided by Namseoul University.

REFERENCES

1. Morifuji, E., H. S. Momose, T. Ohguro, T. Yoshitomi, H. Kimijima, F. Matsuoka, M. Kinugawa, Y. Katsumata, and H. Iwai, "Future perspective and scaling down roadmap for RF CMOS," *Symposium on VLSI Technology Digest of Technical Papers*, 165–166, 1999.
2. Cheng, Y. H., M. J. Deen, and C. H. Chen, "MOSFET modeling for RF IC design," *IEEE Trans. Electron Devices*, Vol. 52, 1286–1303, 2005.
3. Chan, Y.-J., C.-H. Huang, C.-C. Weng, and B.-K. Liew, "Characteristics of deep-submicrometer MOSFET and its empirical nonlinear RF model," *IEEE Trans. Microwave Theory Tech.*, Vol. 46, 611–615, May 1998.
4. Yoon, J., H. Seo, I. Choi, and B. Kim, "Wideband LNA using a negative GM cell for improvement of linearity and noise figure," *Journal of Electromagnetic Waves and Applications*, Vol. 24, No. 5–6, 619–630, 2010.
5. Lovelace, D., J. Costa, and N. Camilleri, "Extracting small-signal model parameters of silicon MOSFET transistors," *IEEE MTT-S Dig.*, 865–868, San Diego, CA, 1994.
6. Biber, C. E., M. L. Schmatz, and T. Morf, "Improvements on a MOSFET model for nonlinear RF simulation," *IEEE MTTS Dig.*, 865–868, Denver, CO, 1997.
7. Lee, S., Y. H. Kyu, C. S. Kim, J. G. Koo, and K. S. Nam, "A novel approach to extracting small-signal model parameters

- of silicon MOSFET's," *IEEE Microw. Guid. Wave Lett.*, Vol. 7, 75–77, 1997.
8. Zhang, Q. J., K. C. Gupta, and V. K. Devabhaktuni, "Artificial neural networks for RF and microwave design: From theory to practice," *IEEE Trans. Microwave Theory Tech.*, Vol. 51, 1339–1350, 2003.
 9. Li, X., J. Gao, and G. Boeck, "Printed dipole antenna design by artificial neural network modeling for RFID application," *International Journal of RF and Microwave Computer-aided Engineering*, Vol. 16, No. 6, 607–611, 2006.
 10. Li, X., J. Gao, J.-G. Yook, and X. Chen, "Bandpass filter design by artificial neural network modeling," *Asia-Pacific Microwave Conference*, Vol. 2, 713–716, 2005.
 11. Li, X. and J. Gao, "Pad modeling by using artificial neural network," *Progress In Electromagnetics Research*, Vol. 74, 167–180, 2007.
 12. Li, X., Y. Li, and J. Zhao, "Ann-based pad modeling technique for MOS-FET devices," *Progress In Electromagnetics Research*, Vol. 118, 303–319, 2011.
 13. Li, X., J. Gao, and G. Boeck, "Microwave nonlinear device modeling using artificial neural network," *Semicond. Sci. Technol.*, Vol. 21, 833–840, 2006.
 14. Mohamed, M. D. A., E. A. Soliman, and M. A. El-Gamal, "Optimization and characterization of electromagnetically coupled patch antennas using RBF neural networks," *Journal of Electromagnetic Waves and Applications*, Vol. 20, No. 8, 1101–1114, 2006.
 15. Jin, L., C. L. Ruan, and L. Y. Chun, "Design *E*-plane bandpass filter based on EM-ANN model," *Journal of Electromagnetic Waves and Applications*, Vol. 20, No. 8, 1061–1069, 2006.
 16. Acikgoz, H., Y. L. Bihan, O. Meyer, and L. Pichon, "Microwave characterization of dielectric materials using bayesian neural networks," *Progress In Electromagnetics Research C*, Vol. 3, 169–182, 2008.
 17. Vakula, D. and N. V. S. N. Sarma, "Fault diagnosis of planar antenna arrays using neural networks," *Progress In Electromagnetics Research M*, Vol. 6, 35–46, 2009.
 18. Michalski, J. J., "Artificial neural networks approach in microwave filter tuning," *Progress In Electromagnetics Research M*, Vol. 13, 173–188, 2010.
 19. Zhang, L., J. Xu, M. C. E. Yagoub, R. T. Ding, and Q. J. Zhang, "Efficient analytical formulation and sensitivity

- analysis of neurospace mapping for nonlinear microwave device modeling,” *IEEE Trans. Microwave Theory Tech.*, Vol. 53, 2752–2767, 2005.
20. Kim, C.-H., C. S. Kim, H. K. Yu, and K. S. Nam, “Unique extraction of substrate parameters of common-source MOSFET’s,” *IEEE Microwave Guided Wave Lett.*, Vol. 9, 108–110, Mar. 1999.
 21. Chang, K. M. and H. P. Wang, “A new small-signal MOSFET model and parameter extraction method for RF IC’s application,” *Microelectron J.*, Vol. 35, 749–759, 2004.
 22. Gao, J. and A. Werthof, “Direct parameter extraction method for deep submicrometer metal oxide semiconductor field effect transistor small signal equivalent circuit,” *IET Microwaves Antennas Propag.*, Vol. 3, 564–571, 2009.
 23. Angelov, I., H. Zirath, and N. Rorsman, “A new empirical nonlinear model for HEMT and MESFET devices,” *IEEE Trans. Microwave Theory Tech.*, Vol. 40, 2258–2266, 1992.
 24. Sirakawa, K., M. Shimiz, N. Okubo, and Y. Daido, “A large signal characterization of an HEMT using a multilayered neural network,” *IEEE Trans. Microwave Theory Tech.*, Vol. 45, 1630–1633, 1997.
 25. Sirakawa, K., M. Shimiz, N. Okubo, and Y. Daido, “Structural determination of multilayered large signal neural-network HEMT model,” *IEEE Trans. Microwave Theory Tech.*, Vol. 46, 1367–1375, 1998.
 26. Yoon, J., H. Seo, I. Choi, and B. Kim, “Wideband LNA using a negative GM cell for improvement of linearity and noise figure,” *Journal of Electromagnetic Waves and Applications*, Vol. 24, Nos. 5–6, 619–630, 2010.
 27. Lee, M.-W. and S.-H. Kam, “A highly efficient three-stage doherty power amplifier with flat gain for WCDMA applications,” *Journal of Electromagnetic Waves and Applications*, Vol. 24, Nos. 17–18, 2537–2545, 2010.
 28. Shi, X., K. S. Yeo, W. M. Lim, M. A. Do, and C. C. Boon, “A spice compatible model of on-wafer coupled interconnects for CMOS RFICS,” *Progress In Electromagnetics Research*, Vol. 102, 287–299, 2010.
 29. Sacha, G. M., F. B. Rodriguez, E. Serrano, and P. Varona, “Generalized image charge method to calculate electrostatic magnitudes at the nanoscale powered by artificial neural networks,” *Journal of Electromagnetic Waves and Applications*, Vol. 24, Nos. 8–9, 1145–1155, 2010.