Progress In Electromagnetics Research C, Vol. 27, 1–13, 2012

DESIGN AND INTEGRATION OF COMPACT K-BAND BALUNS USING IMPEDANCE TUNING APPROACH

T. Zhang* **and V. Subramanian**

Microwave Engineering Laboratory, Berlin Institute of Technology, Berlin, Germany

Abstract—Compact K-Band CMOS baluns are designed, fabricated and characterized in a 130 nm CMOS technology. These baluns include a tunable active balun, a L-C lumped element balun, and two asymmetric planar transformer baluns. The detailed design processes are presented, including the topology selection, the transistor, inductor and transformer sizing, and the layout considerations. These topologies are compared in various aspects such as insertion loss, phase and amplitude imbalance, bandwidth, chip area, power consumption, and the difficulty to design and integration. An impedance tuning approach is implemented to chose the proper balun topology and to simply the balun integration. The baluns are on-wafer characterized and the measurement results compare the state-of-the-art realizations.

1. INTRODUCTION

The balun is an important component in RF and microwave circuits and is implemented in many circuits such as balanced mixers [1–3], frequency dividers [4, 5] and differential amplifiers [6, 7]. In hybrid circuits passive baluns are commonly used [8–11], while in RFIC and MMIC designs both active baluns and passive baluns are widely implemented. For ICs work below 4 GHz, since the passive baluns are too bulky to realize on chip, usually active baluns are implemented [12–14]. For ICs work above 4 GHz, compared with active baluns [15, 16], passive baluns are more intensively studied, such as lumped-element baluns [17], transformer baluns [18–20] and Marchand-type baluns [21–24].

Since there are a lot of choices for baluns operating at higher frequencies, the selection of the proper balun topology for integration

Received 2 December 2011, Accepted 18 January 2012, Scheduled 23 January 2012

* Corresponding author: Tao Zhang (tzhang@mwt.ee.tu-berlin.de).

becomes complex. This paper focuses on the design and integration of K-band CMOS baluns, while different topologies are analyzed and compared with each other. The design processes of an active balun, a lumped-element balun and transformer baluns are presented. Various figures of merit are compared, such as insertion loss, phase imbalance, amplitude imbalance, bandwidth, and chip area. Based on the analysis, the case-dependent optimum topology for specific applications is discussed.

The balun integration is also a popular topic. Usually the load impedance of the balun is not at $50\,\Omega$, such as for mixer integration where the balun load is capacitive [1–3]. Therefore, re-design of the balun is required. In this paper an impedance tuning approach is proposed to simplify the integration process. The insertion loss (IL), amplitude imbalance (ΔA) and phase imbalance ($\Delta\phi$) of the baluns are simulated while the load impedance is tuned at a particular frequency and the performance contours are plotted on the smith chart. Based on the results the proper balun topology could be chosen, while the re-design and integration process could be simplified.

This paper is organized as below. The design aspects of the baluns of various topologies will be discussed in Section 2. Section 3 discusses the impedance tuning approach and its application in balun integration. The measurement results and discussions are presented in Section 4. Section 5 concludes the article.

2. BALUN DESIGN AND COMPARISON

2.1. Active Balun

Among the various topologies of active baluns [12–14], the commonly used topology is the differential amplifier topology. As shown in Figure 1(a), a conventional differential amplifier can be used as an active balun. The RF input is the gate of M1, while the gate of M2 is connected to the RF ground. The common source transistor M1 produces 180 degree phase shift and the common gate transistor M2 does not produce any phase shift. This topology suffers from several problems when frequency goes higher. Firstly, the 180 degree phase shift of M1 and 0 degree phase shift of M2 becomes inaccurate. Secondly, M1 and M2 can not produce the same gain. When the current density is equal, the common source transistor has much higher gain than common gate transistor. Therefore, the active balun suffers from both phase imbalance and amplitude imbalance.

In order to overcome these problems, the active balun is re-designed and the schematic is shown in Figure 1(b). A cross coupled transistor pair is added between the transistor drains and balun

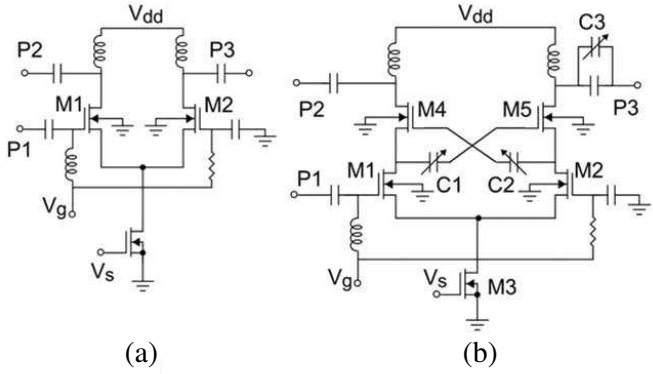

Figure 1. Schematics of (a) a conventional active balun; (b) the proposed active balun.

outputs. Varactor pairs C1 and C2 are inserted between the gate and source of the cross coupled transistors to control the power split ratio. By tuning the varactor capacitance, the coupling between the two branches varies. Therefore, the RF power can be re-distributed between the two branches, and the power imbalance is tunable. In order to tune the phase imbalance, a varactor pair C3 is shunted with the series capacitor used in the output matching network of one branch. To maintain low insertion loss, C3 capacitance is much less than the series MIM capacitor. Tuning the varactor C3 results a phase change.

The transistor sizes are optimized for gain and NF. The current source transistor M3 is designed with $8 \times 12.5\,\mu$m transistor width and $1\,\mu$m transistor length. The voltage drop acorss the current source is minimized to around 0.1 V. The M1 and M2 transistor size is $16 \times 4\,\mu$m, while the M4 and M5 transistor size is $16 \times 6.25\,\mu$m. The length of these transistors are minimized to 130 nm.

Figure 2 shows the simulated amplitude and phase imbalance versus C1 and C3 capacitance. The simulation frequency is 24 GHz. The default capacitances of C1 $\sim$ C3 are 0.1 pF, 0.3 pF, 0.06 pF, respectively. The Q-factors of the varactors are set to 5. It can be seen that C3 has a large influence on $\Delta\phi$ and C1 has a large influence on ΔA. By changing the biasing voltage of the varactors, ΔA varies by ± 2 dB and $\Delta\phi$ varies by ± 10 degree.

2.2. Lumped-element Balun

The lattice-type L-C balun shown in Figure 3 consists of two capacitors and inductors. When the inductor and capacitor values are carefully

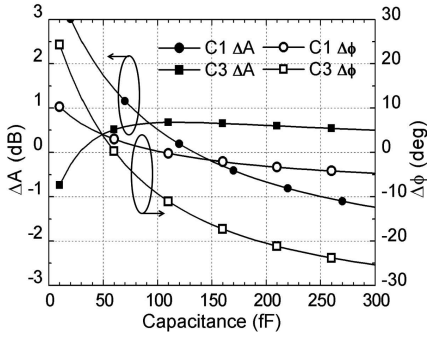

Figure 2. Amplitude and phase imbalance versus C1 and C3 capacitance.

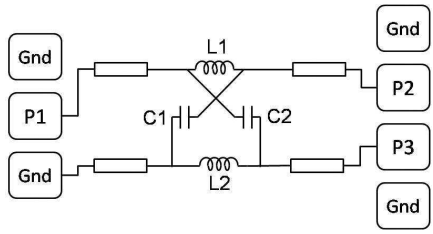

Figure 3. Layout of the transformer baluns.

chosen, the circuit produces ±90 degree phase shift for both branches which results in balanced outputs. The inductance and capacitance are set to $L = Z_c/\omega$ and $C = 1/(Z_c\omega)$, where ω is the angular velocity of the design frequency and Z_c is the geometric mean of the source and load impedance. The inductance is 0.35 nH and the capacitance is set to 0.1 pF.

Patterned ground shielded inductors are selected to minimize the substrate coupling. In order to maximize the Q-factor, symmetrical inductors are selected, which use both RF metal layers as spiral metals. As discussed above, the inductor outer dimension is set to 120 μm. The metal width is minimized to 5 μm. The transmission lines with grounded side shielding are chosen as interconnects.

2.3. Transformer Balun

In order to select a proper topology for transformer balun, stacked transformer balun topologies are compared with the planar transformer topologies. The utilized process has two RF thick metal layers on the top. The stacked transformer use both RF layers and the planar transformer use the bottom one which allows smaller metal-to-metal distance. A stacked transformer and a planar transformer, both with one turn for each winding, metal width of 5 μm and outer dimension of 100 μm, are designed and simulated in ASITIC [25]. The simulated coupling (K-) factor is 0.5 for the stacked transformer and 0.6 for the planar transformer at 24 GHz. The difference of K-factor is due to the process restrictions on the spacing of the metal windings; the minimum distance between the two windings of the stacked balun is

4 μm, while for the planar balun is only 2 μm. Because the planar transformer balun has larger K-factor than the stacked transformer balun under constant Q-factor of the windings in both the cases, it can be mentioned that the planar balun has smaller IL. EM simulation using ADS Momentum shows that the planar balun has 0.15 dB higher gain than the stacked balun at 24 GHz.

In order to design the planar transformer baluns, the outer dimension and number of turns should be optimized first. The peak Q frequency of the windings should be at K-Band. Figure 4 shows the peak Q frequency of the inductors versus the outer dimension and number of turns. The inductors are rectangular planar inductors with 5 μm metal width. If the inductor outer dimension is between 100 μm and 120 μm, and the number of turns is between 1 and 2, the

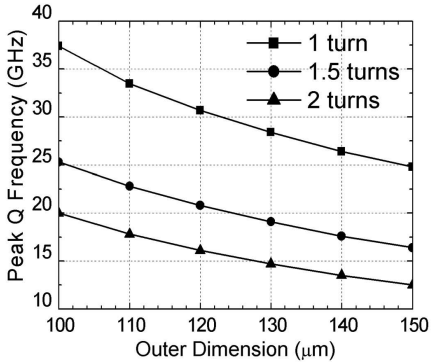

Figure 4. Inductor peak Q frequency versus the outer dimension and number of turns.

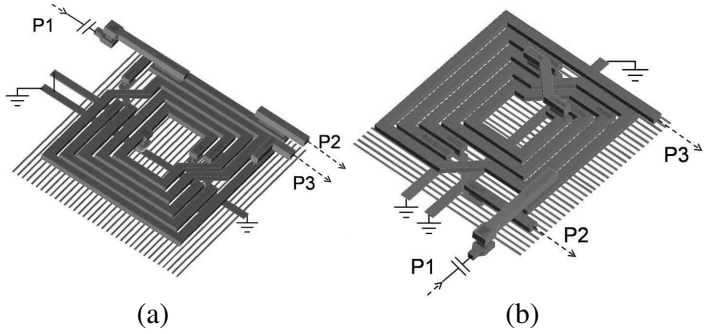

Figure 5. Layout of the transformer baluns.

peak frequency is near K-Band. The number of turns in the primary winding is selected as 2, while in the secondary winding is 1.5. The outer dimension of the balun is 100 μm.

The layout of the two transformer baluns is shown in Figure 5. These two baluns is designed differently to integrate with different circuits. The patterned bottom metal acts as ground shielding. The implementation of patterned ground avoids the eddy current loss in the substrate and ensures high Q-factor of the windings. The input port P1 is matched to 50 Ω at 24 GHz by adding a 0.1 pF series capacitor. The balun outer dimension is slightly modified to tune the winding inductance and improve the input matching. The output ports are not connected with capacitors since by simulation a series capacitor increases the IL. The return loss of P2 and P3 are −5 dB with 50 Ω load impedance at 24 GHz.

The transformer topology ensures the phase balance [18], but the amplitude balance is still a problem. To solve this problem, the position of the center-tap on the secondary winding is moved along the winding. By moving the center-tap position, the coupling of the primary winding with one branch of the secondary winding increases, while the coupling with the other branch decreases and hence the amplitude imbalance could be compensated. It should be notice that the phase imbalance also slightly alters.

2.4. Topology Comparison

Table 1 compares the performances of the three balun topologies. The advantages and disadvantages of all topologies are illustrated in this table. The active balun is good for their gain and wide bandwidth, but suffers from chip size and linearity. The lumped-element balun is good for their low loss and easy to design, the disadvantage is their narrow bandwidth. Although the lumped-element balun might be improved to overcome the narrow bandwidth, the chip size also becomes larger since more inductors will be implemented. The transformer baluns is the best choice for most cases for the wide bandwidth, small chip size and simplicity to integration.

Table 1. Comparison of the balun topologies at K-band.

Topology	IL	B.W.	Chip Size	Design	Integration
Active	With Gain	Wide	Large	Normal	Normal
L-C	Low	Narrow	Large	Easy	Normal
Transformer	Medium	Wide	Small	Normal	Easy

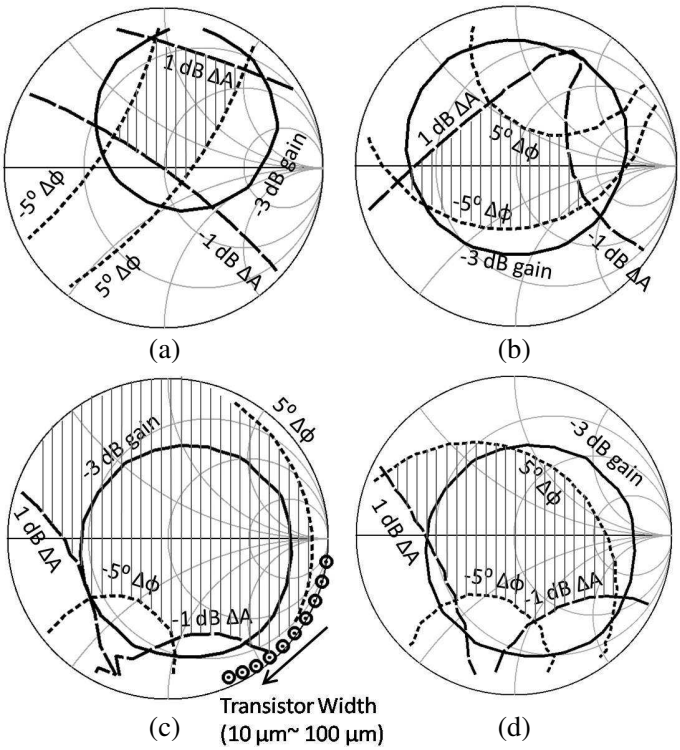

Figure 6. Load impedance tuning for (a) active balun; (b) L-C balun; (c) transformer balun T1; (d) transformer balun T2.

3. IMPEDANCE TUNING APPROACH

To simply the balun integration, an impedance tuning approach is proposed. The load reflection coefficient is swept (for both real and imaginary parts), with reference impedance 50 Ω for the designed passive baluns. The design frequency is 24 GHz and the source impedance is 50 Ω. The IL, ΔA and $\Delta\phi$ are calculated and the contours are plotted in smith charts shown in Figure 6. The solid line circle is the −3 dB gain (3 dB from maximum gain value) circle. The shadowed area is the impedance range where the baluns have less than 1 dB ΔA and less than 5 degree $\Delta\phi$. The transformer balun T1 are better choice for integration since its performance is more robust to impedance variation.

When the balun is integrated with a common source transistor circuit, normally the loads of the balun are the gates of transistors

and the load impedance is capacitive. As a test case for integrate, the transformer baluns are simulated with RF nMOS transistors. The width of RF nMOS transistor is swept from 10 µm to 100 µm and the corresponding load impedance variations are depicted in Figures 6(c) and 7(a). The length of the nMOS is 130 nm and the number of fingers is 10. From Figure 6(c), it can be seen that the transformer balun

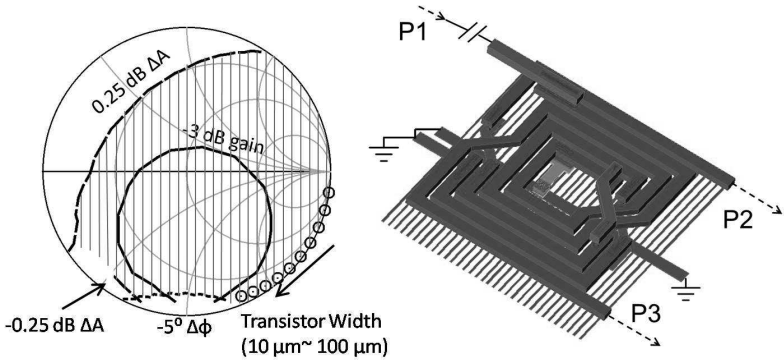

Figure 7. (a) Load impedance tuning for the modified transformer balun; and (b) layout of the modified balun.

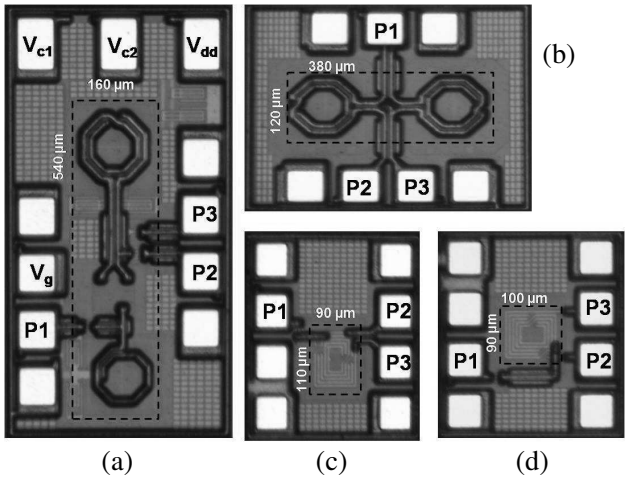

Figure 8. Chip micrograph of (a) active balun; (b) lumped-element balun; (c) transformer balun T1; (d) transformer balun T2.

does not provide enough phase balancing for these impedances. By reducing the balun outer dimension and moving the center tap of the secondary winding, the matching and the amplitude/phase balance performance of the balun are optimized. The simulated results from the load impedance tuning of the modified balun are shown in Figure 7(a), and the layout is shown in Figure 7(b). The $+5°\Delta\phi$ curve is not shown since it is outside the smith chart. From Figure 7(a), it can be mentioned that the modified balun can provide better phase and

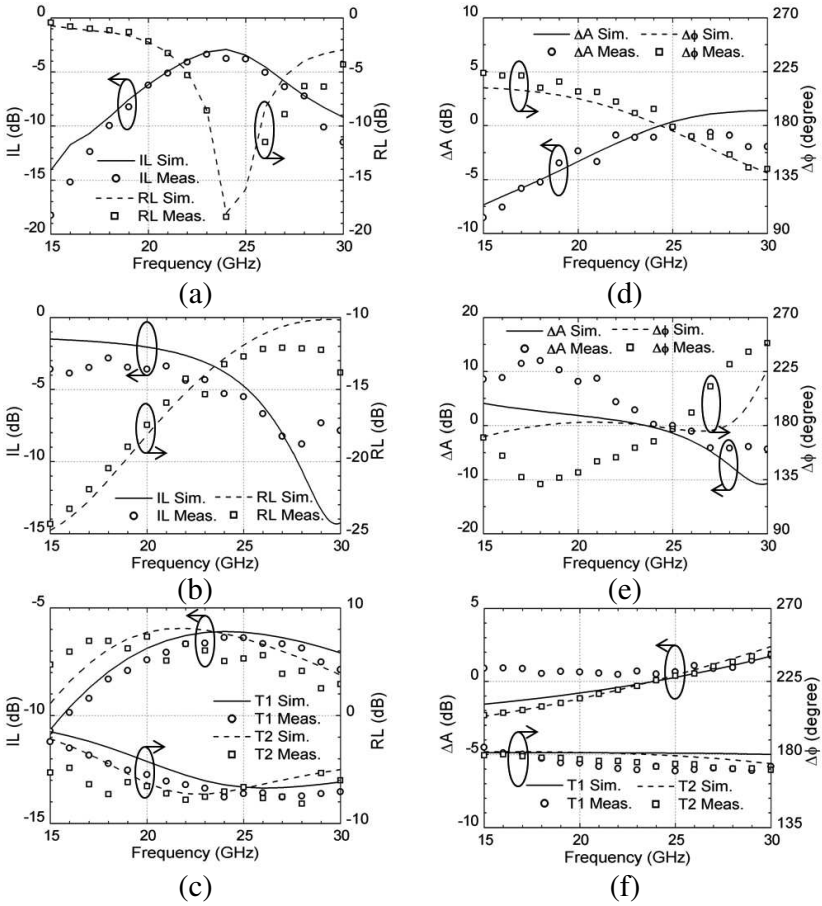

Figure 9. IL and RL of (a) the active balun; (b) the L-C balun; (c) the transformer baluns. ΔA and $\Delta\phi$ of the (d) the active balun; (e) the L-C balun; (f) the transformer baluns.

amplitude balancing for the transistors of different sizes and hence quite suitable for integration in various circuits. The modified balun is integrated with an 8 : 1 static divider as presented in [26].

4. MEASUREMENT AND DISCUSSION

The baluns are designed and fabricated in 130 nm CMOS process. The chip micrographs and the chip area of the core parts are shown in Figure 8. The measurement setup utilized a calibrated vector network analyzer. For each balun, the S-parameters of both branches are measured independently whiles the other port is 50 Ω terminated. Then the measured result is compared with the simulated result. The IL (S_{21}) and RL (Return Loss, S_{11}) results of the baluns, together with ΔA and $\Delta\phi$ are shown in Figure 9. S_{31} is not depicted here since it equals to S_{21} corrected with ΔA and $\Delta\phi$. It can be seen that the measured results match the simulation well, except for the ΔA and $\Delta\phi$ of the L-C balun. As mentioned before, this discrepancy is due to the sensitiveness of the L-C balun to the load impedance variation. A slight variation of the load impedance changes the balancing of the L-C balun.

The active balun T1 achieves a 5 GHz bandwidth from 21 to 26 GHz with $\pm$1 dB ΔA and $\pm$10 degree $\Delta\phi$ and an IL of 5 dB. The transformer balun T1 achieves a 10 GHz bandwidth from 18 to 28 GHz with $\pm$1 dB ΔA and $\pm$10 degree $\Delta\phi$ and an IL of 6 $\sim$ 8 dB. The L-C balun achieves an IL of less than 6 dB and a 2 GHz bandwidth of from 24 to 26 GHz with $\pm$1 dB ΔA and $\pm$10 degree $\Delta\phi$. Table 2 summarized the balun performances. The measured performance of the transformer balun compares state-of-the-art realizations and the ultra-compact size make it very suitable for integration at this frequency band.

Table 2. Summary of balun performances.

	CMOS Process	Freq (GHz)	IL (dB)	ΔA (dB)/ $\Delta\phi$ (degree)	Chip Area (mm^2)
[22]	180 nm	15–40	-9	2/10	0.06
[27]	180 nm	19–32	-7	1/5	0.073
Active	130 nm	21–26	-5	1/10	0.086
L-C	130 nm	24–26	-6	1/10	0.053
Transformer	130 nm	18–28	-8	1/10	0.01

5. CONCLUSION

Three balun topologies, active balun, lumped element balun and transformer balun are compared for CMOS K-Band applications. It is found that the active balun is a suitable choice when the balun requires a high gain, while the transformer balun is the right choice when the balun needs to be broadband and miniature. The impedance tuning method is implemented to characterize the balun performance and to simplify the integration. The measurement results show that designed balun compares with the state of the art realizations in K-Band.

ACKNOWLEDGMENT

This work is part of the LOWILO project (BMBF Project No. 16SV3654). The authors wish to acknowledge BMBF for sponsoring and other project partners for their support.

REFERENCES

1. Rao, P. Z., T. Y. Chang, C. P. Liang, and S. J. Chung, "An ultra-wideband high-linearity CMOS mixer with new wideband active baluns," *IEEE Microw. Theory Tech.*, Vol. 57, No. 9, 2184–2192, 2009.
2. Wei, C. C., H. C. Chiu, H. C. Hsu, W. S. Feng, and J. S. Fu, "Fully integrated 24 GHz differential active sub-harmonic mixer located in CMOS multi-layer Marchand baluns," *IET Microw. Antenna Prop.*, Vol. 4, No. 11, 1789–1798, 2010.
3. Jeong, J. C., I. B. Yom, and K. W. Yeom, "An active IF balun for a doubly balanced resistive mixer," *IEEE Microw. Wirel. Compon. Lett.*, Vol. 19, No. 4, 224–226, 2009.
4. Trotta, S., H. Li, V. P. Trivedi, and J. John, "A tunable flipflop-based frequency divider up to 113 GHz and a fully differential 77 GHz push-push VCO in SiGe BiCMOS technology," *IEEE RFIC Symposium 2009*, 47–50, 2009.
5. Chen, H. K., H. J. Chen, D. C. Chang, Y. Z. Juang, Y. C. Yang, and S. S. Lu, "A mm-wave CMOS multimode frequency divider," *IEEE ISSCC 2009*, 280–281, 2009.
6. Afsahi, A., A. Behzad, V. Magoon, and L. E. Larson, "Fully integrated dual-band power amplifiers with on-chip baluns in 65 nm CMOS for an 802.11n MIMO WLAN SoC," *IEEE RFIC Symposium 2009*, 365–368, 2009.

7. Kidwai, A. A., A. Nazimov, Y. Eilat, and O. Degani, "Fully integrated 23 dBm transmit chain with on-chip power amplifier and balun for 802.11a application in standard 45 nm CMOS process," *IEEE RFIC Symposium 2009*, 273–276, 2009.
8. Lin, C.-M., C.-C. Su, S.-H. Hung, and Y.-H. Wang, "A compact balun based on microstrip EBG cell and interdigital capacitor," *Progress In Electromagnetics Research Letters*, Vol. 12, 111–118, 2009.
9. Yeh, Z.-Y. and Y.-C. Chiang, "A miniature CPW balun constructed with length-reduced 3 dB couples and a short redundant transmission line," *Progress In Electromagnetics Research*, Vol. 117, 195–208, 2011.
10. Persico, R., N. Romano, and F. Soldovieri, "Design of a balun for a bow tie antenna in reconfigurable ground penetrating radar systems," *Progress In Electromagnetics Research C*, Vol. 18, 123–135, 2011.
11. Shao, J., H. C. Zhang, C. Chen, S. Tan, and K. J. Chen, "A compact dual-band coupled-line balun with tapped open-ended stubs," *Progress In Electromagnetics Research C*, Vol. 22, 109–122, 2011.
12. Ji, Y., C. Wang, J. Liu, and H. Liao, "1.8 dB NF 3.6 mW CMOS active balun low noise amplifier for GPS," *Electronics Letters*, Vol. 46, No. 3, 251–252, 2010.
13. Mastantuono, D. and D. Manstretta, "A low-noise active balun with IM2 cancellation for multiband portable DVB-H receivers," *IEEE ISSCC 2009*, 216–217, 2009.
14. Godara, B. and A. Fabre, "A highly compact active wideband balun with impedance transformation in SiGe BiCMOS," *IEEE Microw. Theory Tech.*, Vol. 56, No. 1, 22–30, 2008.
15. Jung, K., W. R. Eisenstadt, R. M. Fox, A. W. Ogden, and J. Yoon, "Broadband active balun using combined cascode-cascade configuration," *IEEE Microw. Theory Tech.*, Vol. 56, No. 8, 1790–1796, 2008.
16. Huang, B. J., B. J. Huang, K. Y. Lin, and H. Wang, "A 2–40 GHz active balun using 0.13 µm CMOS process," *IEEE Microw. Wirel. Compon. Lett.*, Vol. 19, No. 3, 164–166, 2009.
17. Chiou, H. K., H. H. Lin, and C. Y. Chang, "Lumped-element compensated high/low-pass balun design for MMIC double-balanced mixer," *IEEE Microw. and Guided Wave Letters*, Vol. 7, No. 8, 248–250, 1997.

18. Long, J. R., "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, Vol. 35, No. 9, 1368–1382, 2000.
19. Hsu, H. M., J. S. Huang, S. Y. Chen, and S. H. Lai, "Design of an on-chip balun with a minimum amplitude imbalance using a symmetric stack layout," *IEEE Microw. Theory Tech.*, Vol. 58, No. 4, 814–819, 2010.
20. Chiou, H. K. and T. Y. Yang, "Low-loss and broadband asymmetric broadside-coupled balun for mixer design in 0.18 µm CMOS technology," *IEEE Microw. Theory Tech.*, Vol. 56, No. 4, 835–848, 2008.
21. Huang, C. H., C. H. Chen, and T. S. Horng, "Design of integrated planar Marchand balun using physical transformer model," *Asia Pacific Microw. Conf. 2009*, 1004–1007, 2009.
22. Chiang, M. J., H. S. Wu, and C. K. C. Tzuang, "A compact CMOS Marchand balun incorporating meandered multilayer edge-coupled transmission lines," *Microwave Symposium Digest 2009*, 125–128, 2009.
23. Yang, Z. Q., T. Yang, and Y. Liu, "Analysis and design of a reduced-size marchand balun," *Journal of Electromagnetic Waves and Applications*, Vol. 21, No. 9, 1169–1175, 2007.
24. Ercoli, M., M. Kraemer, D. Dragomirescu, and R. Plana, "An ultra small passive balun for 60 GHz applications in CMOS 65 nm technology," *NEWCAS Conference 2010*, 329–332, 2010.
25. Niknejad, A. M., "Modeling of passive elements with ASITIC," *Microwave Symposium Digest 2002*, 149–152, 2002.
26. Shu, R., V. Subramanian, and G. Boeck, "Millimeter-wave static frequency divider in 0.13-m CMOS technology," *NEWCAS Conference 2011*, 2011.
27. Yu, H. Y., S. S. Choi, S. H. Kim, and Y. H. Kim, "K-Band balun with slot pattern ground for wide operation using 0.18 µm CMOS technology," *Electronics Letters*, Vol. 43, No. 5, 51–52, 2007.