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MICROSTRIP PHASE INVERTER USING INTERDIGITAL STRIP LINES AND DEFECTED GROUND

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Abstract—A new wide-band microstrip phase inverter is reported in this paper. Interdigital striplines, defected ground and via holes are used to obtain 180° phase shift. The structure is simple and can be realized with ordinary microwave integrated circuit (MIC) fabrication process. The bandwidth is enhanced largely. A lumped-element model of the phase shifter is devised. The fabricated phase inverter has a bandwidth of 105.6% (2.065–6.682 GHz), with 1 dB insertion loss and a phase deviation less than 10°.

1. INTRODUCTION

A phase inverter (PI) is a device that changes the phase of a signal by 180°. It has been applied in many microwave components such as rat-race hybrids, balanced mixer, frequency discriminator, and feeding network of antenna arrays. The $\lambda/2$-transmission line (TL) is the simplest PI. It has a bandwidth of 13% and $180 \pm 10°$ phase shift [2]. The $\lambda/4$-coupled line section with diametrically opposing ends short-circuited can approximate a phase-reversing network referred to a $\lambda/2$-TL and has a bandwidth of 50% and $180 \pm 10°$ phase shift. But the line space is too narrow to fabricate with standard microstrip process [1]. The $\lambda/4$-microstrip (MS)-to-coplanar waveguide (CPW) broadside-coupled structure [2] has an identical property to that in [1]. The CPW and microstrip have identical linewidths for the ease of design. The high coupling level can be realized easily. A PI may also be obtained by means of reversing field orientations with reference to a particular ground plane. This mechanism can be easily realized

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with uniplanar techniques since all the conductors are located on the same side of the substrate. In recent years, efforts have been directed to the development of a broad-band PI. Some broad-band uniplanar phase inverters have been reported in [3–6, 8–10]. Coplanar waveguide (CPW) PI [3] has 3.1 : 1 bandwidth with 0.5 dB insertion loss and 140° phase shift. The PI consisting of micro-coplanar strip (MCS) and coplanar strip (CPS) structures [4] has 3.8 : 1 bandwidth with 1 dB insertion loss and 160° phase shift. CPW phase inverters with spiral-slot [6] has about 60% bandwidth with −10 dB return loss.

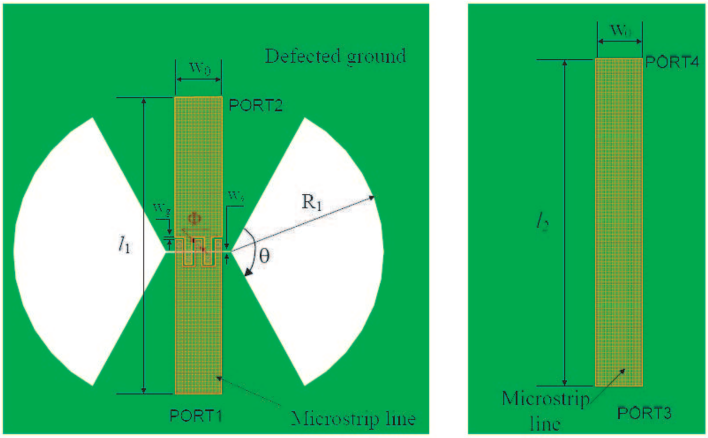
The ideal finite-ground-plane CPW (FCPW) PI [5] and interdigital CPS PI [8] need very narrow gap width and very thin bonding wires. Another ideal PI [7] is realized with multilayer substrates. A PI integrated on the microstrip hybrid requires a transition between the microstrip line and CPW [9] that requires complicated structures. The simple microstrip PI using a slotted ground [10] has 1.93 : 1 bandwidth with 1 dB insertion loss and 160° phase shift. The bandwidth and an easy-realized structure are the major problems in the PI design. This paper proposes a simple wide-band microstrip PI using interdigital strip and a defected ground.

2. MICROSTRIP PI AND ITS EQUIVALENT CIRCUIT

Figure 1(a) shows the geometry of the PI. The proposed microstrip PI consists of five via holes, which connect the interdigital microstrip lines to the ground, and a slot with radial short end in the ground. The via holes make the ground currents of port 1 flow into the microstrip line of port 2 or vice versa; the slot blocks the ground currents that flow between the two lines at the resonant frequency. The radial slot in the ground is the modified version of the conventional $\lambda_g/4$ short-stub structure and has the advantage of wider bandwidth. Compared with the microstrip PI using slotted ground [10], the interdigital microstrip lines are applied in the proposed structure, and the slot line in the middle part is avoided. Moreover, the radial slot is applied other than long linear slot line.

The diameter of the via hole is 0.3 mm. Both the slot and gap widths are 0.2 mm. The PI is mounted on a dielectric substrate that has a dielectric constant ε_r of 2.2 and thickness t of 1 mm. The dimensions are shown in Fig. 1. The radial slot resonates at 2.78 GHz.

The equivalent circuit model of the PI (Fig. 2) is constructed using series inductors L, L_2, L_3 and parallel resonant circuits L_1 and C_1. The series inductors are introduced through the vertical via holes to represent the signal delays. L represents inductor of the back feed pin of the coaxial line. L_2 represents the three via holes from port 1 to



(a) (b)

Figure 1. Geometry of the microstrip PI (a) and the microstrip transmission line. (b) For substrate: $h = 1\,\text{mm}$, $\varepsilon_r = 2.2$. Other dimension: $w = 3.1\,\text{mm}$, $w_s = w_g = 0.2\,\text{mm}$, $R_1 = 10.45\,\text{mm}$, $\theta = 120°$, $\Phi = 0.3\,\text{mm}$, $l_1 = 20\,\text{mm}$, $l_2 = 22\,\text{mm}$.

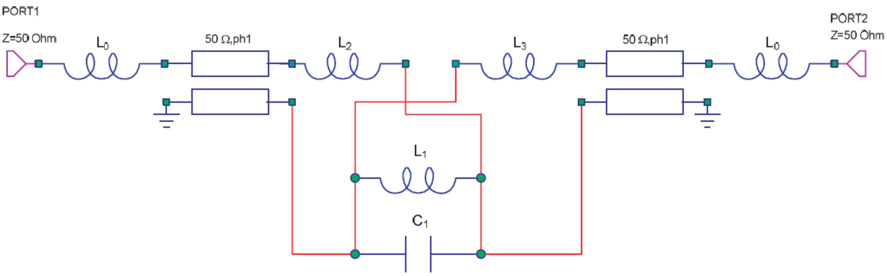


Figure 2. Equivalent circuit model of microstrip PI: $L_0 = 0.1692\,\text{pH}$ $L_1 = 11.7329\,\text{nH}$, $C_1 = 0.2599\,\text{pF}$, $L_2 = L_3 = 0.1558\,\text{nH}$, $ph1 = 56.36°$.

the ground while L_3 represents the two via holes from port 2 to the ground. The parallel resonant circuit is used to model the radial slot resonance. The values of the lumped components are extracted from the EM simulated results. As to the dimensions shown in Fig. 1(a), the values of the lumped elements are shown in Fig. 2.

The PI is back fed and simulated with Ansoft ensemble 8.0. As shown in Fig. 3, the simulation and equivalent circuit results are consistent, in terms of S-parameters, phase differences and insertion losses. The difference between the insertion losses in Fig. 3(a) is caused

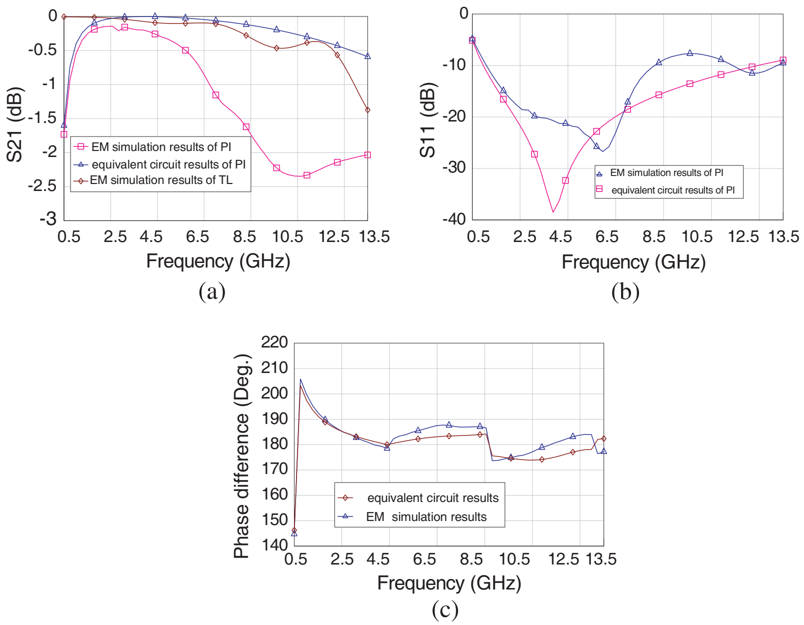


Figure 3. Comparison of the S-parameters and the phase difference between equivalent circuit model and EM model of the PI.

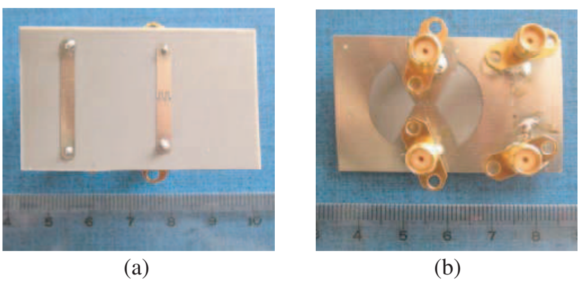


Figure 4. Photograph of the proposed PI and the transmission line (a) top face and (b) bottom face.

by losses due to slot radiation and resonant currents on the ground. The insertion loss is defined by subtracting the S_{21} (dB) of the PI from the S_{21} (dB) of the TL (transmission line as shown in Fig. 1(b)). The phase difference is defined by subtracting the phase of PI from the phase of TL with length l_3. The length of the transmission line in Fig. 1(b) is longer than the length of the PI in Fig. 1(a) by 2 mm to compensate the signal delays caused by the via holes. Simulation

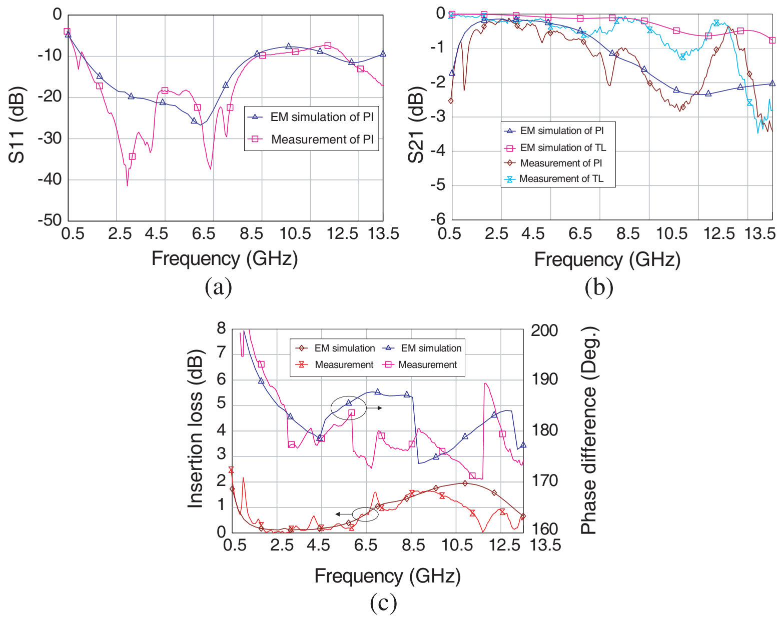


Figure 5. S_{11}, S_{21}, insertion loss and phase difference of the fabricated PI.

results show that the PI has a bandwidth of 118.4% (1.772–6.916 GHz, 3.9 : 1), 1 dB insertion loss and a phase deviation less than 10°.

3. PERFORMANCES OF MICROSTRIP PI

The proposed microstrip PI and microstrip transmission line are fabricated as shown in Fig. 4. The measurements are performed by using an HP8719E vector network analyzer. There seems to be good agreement between the measured and simulated results as shown in Fig. 5. Also the insertion loss is defined by subtracting the S_{21} of the PI from the S_{21} of the TL. The measured results show that the proposed microstrip PI has a bandwidth of 105.6% (2.065–6.682 GHz, 3.2 : 1), 1 dB insertion loss and a phase deviation less than 10°. Moreover, the bandwidth of phase deviation less than 10° can be extended largely without regard for the insertion loss. The insertion loss limits the bandwidth of the PI. Through decreasing the slot radiation loss, the bandwidth can be extended more over.

Table 1 gives the performance comparisons of published PI and the proposed PI. The proposed PI shows the advantages in both bandwidth and simple structure.

Table 1. Performance comparisons of published PI and the proposed PI.

ref	PI technique	Bandwidth	Insertion loss	Phase difference	Fabrication process
	$\lambda/2$-TL	13%		$180 \pm 10^\circ$	Single-layered PCB
[1]	$\lambda/4$-coupled line	50%		$180 \pm 10^\circ$	Single-layered PCB with via holes, line space is too narrow
[2]	$\lambda/4$-MS-to-CPW broadside-couple	50%		$180 \pm 10^\circ$	Double-layered PCB with via holes
[3]	CPW PI	103%	0.5 dB	$180 \pm 40^\circ$	Single-layered PCB with bonding wires
[4]	MCS-CPS PI	117%	1	$180 \pm 20^\circ$	Single-layered PCB with bonding wires
[6]	CPW-spiral slot PI	60%			Air bridge
[7]	Multi-layered substrates	185%	1.1 dB	$180 \pm 10^\circ$	Multi-layered substrates
[9]	MS-CPW	120%		$180 \pm 25^\circ$	Double-layered PCB with via holes
[10]	MS-slot	63.5%	1 dB	$180 \pm 20^\circ$	Double-layered PCB with via holes
This work	interdigital MS line with defected ground, via holes	105.6%	1 dB	$180 \pm 10^\circ$	Double-layered PCB with via holes

4. CONCLUSION

A new wide-band microstrip PI using interdigital striplines, defected ground and via holes has been proposed. The PI has more than 3.2 : 1 bandwidth centered at 4.3735 GHz with better than 1 dB insertion loss and 10° phase shift. The structure is simple and can be realized with ordinary microwave integrated circuit(MIC) fabrication process. The proposed PI can be used in components such as rat-race hybrids, balanced mixer, frequency discriminator, and feeding network of antenna arrays. The slot radiation loss limits the bandwidth of the PI in high part. By decreasing the slot radiation loss [11], the bandwidth can be further extended.

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