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A 20–31 GHz HIGH IMAGE REJECTION RATIO SUB-HARMONIC MIXER

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Abstract—A broadband monolithic image rejection subharmonic mixer using a standard 0.18 μm CMOS technology is proposed. This circuit is composed of a band-pass filter with an intermediate frequency (IF) extraction function that can simplify the block diagram of the image rejection mixer. The entire passive circuit is constructed using a broadside coupling structure to achieve a high level of integration. Based on measured results, the proposed mixer exhibits conversion loss of 15.5–18.5 dB at a local oscillator (LO) power of 13 dBm, whereas the 3 dB bandwidth ranges from 20 to 31 GHz (43.1%) with a miniature chip dimension of $0.77 \times 0.81\,\text{mm}^2$. The LO-to-radio frequency (RF), 2LO-to-RF, and RF-to-IF isolation levels are higher than 22.5, 42.9, and 34.5 dB, respectively. The best image rejection ratio of 29 dBc with 20° phase compensation at 24.5 GHz can be achieved.

1. INTRODUCTION

Recently, the demand for high-volume, low-cost, and high-performance monolithic millimeter-wave integrated circuits has significantly increased. An important component of these systems is the mixer that converts signals from one frequency to another. However, the resonator quality of the oscillator degrades as operating frequency increases, resulting in increased phase noise and diminished output power. The balanced mixers have inherent port-to-port isolation and even-order

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mixing product suppression. However, due to the LO not reliable in high frequency, it wasn't suitable in millimeter-wave range applications [1, 2]. The frequency multipliers or subharmonic mixers are promising tools that allow for the use of LO signals at a relatively low frequency, making LO sources more reliable and less expensive [3].

Previously, many methods have been developed to filter the image signals. Image rejection mixer (IRM) is one of the most common methods to avoid noise interference from image frequencies in receiver systems. The anti-parallel diode pair (APDP) topology has been commonly used for diode mixers, particularly subharmonically pumped mixer [4]. However, compared with other types of diode mixers, the APDP topology of the subharmonically pumped mixer occupies a large chip dimension. A 1.9 GHz receiver front end integrated well with an active image-reject filter has been proposed [5]. Tunable image-reject filters reduce chip dimensions and provide an image frequency tuning function. However, active image-reject filters incorporate additional DC bias to accommodate extra DC consumption. Besides, passive notch filters are extensively applied to image reject mixer design [6]. Due to its high channel selectivity, the prototype typically suffered from a narrow operating bandwidth. The active dual-band IRM using 0.18 m CMOS technology is demonstrated to achieve high level integration and high conversion gain performances [7, 8]. However, these active IRM has poor 1 dB compression power point, narrow bandwidth and additional power consumption.

In order to improve the broadband performance, Hartley architecture provides a more convenient solution for IRM design. Accordingly, a number of Hartley-type IRMs have been proposed to suppress image signal [9–13]. Chiou et al. [10] divided and fed LO signals into two subharmonic mixers and RF signals through a 90° hybrid system to generate 0° and 90° signals and then connected the IF I/Q signals to the off-chip mixer for image rejection. However, the IF and RF matching circuits still occupy a large chip area. Although the operating bandwidth of IRM is extended substantially, the large chip dimension cannot be neglected yet. Furthermore, Hartley architecture is rather sensitive to I/Q mismatches subsequently on the degradation of image rejection ratio (IRR). The IRM utilizing a new RF dual balun to provide balanced RF signals and simultaneously simplified IF extraction to enhance RF/LO-to-IF isolation levels without additional IF filters was proposed [14]. However, they used the off-chip component of the IF quadrature hybrid to connect the IF I/Q ports, which lowered the integration level.

As mentioned, it is essential to design a broadband, compact and high-performance IRM without DC consumption. In this work, to

reduce the chip size and improve RF-to-IF isolation further without any other IF filters, a band-pass filter with the IF extraction function which can simplify the block diagram of image rejection mixer is proposed. A band-pass filter with an IF extraction function that can simplify the block diagram of IRMs is herein used to reduce chip size and further improve RF-to-IF isolation without any IF filters. Furthermore, the broad side coupling structure to achieve high-level integration is used to further reduce the chip size. In addition, an IF phase calibration is used to compensate I/Q mismatches. Subsequently, a good image rejection ratio (IRR) can be achieved.

2. CIRCUIT DESIGN

Figure 1(a) shows the block diagram of the proposed SHIRM, consisting of LO power divider, band-pass filter with an IF extraction function, and transistors. A broadside Marchand dual balun is used between the LO input and MOSFET to generate the balanced signals and fed into the gates of the transistors. In addition to power division,

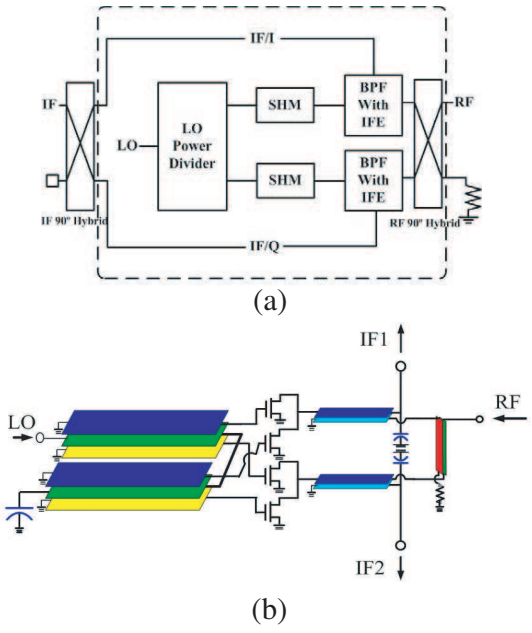

Figure 1. (a) Block diagram of the proposed SHIRM. (b) The designed broadside coupling circuit using the band-pass filter with IF extraction function.

the LO signals can be cancelled at the transistor drain. This can greatly enhance the LO-to-RF/IF isolation The use of broadside coupling structures makes the design more flexible. The corresponding designed circuit using the band-pass filter with broadband IF extraction is shown in Fig. 1(b). The bandpass filter with IF extraction function between the transistors and the IF/RF ports offers impedance matching among the three ports. In addition to achieving isolation of the IF and RF ports, it also provides the transistors with the RF/IF signals

The bandpass filter with IF extraction function is mainly formed by a $\lambda/4$ microstrip-line coupler. The overall passive circuit is constructed using broadside coupling to achieve a high level of integration. As IF extraction remains a key issue in subharmonic mixer design, the proposed LO dual extraction circuits to satisfy the requirements of broadband operation. The balun aims to provide balanced signals for mixing and combining IF compact rearrangement of the SHIRM will greatly reduce its layout complexity and chip dimension.

The proposed RF band-pass filter with IF extraction function is composed of a $\lambda/4$ coupler line and a low-pass filter (Fig. 2). The scattering matrix can be derived as follows:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{2}\left(1+\frac{-Y}{Y+2Y_0}\right) & \frac{\sqrt{2}Y_0}{Y+2Y_0} & \frac{j}{2}\left(1+\frac{Y}{Y+2Y_0}\right) \\ \frac{\sqrt{2}Y_0}{Y+2Y_0} & \frac{-Y}{Y+2Y_0} & \frac{-j\sqrt{2}Y_0}{Y+2Y_0} \\ \frac{j}{2}\left(1+\frac{Y}{Y+2Y_0}\right) & \frac{-j\sqrt{2}Y_0}{Y+2Y_0} & \frac{-1}{2}\left(1+\frac{-Y}{Y+2Y_0}\right) \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} \quad (1)$$

where $Y = j\omega C$ and $Y = 1/Z_o$ are the characteristic admittance parameters among three ports. As $C \to \infty$ and $Y \to \infty$, we have

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & j \\ 0 & -1 & 0 \\ j & 0 & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} \quad (2)$$

The coupling between S_{31} and S_{13} shows a 90° phase difference, that is, the low-frequency IF signal can directly transmit between port 1 and port 3 without any losses. RF signals can be fed into the transistors for subharmonic mixing. $S_{12} = S_{21} = 0$ indicates good RF-to-IF isolation between ports.

A major consideration is the enhancement of the isolation between RF and IF ports, which prevent RF signal leakage from the IF port and vice versa. For more efficient utilization of the chip area, a broadside coupling structure is proposed to reduce the size of the conventional planar edge-coupling structure without altering its performance. As a result of the external coupled-line structure of the dual balun and the IF extraction circuit in the RF band-pass filter, the isolation can

be enhanced and the chip dimension can be reduced, which would effectively reduce the chip area. A wide band (K- to Ka-band) can also be achieved.

3. MIXER IMPLEMENTATION AND RESULTS

Zeland IE3D software was used in the full-wave electromagnetic (EM) simulation to calculate the S-parameters of the passive circuits. An Agilent ADS corresponding to a TSMC Corporation design kit was used for circuit simulation. These individual components were combined in a harmonic balance simulator to optimize the performance of the mixer. In this work, the mixer was constructed using 0.18 µm CMOS technology. The gate drain that connected nMOS with f_T and $f_{\max}$ values higher than 60 and 55 GHz, respectively, was used as the diode. The 16-finger diode with a total gate width of 26 µm was optimized to ensure minimum conversion loss and ultimately

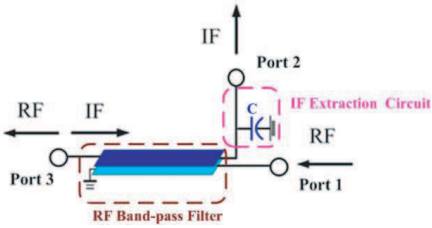

Figure 2. The proposed RF band-pass filter with IF extraction function.

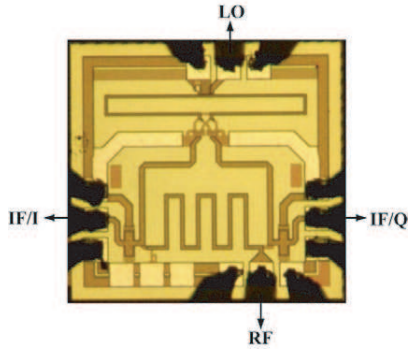

Figure 3. Microphotograph of the fabricated CMOS SHIRM. The overall chip dimension, including the contact pads, measures 0.81 × 0.77 mm^2.

achieve good impedance matching. Fig. 3 is a microphotograph of the fabricated CMOS SHIRM, with the chip dimension reduced to $0.81 \times 0.77\,\text{mm}^2$. The broadside Marchand dual balun dimension was $670 \times 70\,\mu\text{m}^2$. The line length and width of the proposed RF band-pass filter with IF extraction were 520 μm and 18.5 μm, respectively.

The measurement signals were provided by the coplanar ground-signal-ground (GSG) and ground-signal-ground-signal- ground (GSGSG) (100 μm pitch) on a wafer probe measurement system based on an Agilent E4446A spectrum analyzer, which was calibrated with an E44198 power meter. The losses of the probes and cables were measured separately and used to correct the results.

Figure 4 illustrates the measured and simulated conversion losses of the CMOS SHIRM as functions of RF at a fixed LO power of 13 dBm and an RF power of −10 dBm. The obtained conversion loss is 15.5–18.5 dB within an RF 3 dB bandwidth ranging from 20 to 31 GHz (43.1%). Due to the lossy substrate in silicon-based processes and the inaccuracy of EM estimation, the overall conversion loss increases by 3 dB at 25 GHz relative to the design goal. However, the trend of the measured curve agrees well with the simulation.

Figure 5 illustrates the measured and simulated conversion losses as functions of LO power with an RF power of −10 dBm, an RF of 23.5 GHz, and an IF of 0.5 GHz. A significant mixing effect of an LO drive level of 10 dBm can be seen. The best conversion loss is 15.5 dB at an LO power level of 14 dBm while 15.7 dB conversion loss for the 13 dBm. As discussed later, the power mismatch decreases

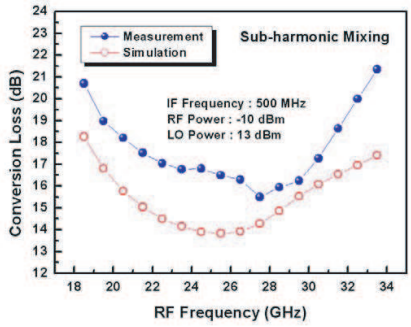

Figure 4. Measured and simulated conversion losses of the CMOS SHIRM as functions of RF at a fixed LO power of 13 dBm and an RF power of −10 dBm.

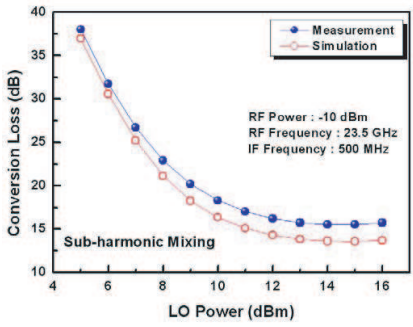

Figure 5. Measured and simulated conversion losses as functions of LO power.

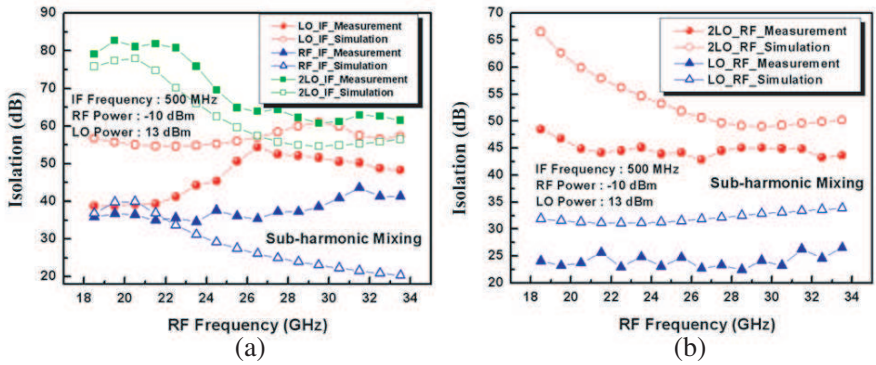

Figure 6. Measured and simulated 2LO-to-IF, LO-to-IF, RF-to-IF, 2LO-to-RF, and LO-to-RF isolation levels as functions of the RF.

with decreasing input power levels. Thus, 13 dBm LO power level, instead of 14 dBm, is used to achieve good conversion loss and lower power mismatch simultaneously. The measured and simulated 2LO-to-IF, LO-to-IF, RF-to-IF, 2LO-to-RF, and LO-to-RF isolation levels as functions of RF frequency for the down-converter mode are plotted in Fig. 6. All port-to-port isolation levels, except for that of the LO-to-IF isolation, which was between 39.3 and 54.4 dB, exceeded 22.5 dB over the RF bandwidth range of 20–31 GHz under the measured conditions shown in the inset of the figure. Hence, LO-to-RF RF-to-IF, 2LO-to-IF, and 2LO-to-RF isolation levels of 23–26 35–44, 61–85, and 43–47 dB, respectively, can be achieved Fig. 7 shows the measured and simulated conversion losses as functions of RF input power at an LO power of 13 dBm, an IF of 0.5 GHz, and RF of 23.5 and 29.5 GHz, respectively. A 1 dB compression power point of approximately 3–4 dB can be observed.

The IRR can be measured using the expression reported by Gunnarsson et al. [9]:

$$\mathrm{IRR} = \left[\frac{G_c + 2\sqrt{G_c}\left(\sqrt{G_c}+\varepsilon\right)\cos\theta + \left(\sqrt{G_c}+\varepsilon\right)^2}{G_c - 2\sqrt{G}\left(\sqrt{G_c}+\varepsilon\right)\cos\theta + \left(\sqrt{G_c}+\varepsilon\right)^2}\right] \tag{3}$$

where G_c is the conversion gain of the unitary IF output port, ε is the power mismatch of IF I/Q signals, and θ is the phase difference. The square term in the IRR equation significantly affects the power mismatch of IF I/Q signals. Fig. 8 shows the measured power mismatch of the fabricated SHIRM as a function of the upper side band (USB) RF at different LO power levels. The power mismatch decreases with decreasing input power levels.

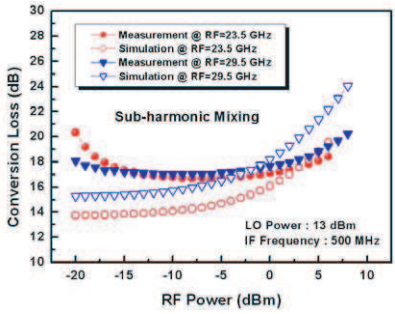

Figure 7. Measured and simulated conversion losses as functions of RF power.

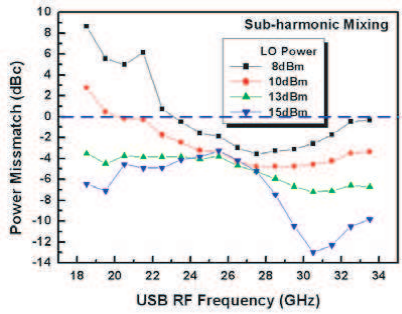

Figure 8. Measured conversion loss as a function of USB RF at different LO power levels.

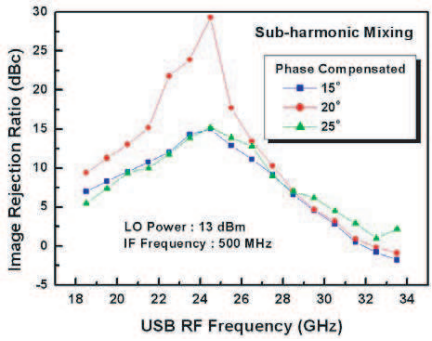

Figure 9. Measured IRR as a function of USB RF at different compensated phases.

Excellent image suppression requires accurate phase and amplitude balance in the overall SHIRM. Equation (3) describes the IRR in terms of phase θ, amplitude errors, and the conversion efficient of the mixer [7]. It is a reliable tool for calibrating phase and amplitude errors using high-speed ADCs, but it requires additional DC consumption. In the proposed CMOS SHIRM, a passive phase-delay transmission line using the branch-line coupler on the FR4 substrate suitably compensates for the phase error produced from the passive circuits. From the phase calibration measurement, a 20° phase compensation provides the highest level of image signal suppression.

The measured IRR as a function of the USB RF at different LO power levels, similar to the power mismatch, is enhanced by a decrease in LO power. The best IRR of 33 dBc at 24.5 GHz and an LO power of 8 dBm can be achieved.

Table 1. Performance comparison of the reported IRMs.

Ref..	Technology .	RF Bandwidth (GHz)	CL (dB)	Best IRR (dBc)	Isolation (dB)			P_{LO} (dBm)	Size (mm^2)
					LO–IF	LO–RF	RF–IF		
[7]	CMOS 180 nm	2.45 / 5.2	10.5 / 11*	36 / 45	N/A	N/A	N/A	N/A	1.2
[8]	CMOS 180 nm	2.4 / 5.2	9 / 8*	40 / 40	N/A	N/A	N/A	17	4
[9]	PHEMT 150 nm	55–65 (16.7%)	10.2	30	N/A	N/A	N/A	10	9.24
[10]	PHEMT 150 nm	40.5–43.5 (7.1%)	8.9–12	22	42–47	37–40	50–60	15.5	0.84
[14]	CMOS 180 nm	9–21 (80%)	19.4	34	26–47	>30	10–28	13	0.67
[15]	CMOS 180 nm	5.25	16*	50.6	N/A	N/A	N/A	7.4	3
[16]	CMOS 180 nm	5.25	14*	45	N/A	N/A	N/A	N/A	4
This work	CMOS 180 nm	20–31 (43.1%)	15.5–18.5	29	39–54	23–26	35–44	13	0.62

*conversion gain

Figure 9 shows the measured IRRs of the CMOS SHIRM as a function of the USB RF for the LO power of 13 dBm at different phase compensations. The best IRR for the phase compensated at 20° is 29 dBc at 24.5 GHz.

Table 1 summarizes the comparative results for the proposed structure with other reported IRMs [7–10, 14–16]. The proposed CMOS SHIRM presents some significant advantages over previously reported designs, including its operating bandwidth of 11 GHz across the K-band, IRR of 29 dB, and compact chip size.

4. CONCLUSION

A miniature broadband 20–31 GHz monolithic SHIRM using broadside coupling with a chip dimension of 0.62 mm^2 was designed and fabricated using 0.18 µm CMOS technology. The new band-pass filter simultaneously simplifies IF extraction to enhance RF/LO-to-IF isolations without additional IF filters and reduces the chip dimension. Based on measured results, the proposed architecture

has some significant advantages, such as wide RF bandwidth, good isolations, and the improved IRR of 29 dB, which are relatively suitable for millimeter-wave applications.

ACKNOWLEDGMENT

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