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A CIRCUIT MODEL FOR VERTICAL MULTILAYER TRANSITIONS IN COPLANAR WAVEGUIDE TECHNOLOGY

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Abstract—A circuit model for vertical transitions between different coplanar waveguide systems using via-holes is presented. The model is directly extracted from the geometry of the transition using closed expressions. Additionally, it can be used to find suitable initial dimensions for the transition in a circuit simulator, thereby greatly reducing the effort spent on subsequent electromagnetic simulations. To test the validity of the developed model, it is applied to a variety of situations involving a wide range of stack heights, dielectric constants, and transmission line geometry values. These situations cover most of the relevant broadband vertical transitions used in practical PCB and LTCC designs. Comparative analysis of the circuit model and electromagnetic simulations yields good agreement in all analyzed situations. Experimental assessment of the model is also provided for some of the transitions that were built and characterized in a back-to-back configuration.

1. INTRODUCTION

Multilayer technology is widely used in microwave design to reduce the final circuit size. The use of multiple layers requires high quality vertical transitions to interconnect the different components of the circuit. This is, for example, the case in buried broadband coupler designs where the vertical transitions are the final limiting factor of device performance [1]. Such interconnection can be realized with via-holes, [2, 3] or field coupled transitions [4]. Via-hole based vertical

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transitions are widely employed in multilayer technology, such as LTCC or PCB, because they provide a broad bandwidth from DC. Achieving a high performance over a broad bandwidth is often complicated and normally it requires an intensive effort of full-wave simulations for optimizing and obtaining the target behavior. Thus, in the design process, having a circuit model of the transition that could rapidly provide a good starting point, would be highly valuable as it would reduce the total number of iterations and computational effort in the subsequent full-wave simulations. However, establishing a general circuit model is not feasible due to the huge number of possible scenarios, so different circuit models are used for each particular situation.

Some examples of high performance, via-hole based vertical transitions in LTCC or PCB technology can be found in [6–9]. In [6] transitions were designed using electromagnetic (EM) simulations to optimize bandwidth, while in [7] a simple circuit model with distributed elements was developed to obtain an approximate initial design prior to developing a more exact design based on intensive electromagnetic simulations. In [8] a lumped component circuit model was presented to design a transition between coplanar transmission lines. Recently, the authors have designed a high performance transition in PCB technology [9]. In doing so, a circuit model combining lumped and distributed element was used with good results.

In the present work this model is further detailed and applied in a wider variety of scenarios. The objective of this model is not to compete with full wave EM simulations, but to provide a powerful tuning tool for finding a good set of initial values for the transition design. Thus an adequate tradeoff between complexity and accuracy must be achieved. As will be shown, this circuit model allows us to predict the transition behavior with a reasonable accuracy using only a circuit simulator. All model parameters are given by closed expressions.

Figure 1 shows an example of a type of vertical transitions analyzed here. In this case, the transition interconnects a Grounded Coplanar Waveguide (GCPW) and a Shielded Multilayer Coplanar Waveguide (SMCPW) line. A signal via-hole, passing through the ground planes by means of suitable irises, is used to interconnect the central conductors of the two coplanar waveguides in different layers. Shielding via-holes are also placed in the multilayer structure, forming a ring around the signal via-hole to avoid the presence of signal crosstalk between adjacent circuits and to eliminate parasitic substrate modes [5].

In the developed model, the vertical signal and grounding

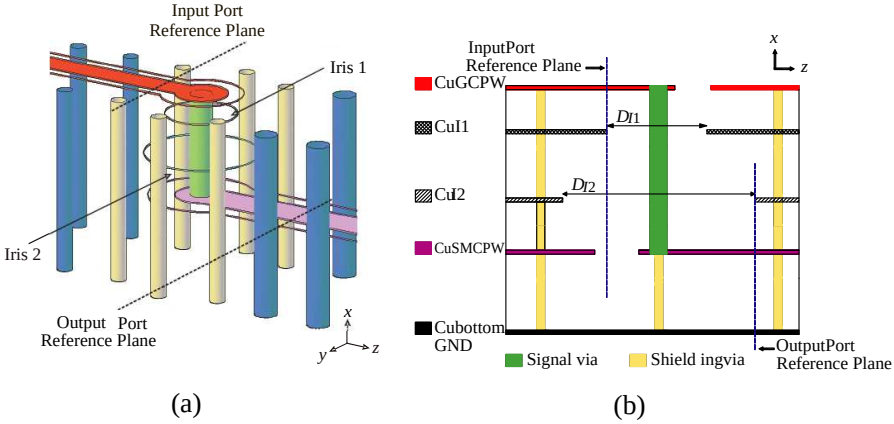


Figure 1. Multilayer structure. (a) 3D view of a GCPW-to-SMCPW transition (ground planes have been removed for clarity). (b) Transition side view showing the position of reference planes, signal and grounding via-holes and interconnecting irises.

via-holes are treated as a coaxial transmission line, while irises in intermediate layers are modeled by parallel capacitors loading the coaxial transmission line. In addition, the input and output pieces of the transmission line surrounding the vertical signal via-hole are modeled as a transmission line with electrical parameters corresponding to those of the even mode of a pair of coupled coplanar waveguides. This results in a circuit model that can be directly extracted from the geometry of the transition using closed expressions and providing a deeper understanding of transition behavior. Simulation results of the developed circuit model have been compared with rigorous 3D electromagnetic simulations for several possible situations in PCB and LTCC technologies with good agreement.

Further model assessment has been carried out by applying this circuit model to design a specific transition for minimum return losses: first, the circuit model is used for a preliminary design, then a full-wave simulator is used to fine-tune the final design. Results confirm that final geometry is very close to the preliminar one. This transition is manufactured and measured, showing an excellent return loss better than 20 dB, from DC to 20 GHz.

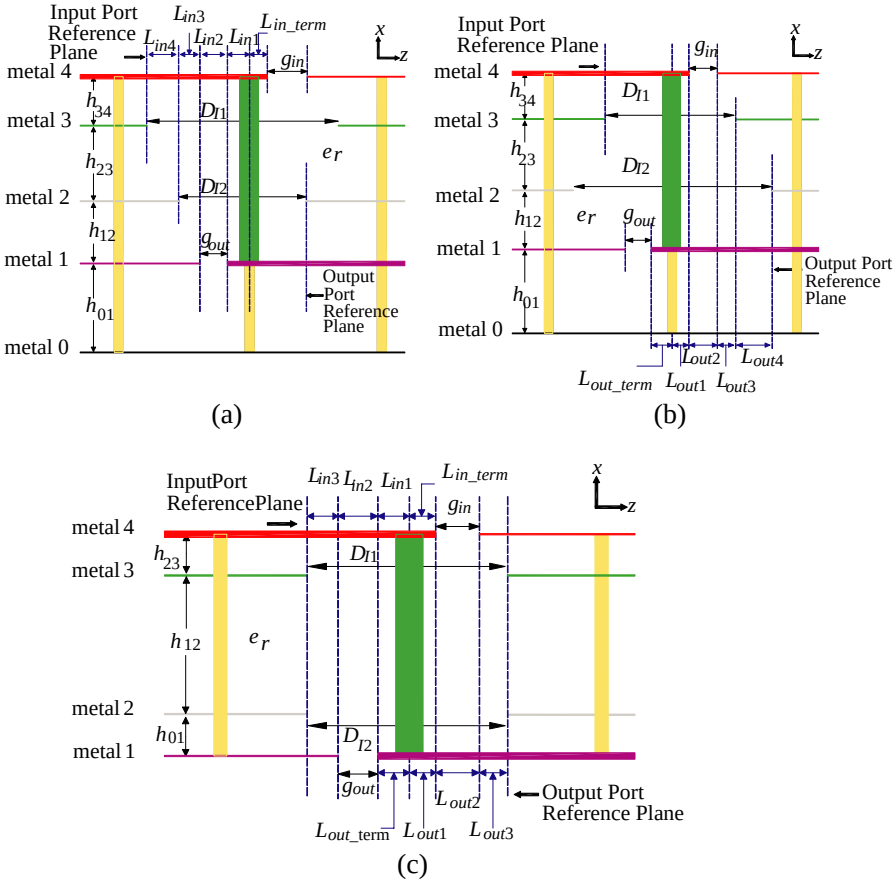


Figure 2. Side views of the multilayer transitions. (a) Transition type I with iris 1 bigger than iris 2. (b) Transition type I with iris 1 smaller than iris 2. (c) Transition type II with the pieces of the access lines.

2. TRANSITION GEOMETRY AND PROPOSED CIRCUIT MODEL

Although a general structure of the analyzed vertical transition has already been shown in the previous section, a detailed transversal view of the specific vertical transitions, used to assess the developed model, is shown in Figure 2. In the scenarios which will be shown, the signal via-hole will interconnect one GCPW line with one buried Shielded Multilayer Coplanar Waveguide (SMCPW) line or two superficial Grounded Coplanar Waveguide (GCPW) lines. Thus two types of

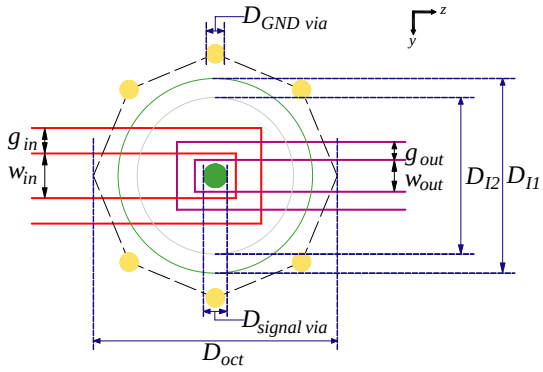


Figure 3. Top view of the multilayer transition showing: the geometries of the input (w_{in}, g_{in}) and output transmission lines (w_{out}, g_{out}); the position of the ground via-holes on the vertices of an octagon (D_{oct}); and the diameters of the irises (D_{I1}, D_{I2}), signal via-hole (D_{signal_via}) and grounding via-holes (D_{GND_via}).

cross section are presented, hereinafter referred to as type I and type II respectively. In addition, the input and output access lines affected by the irises will be divided in different parts. The number of these parts will depend on the iris sizes. To appreciate adequately the maximum number of the horizontal parts that can be produced, two cases have been showed explicitly for type I transitions. Figures 2(a) and 2(b) show a vertical transition (type I) between a GCPW line and a SMCPW line. The only difference between Figures 2(a) and 2(b) is that the iris sizes have been modified to show their influence on the number and type of input and output transmission lines of the our circuit model. On the other hand, Figure 2(c) shows the commonly found transition between two superficial GCPW lines placed on opposites sides of the stack (type II). Finally, Figure 3 shows the top view of the transitions, showing the geometry of the input and output transmission lines and the position and diameters of the via-holes and irises.

The transition circuit model proposed in this work can be seen in Figure 4. It comprises three sections (horizontal input, vertical and horizontal output sections) which are modelled using ideal capacitors and transmission lines, available in commercial microwave circuit simulators. The advantage of the proposed model is that, as will be detailed in the following paragraphs, all circuit model parameters are directly obtained from the geometry of the transition (Figures 2 and 3) by closed analytical formulas.

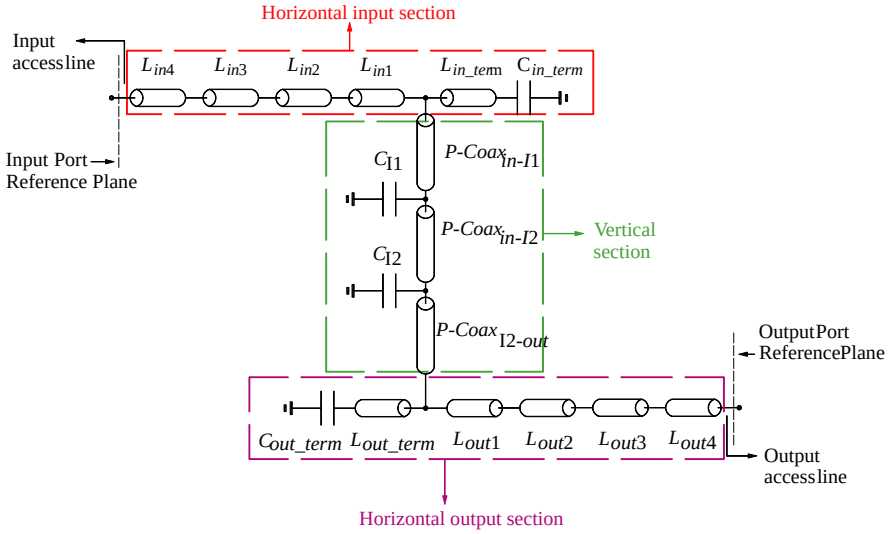


Figure 4. Circuit model of the multilayer transition.

2.1. Vertical Section

As seen in Figures 1 and 2, the transition consists of a via-hole, running through two circular irises in intermediate layers, to interconnect the input and output coplanar waveguide lines. The vertical section is formed by the signal via-hole, which is surrounded by six grounding via-holes whose centres are located on a circle of diameter D_{oct} (see details in Figure 3) to interconnect the ground planes, and the irises through which the signal via-hole passes. This vertical part of the transition is then modeled as a coaxial transmission line loaded with the capacitances of the irises. This is shown in Figure 4 as three transmission lines called P-Coax and two capacitances, C_{I1} and C_{I2}. These capacitances C_{I1} and C_{I2} depend on the iris diameters, D_{I1} and D_{I2} in Figures 2 and 3, and their values can be directly estimated using the expressions available in [10, Eqs. (1a)–(1c) Sec. 5.3b]. The coaxial inner and outer radii are set to the radius of the signal via-hole (D_{signal_via}) and the diameter of the circle on which the grounding via-holes lie (D_{oct}), respectively, as seen in Figure 3. This approximation will be discussed later. Coaxial model impedance is then obtained with well known formulas, [10, Eq. (2.32)].

2.2. Horizontal Sections

The horizontal sections in Figure 4 model the access input and output coplanar waveguide lines from their respective reference planes (as

shown in Figure 2) to their connections with the vertical signal via-hole. Each horizontal section comprises several pieces of transmission line which are characterized by their impedance and effective permittivity. Notice that, as seen in Figure 2, these pieces of transmission line account for the different transversal geometries appearing in the access coplanar waveguide lines as a consequence of ground plane removal, at different levels, to provide the necessary irises in the structure. For the rest of this subsection we will focus on modeling of type I transitions (Figures 2(a) and 2(b)). Application to the type II transition seen in Figure 2(c) will then be easily derived from this explanation.

2.2.1. Horizontal Input Section

As detailed in Figure 2(a), the most complicated situation at the input access line occurs when iris 1 is bigger than iris 2. This situation yields the maximum number of segments of the lines. In this case there are five possible horizontal sections: L_{in1}, L_{in2}, L_{in3}, L_{in4} and L_{in_term}. L_{in4}, L_{in3} and L_{in2} are modeled as GCPW lines [12, Eqs. (18) and (22)] with the ground plane in metal 2, 1 and 0, respectively. L_{in1} consists of broadside-coupled coplanar waveguides (between metal 4 and 1) with the particularity that the odd mode is short-circuited by the via-hole. Therefore, this section is modeled as a transmission line with the characteristic impedance and propagation constant of the even mode of a broadside-coupled coplanar waveguide, which is obtained by placing a magnetic wall in the middle of the stack between metal 4 and 1 [13, Eqs. (7.105) and (7.109)]. L_{in_term} accounts for the small piece of transmission line remaining after being connected to the vertical via-hole. Since it shares the same transversal geometry as L_{in1}, it is also modeled in the same way. This section ends with a capacitor to the ground, C_{in_term}, accounting for gap g_{in} in Figure 2(a), whose value is estimated from [13, Eqs. (9.1) and (9.7)]. Modelling the horizontal input section becomes simpler if iris 1 is smaller than iris 2 as, in this case, it is obvious from Figure 2(a) that L_{in4} should be set to zero.

2.2.2. Horizontal Output Section

The output horizontal sections are modeled following the same approach as described above, as seen in Figure 2(b) (plotted for iris 1 smaller than iris 2): L_{out4} and L_{out3} are modeled as a SMCPW with ground plane in metal 3 and 4 respectively. L_{out2} is modeled as a buried GCPW and L_{out1} and L_{out_term} are modeled as the even mode of a broadside-coupled coplanar waveguide. This section ends with a capacitor to the ground, C_{out_term}, accounting for gap g_{out} in

Figure 2(b), whose value is again estimated from [13, Eqs. (9.1) and (9.7)]. It is also obvious that, if iris 1 is smaller than iris 2, then L_{out4} should be set to zero.

3. MODEL DISCUSSION AND LIMITATIONS

Distributed elements have been used to model some parts of the presented transitions. It could be argued that, being electrically short, such pieces could have been modelled as lumped components, thus redounding in further model simplification. However, there are several reasons to follow the transmission line approach: 1) as will be shown in the model assessment section, model transmission lines can be around 30–35 degrees in electrical length at the highest considered frequency, which indicates that distributed behaviour is relevant; 2) on the other hand, as seen in Figure 2, transmission line lengths depend on the iris dimension and can be directly obtained from the geometry of the transition; and 3) all commercial microwave circuit CAD tools implement transmission line elements which can be used straight away to implement the proposed model. It could also be argued that the changes in the cross section will excite higher order modes and produce fringing effects that are not accounted for in the proposed model, but this is not the case due to the fact that cross section variation between different sections is small enough and the energy in higher order modes is negligible.

Monomode operation of all the transmission line components limits the absolute maximum frequency of model validity. Thus, good model results are not expected near the lowest higher order cutoff frequency of any of the transmission lines (input, output or coaxial) used in the model, including: any of the access coplanar input or output lines or the coaxial line of the vertical section. As the model comprises many different input/output coplanar transmission lines, it would be unpractical to calculate all their cutoff frequencies. Thus, in the next section we will only provide the higher order cutoff frequencies of the input ($f_{GCPW\,access\,line}$) and ouput ($f_{SMCPW\,access\,line}$) coplanar access lines for each particular scenario. In addition, we will calculate the cutoff frequency of the modelled coaxial (f_{coax}), which can be used to estimate the cutoff frequency of the vertical part of the real transition. As a rule of thumb, the maximum usable frequency of the model can be stablished by the heuristic formula

$$f_{\max} = \min(f_{SMCPW\,access\,line}, f_{GCPW\,access\,line}, 0.8 f_{coax}) \qquad (1)$$

where a weighting coefficient of 0.8 is applied to f_{coax} as a safety margin to account for the open nature of the vertical structure which is being simulated by a simple coaxial.

Modelling the vertical via-hole plus grounding via-holes as a coaxial line is a rough approximation that will only yield good results while the shielding in the coaxial is acceptable. Referring to Figure 3 and as a rule of thumb, good shielding is expected if the edge of the octagon, on which the grounding via-holes lie, minus the ground via-hole diameter, D_{GND_via}, is less than $\lambda_g/8$ in the coaxial. Furthermore, as previously mentioned, coaxial impedance has been estimated from [11, Eq. (2.32)]. Obviously an error of a few ohms is expected from this formula depending on each particular situation. In general, if grounding via-hole separation fulfils shielding considerations, then higher errors are expected for larger grounding via-hole diameters. These considerations put further limits on model performance. However, as will be seen in the following section, good engineering results have been obtained with this approach for all the grounding via-hole diameters that have been tested.

The end capacitor, C_{in_term}, is modelled as a CPW line open-circuit end-effect [13, Eqs. (9.1)–(9.7)]. In doing so, the open circuit equivalent length extension is directly calculated from g_{in} and w_{in} applying [13, Eq. (9.7)], and then C_{in_term} is calculated by [13, Eq. (9.4)], where the characteristic impedance and propagation constant are those of the even mode of a broadside-coupled coplanar waveguide (as done previously in Section 2.2.1). A similar approach was followed for the output section capacitor C_{out_term}. As will be shown in the results, this approximation of the open end effect yields acceptable results.

4. MODEL ASSESSMENT

Model assessment was carried out by comparing rigorous 3D EM simulation with HFSS (using infinitesimal metal thickness) in a wide variety of test structures of practical interest. In the HFSS simulator, a waveport with up to three modes has been used to excite the structure. A deembeding procedure has been carried out to ensure a monomode excitation of the transition. The reference planes have been allocated in the same position as it is indicated in Figure 1 and Figure 2. Test structures covered a large scope of situations and included a range of varying parameters, such as: four different stack types (with different dielectric constants and layer thicknesses); two types of transitions (Type I or II, as shown in Figure 2), different numbers of irises (one or two), different widths and gaps of access lines w_{in}, w_{out}, g_{in}, g_{out}), as well as the various diameters appearing in the design (signal via-hole D_{signal_via}, ground via-hole D_{GND_via}, octagon D_{oct}, iris D_{I1}, D_{I2}). These situations were selected to cover realistic transitions used in

typical PCB and LTCC technology.

Four different realistic scenarios (named A to D) involving different stack structures were defined. Table A1 describes the layer thicknesses and dielectric constants of each scenario. Scenarios A and D involve a long type II transition (via-hole length 1800 μm), and a short type I transition (via-hole length 1336 μm), respectively, on a typical soft PCB substrate (RO4350 laminate). Scenarios B and C involved a short type I (via-hole length 600 μm, $\varepsilon_r = 5.9$), and long type II transition (via-hole length 800 μm, $\varepsilon_r = 7.8$), respectively, on two different LTCC substrates (FERRO-A6M, DUPONT-951). It is important to note that, although the different scenarios cover a wide range of via-hole lengths (600–1800 μm), the electrical length of the via-holes, at the maximum simulated frequency, is nonetheless large in all situations (Scenario A: 68°@25 GHz; scenario D: 61.4°@20 GHz; scenario B: 78°@45 GHz; scenario C: 120°@45 GHz).

In all four scenarios, the widths and gaps of the input/output coplanar waveguides (see Figure 3) were calculated to obtain an impedance of 50 Ω outside the transition regions (see Table A2). Then, the effective dielectric constant (ε_{eff}) and characteristic impedance (Z_0) of each piece of transmission line in the horizontal input and output sections of the model can be calculated, as explained in Section 2.2.1 and 2.2.2, by closed expressions, and are given in Tables A3 and A4. For each particular scenario, several situations (versions) were analyzed corresponding to different diameter values: signal via-hole (D_{signal_via}), ground via-hole (D_{GND_via}), octagon on which the grounding via-hole centres lie (D_{oct}), irises in intermediate layers (D_{I1}, D_{I2}). These scenario versions include a wide range of parameter changes and make it possible to obtain a complete view of model behaviour in a wide variety of situations. Detailed descriptions of the different scenario versions are given in Table A5.

From the geometry data in Tables A1, A2, and A5, the rest of the parameters required to define the circuit model in Figure 4 for the different scenarios can be obtained directly, as explained previously, using closed expressions, and are given in Tables A6, A7 and A8 for convenience. In addition, Table A9 contains the cutoff frequencies of input and output coplanar access lines, for each particular scenario, which were obtained from 2D EM simulation. The maximum usable frequency in the model, as calculated from Eq. (1), is also included in this table.

The obtained results in all scenarios are presented and compared on Smith chart and on reflection coefficient in dB. Additionally, a quantitative figure of merit is included to estimate the expected error from this circuit model. The considered figure of merit is the

impedance modulus percentage error. From a reflection coefficient, S_{11}, we can calculate its associated impedance, Z_{in},

$$Z_{in} = Z_0 * \frac{(1 + S_{11})}{(1 - S_{11})}, \tag{2}$$

where the Z_0 is the reference impedance ($50\,\Omega$). Thus, the percentage error of the impedance modulus is calculated as follow

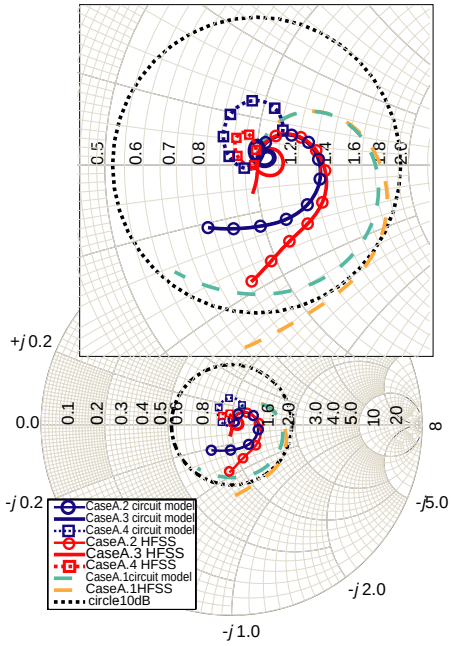
$$Z_{error}{=}100 * \sqrt{\frac{[\mathrm{Re}(Z_{HFSS}) - \mathrm{Re}(Z_{model})]^2 + [\mathrm{Im}(Z_{HFSS}) - \mathrm{Im}(Z_{model})]^2}{[\mathrm{Re}(Z_{HFSS})]^2 + [\mathrm{Im}(Z_{HFSS})]^2}}, \tag{3}$$

where Z_{HFSS} and Z_{model} are obtained by simulation with HFSS and the proposed circuit model, respectively.

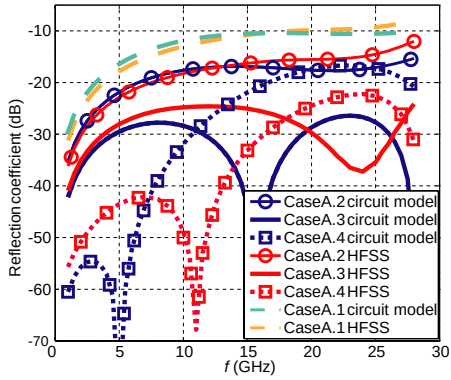
4.1. Model Performance in Scenario A

Four different versions are presented for this symmetric scenario, as seen in Tables A5–A8. In all versions, results are presented up to a maximum frequency of 28 GHz, approximately corresponding to the maximum frequency value in Table A9.

To highlight the idea that modelling the vertical signal and grounding via-holes with a coaxial gives adequate engineering results, the vertical signal and grounding via-holes were modified in the four

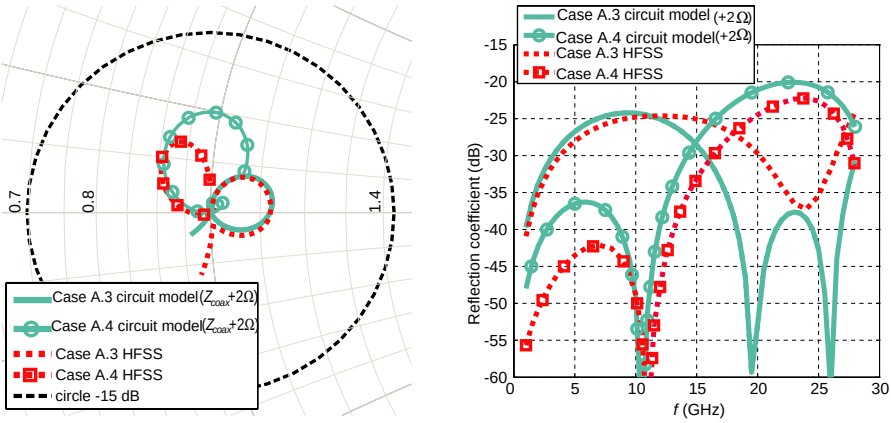


(a)



(b)

Figure 5. Comparison of electromagnetic simulation and circuit model for scenario A. (a) Reflection coefficient (inset into −10 dB circle). (b) Return losses.



(a) (b)

Figure 6. Comparison of electromagnetic simulation and circuit model for case A.3 and A.4 with coaxial impedance adjusted +2 Ω. (a) Reflection coefficient. Smith chart zoom into the circle of −15 dB. (b) Return losses.

versions, yielding a final coaxial impedance variation between 79 Ω to 51 Ω, as indicated in Table A8, while the iris diameter was kept constant. As seen in Figure 5, the circuit model adequately predicts the EM simulation performance. Taking into account Figure 5(b), better result agreement is obtained for versions A.1 and A.2 (in which

D_{GND_via} is 300 µm) than for A.3 and A.4 (in which D_{GND_via} is 200 µm). For these versions, the obtained error from Eq. (3) is less than 20% up to 20 GHz. This is a consequence of the expected difficulties of modelling the complex vertical geometry by a simple coaxial line. However, it is important to note that in this particular scenario a correct adjustment of the coaxial impedance is very critical. Indeed, as shown in Figure 6, just a small $+2\,\Omega$ adjustment of the coaxial impedance would yield much more accurate results.

4.2. Model Performance in Scenario B

Four versions are presented in this type I, LTCC transition scenario (B.1–B.4) whose parameters are summarized in Tables A5–A8. The results are plotted up to 44 GHz. As seen in Table A9, this frequency

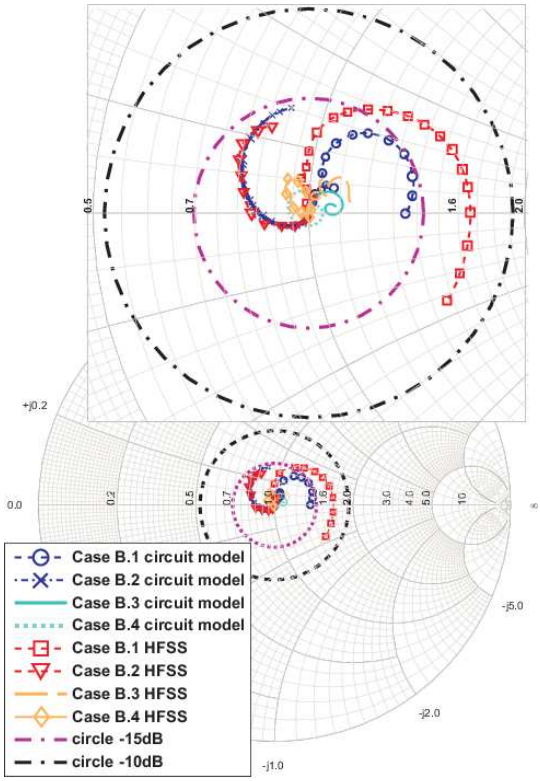


Figure 7. Comparison of electromagnetic simulation and circuit model for scenario B. Reflection coefficient (inset into −10 dB circle).

essentially coincides with calculated $f_{\max}$ for versions B.2–B.4 but clearly exceeds $f_{\max}$ for B.1.

Figure 7 shows a comparison between the electromagnetic and circuit model simulations of the reflection coefficient of the transition, for all the versions B.1–B.4 of this scenario. Figure 8 shows transition return losses. Separate plots are given for versions B.1–B.2 (Figure 8(a)) and B.3–B.4 (Figure 8(b)) because the latter have been further optimized for lower return losses and would be difficult to appreciate in the same scale plot. As can be seen, good results are obtained for all the situations and the model is capable of clearly differentiating between good and bad designs.

The obtained error from Eq. (3) in version B.2 is less than 6% up to 40 GHz. For versions B.3 and B.4 this error is less than 12% up to 40 GHz. Worst model performance is obtained for version B.1, where calculation of the cutoff frequency of the coaxial yields 45 GHz instead of the 61 GHz calculated for versions B.2–B.4 (due to D_{oct} reduction from 1540 µm to 1200 µm). Therefore, in B.1 it is clear that the proposed model is used beyond its reasonable limits, thus increasing its error. In fact, the obtained error from Eq. (3) for this version reaches the 29% in 43 GHz. In addition, differences observed in versions B.3–B.4 should be put into perspective as the very small values of return losses (lower than −25 dB) make it extremely difficult to make an adequate comparison.

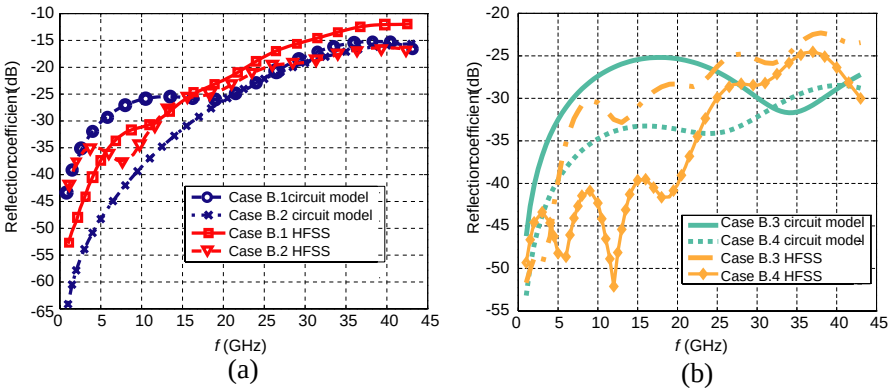


Figure 8. Comparison of electromagnetic simulation and circuit model for scenario B. (a) Return Losses for B.1–B.2. (b) Return Losses for B.3–B.4.

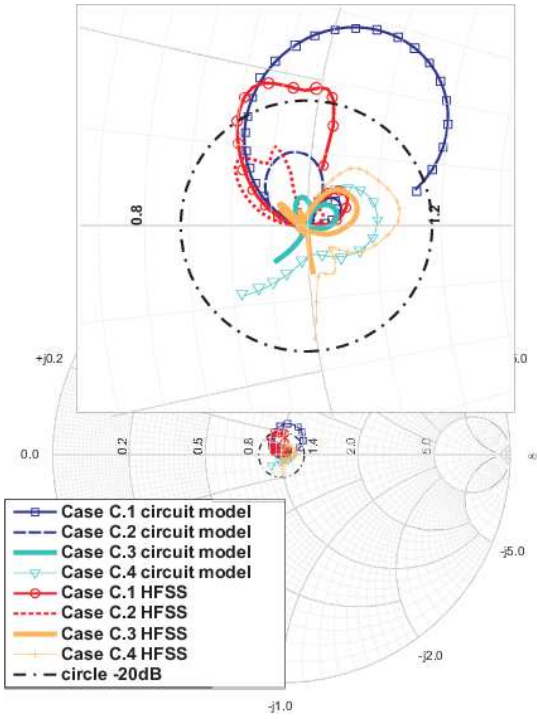


Figure 9. Comparison of electromagnetic simulation and circuit model for scenario C. Reflection coefficient (inset into −20 dB circle).

4.3. Model Performance in Scenario C

This is a type II high dielectric constant LTCC transition scenario, in which four different versions C.1–C.4 are compared. Results are shown up to 44 GHz which slightly exceeds the $f_{\max}$ limit of Table A9.

As can be seen in Figures 9 and 10, in this scenario, a good agreement is also observed for all situations. This scenario is used to show how the model can be used advantageously to achieve a high quality transition. Starting from an unsatisfactory situation in C.1, the return losses are first improved by simultaneously diminishing the signal via-hole diameter (to increase the coaxial impedance), and the iris sizes (to increase the capacitance) yielding a better transition C.2. Further decreasing the signal via-hole diameter yields a high quality transition C.3 where insertion losses are predicted to be below −30 dB and are finally calculated by a 3D EM simulator to be below −28 dB. It must be noticed that model results are still very good despite the very low values of final return losses which make prediction difficult. Finally,

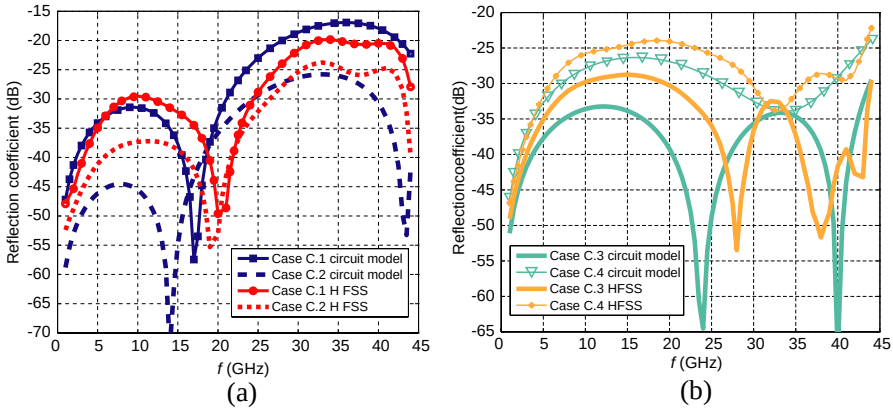


Figure 10. Comparison of electromagnetic simulation and circuit model for scenario C. (a) Return Losses for C.1–C.2. (b) Return Losses for C.3–C.4.

C.4 shows that further pushing the via-hole diameter to lower values degrades transition performance. The obtained error from Eq. (3) for C.2, C.3 and C.4 versions is less than 10% up to 43 GHz. This error is estimated for the C.1 version in 28 GHz.

4.4. Model Performance in Scenario D

This is a type I, low dielectric constant scenario. Five versions are presented (D.1–D.5), as defined in Tables A5–A8. The results are plotted up to 20 GHz which, as seen in Table A9, is slightly lower than the calculated $f_{\max}$ for all the cases.

Figure 11 shows the results for the first three versions D.1–D.3, in which the signal via-hole diameter and octagon diameter has been modified (to change coaxial impedance from 53 Ω to 75 Ω) but iris diameters have been kept constant to a high value so its capacitive effect is almost negligible. The obtained error from Eq. (3) for D.1 and D.3 versions is less than 7% up to 20 GHz. This error is estimated for the D.2 version in 12 GHz. Some performance improvement has been obtained with this strategy, but it is not enough to maintain return losses below a typically required −15 dB level. Further transition refinement can be obtained by adjusting the capacitive effect of the irises. This can be seen in Figure 12, which shows the results of versions D.4–D.5, in which return losses have been reduced to under −23 dB. For these both versions, the obtained error from Eq. 3 is less than 11% up to 20 GHz. Again, good agreement between the circuit model and EM simulation was observed in all versions of this scenario.

5. EXPERIMENTAL RESULTS

For further model validation, a complete transition, corresponding to scenario D, was designed and characterized. In comparison to previously presented idealized results, two new differences exist: i)

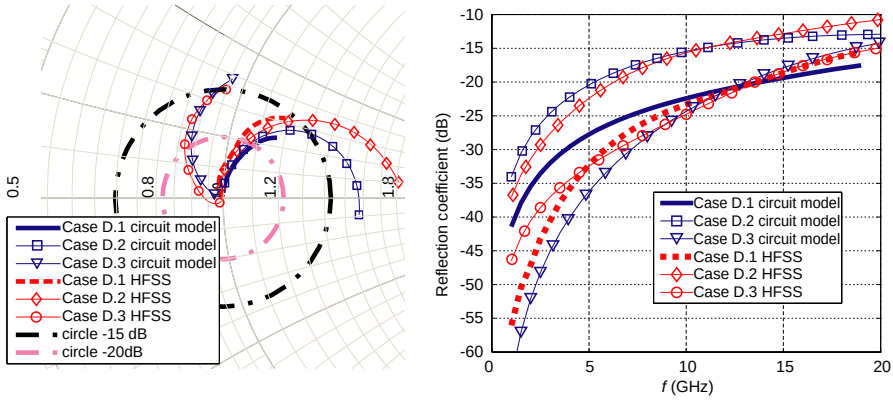


Figure 11. Comparison of electromagnetic simulation and circuit model for versions D.1–D.3. (a) Reflection coefficient. Smith chart zoom into the circle of −15 dB. (b) Return Losses.

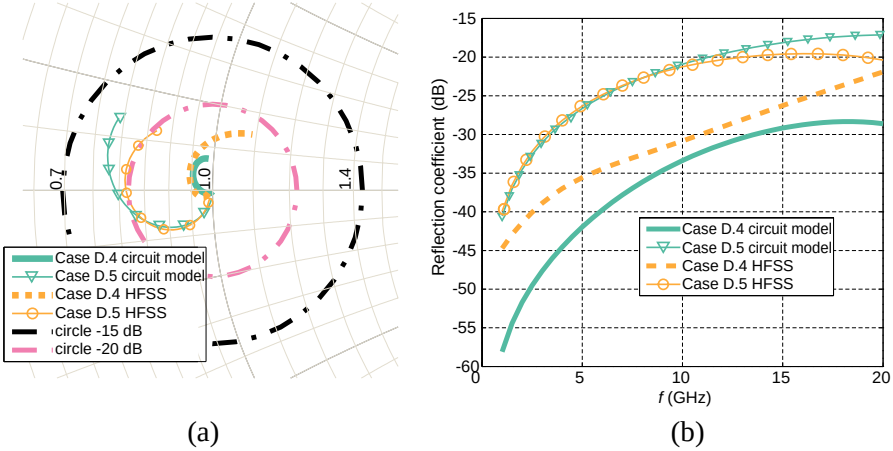


Figure 12. Comparison of electromagnetic simulation and circuit model for versions D.4–D.5. (a) Reflection coefficient. Smith chart zoom into the circle of −15 dB. (b) Return Losses.

conductors have finite thickness, ii) technological issues preclude the use of straight line-end geometry as shown in Figure 3; round shaped end lines, as shown in Figure 1, must be used instead. Both facts will be taken into account in the 3D EM simulations but still, as will be shown later in this section, the circuit model is capable of yielding good engineering results for designing purposes.

Although from previous results, transition D.4 appears to be a good starting point for design, manufacturing restrictions are recommended using the largest possible signal via-hole diameter, in order to relax the tolerances effect on transition behavior. Thus a signal via-hole diameter of 300 µm and a coaxial impedance of 62.4 Ω, as in version D.1, were used as the starting point. The design strategy then focused on finding suitable iris diameters to optimize transition behavior. Figure 13 shows Smith chart plots of the transition's reflection coefficient for several combinations of iris diameters. In addition to the fact that this graph shows that the best results are achieved when D_{I2} is 1500 µm and D_{I1} between 750 µm and 950 µm, it can also be used to attain a better understanding of the transition.

By examining Figure 13, one can conclude that response sensitivity is greatly dependent on iris size and that iris 1 is the key element in this transition. If the diameter of iris 1 is far from the optimum value, then the final response will have virtually no relation to the diameter of iris 2. That is, when iris 1 is 1.5 mm, the response

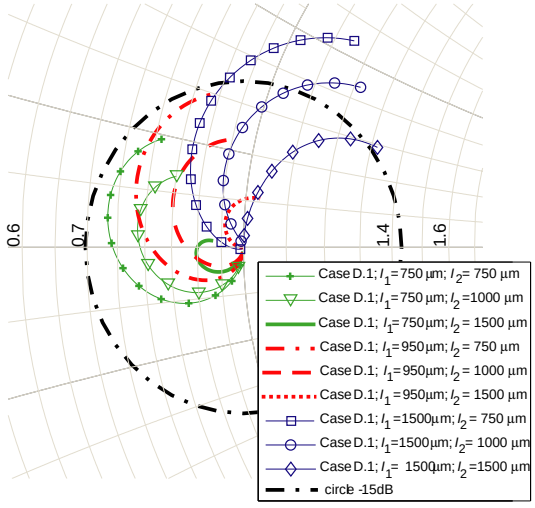


Figure 13. Circuit model behavior in the case D.1 for different combinations of irises 1 and 2. Smith chart zoom into circle of −15 dB.

is poor for any value of iris 2. Only when iris 1 is around 1 mm is the effect of iris 2 relevant. The developed model gives some insight into this behavior. Notice that, as can be seen in Figure 2 and in Tables A5–A8, the irises not only capacitively load the vertical coaxial line, but also modify the length of access line sections L_{in1}, L_{in2}, L_{out1}, L_{out2}, etc. Increasing the diameter of iris 2 increases lengths L_{out3}, L_{out2}, etc, whose impedances are around 59 Ω (Table A4, scenario D); therefore, modifying iris 2 mainly affects the capacitive loading C_{I2}. However, increasing iris 1 not only affects capacitive loading C_{I1}, but also increases L_{in3}, L_{in2}, etc, whose impedance is around 73 Ω (Table A4, scenario D), and thus has a much greater influence on transition behavior.

The last design step consisted of carrying out a final transition optimization using the 3D EM simulator. Simulation showed best transition performance for $D_{I2} = 1500\,\mu m$ and $D_{I1} = 950\,\mu m$, which were used in the final manufactured design. In Figure 14, we again compare the results of the proposed circuit model and rigorous 3D EM simulation, for several iris size values. It must be highlighted that, even though the 3D EM simulation includes two new effects (finite conductor thickness and round shaped end lines), which are not considered in the circuit model, the prediction is still satisfactory and useful for design purposes. The transition was built on standard plastic

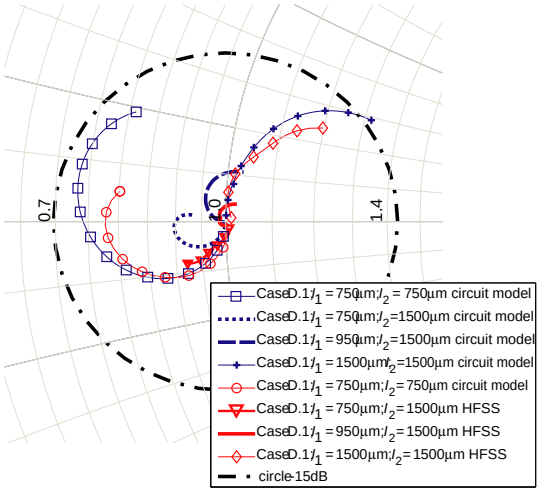


Figure 14. Reflection coefficient. Circuit model versus HFSS behavior in the case D.1 for several combinations of irises 1 and 2. Smith chart zoom into circle of −15 dB.

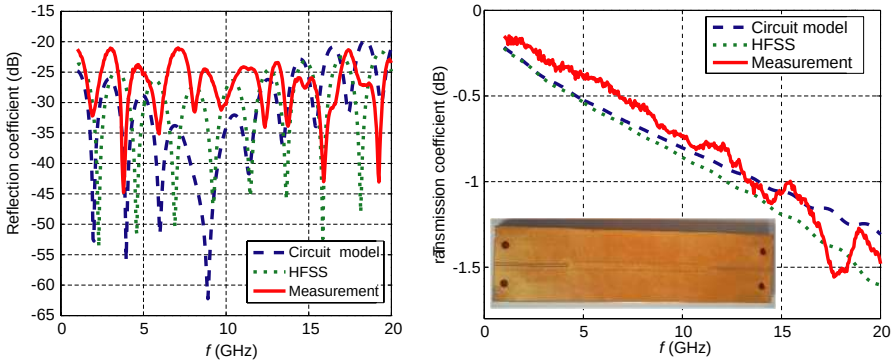


Figure 15. Measured results for the implemented transition in back-to-back configuration. (a) Reflection coefficient. (b) Transmission coefficient.

substrate (RO4350B) and measured in a back-to-back configuration (a 3.4 cm SMCPW transmission line was used to connect both individual transitions). TRL calibration was performed to extract the transition S-parameters using a Vector Network Analyzer. The measurement was carried out with CPW probe tips. The reference planes have been allocated in the same position as it is indicated in Figure 1 and Figure 2. Figure 15 shows the measured results compared to those obtained by simulation. A return loss better than -20 dB in back to back configuration has been measured. Despite fabrication tolerances, a reasonable agreement was observed between the measured and modeled results, thus confirming the validity of the developed model.

6. CONCLUSIONS

In this paper, a new circuit model for vertical transitions between coplanar waveguide systems in multilayer technology was presented. This circuit model was extensively tested in a wide variety of scenarios of practical interest (including a wide range of stack heights, dielectric constants, and transmission line geometry parameters) using different manufacturing technologies, and exhibited good agreement with 3D EM simulations. In addition to giving greater insight into transition behavior, the model was used to design a via-hole transition in standard multilayer technology from DC to 20 GHz, avoiding the intensive use of 3D EM simulations. Experimental results of the manufactured transition showed good agreement between measured results, 3D EM simulations and circuit model simulations.

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APPENDIX A. TABLES OF PHYSICAL AND ELECTRICAL PARAMETERS

Table A1. Stack definition for each defined Scenario (Scenario A to D) used for model assessment. Units in μm.

Scenario	Type	ε_r	h_{01}	h_{12}	h_{23}	h_{34}
A	II	3.66	254	1292	254	-
B	I	5.9	400	200	200	200
C	II	7.8	200	400	200	-
D	I	3.66	1067	559	523	254

Table A2. Dimensions of input and output lines in the multilayer transitions. Dimensions have been designed with the help of expressions [12, Eq. (22)] to obtain $50\,\Omega$ impedance outside the transition. Units in μm.

Scenario	w_{in}	g_{in}	w_{out}	g_{out}
A	615	150	615	150
B	235	100	130	100
C	180	100	180	100
D	470	150	570	210

Table A3. Effective dielectric constant calculated for the horizontal input and output trasnmission lines of the model. Obtained from Table A1 and Table A2 by closed expressions.

S.	L_{in4}	L_{in3}	L_{in2}	L_{in1} /L_{in_term}	L_{out4}	L_{out3}	L_{out2}	L_{out1} /L_{out_term}
A	-	2.35*	2.36*	2.30**	-	2.35*	2.36*	2.30**
B	3.58*	3.55*	3.47*	3.34**	5.90	5.90	5.90	5.90
C	-	4.44*	4.47*	4.33**	-	4.44*	4.47*	4.33**
D	2.39*	2.35*	2.34*	2.29**	3.66	3.66	3.66	3.66

(*) [12, eq. (18)].
(**) [13, eq. (7.105)].

Table A4. Calculated impedance for the horizontal input and output trasnmission lines of the model. Obtained from Table A1 and Table A2 by closed expressions. Units in Ω.

S.	L_{in4}	L_{in3}	L_{in2}	L_{in1} /L_{in_term}	L_{out4}	L_{out3}	L_{out2}	L_{out1} /L_{out_term}
A	-	63.8*	64.4*	66.9**	-	63.8*	64.4*	66.9**
B	59.0*	61.3*	62.7*	67.5**	55.3	56.2	56.6	58.3
C	-	60.3*	60.7*	62.9**	-	60.3*	60.7*	62.9**
D	66.4*	69.0*	70.0*	73.3**	54.3	55.0	55.9	59.1

(*) [12, eq. (22)].
(**) [13, eq. (7.109)].

Table A5. Definition of different Scenario versions. Diameters of irises, GND and signal via-holes and octagon of the multilayer transition (see Figure 3). Units in μm.

Scenario	Version	D_{signal_via}	D_{GND_via}	D_{oct}	D_{I1}	D_{I2}
A	1	175	300	2200	1300	1300
	2	250	300	2200	1300	1300
	3	300	200	1800	1500	1500
	4	350	200	1800	1500	1500
B	1	125	200	1540	1300	1300
	2	125	180	1200	600	1000
	3	86	180	1200	600	1000
	4	94	180	1200	500	1000

Scenario	Version	D_{signal_via}	D_{GND_via}	D_{oct}	D_{I1}	D_{I2}
C	1	100	200	1200	1000	1000
	2	85	200	1200	650	650
	3	77	200	1200	650	650
	4	70	200	1200	650	650
D	1	300	200	2200	1500	1500
	2	200	200	2200	1500	1500
	3	350	200	1900	1500	1500
	4	250	200	2200	700	700
	5	300	200	2200	700	700

Table A6. Physical dimensions of transmission lines of the circuit model: Sections of input access lines for different scenario versions. Obtained from Table A5 by simple inspection of transition geometry. Units in μm.

Scenario	Version	L_{in4}	L_{in3}	L_{in2}	L_{in1}	L_{in_term}
A	1-2	-	200	150	300	300
	3-4	-	300	150	300	300
B	1	0	350	100	200	200
	2-3	0	80	100	120	120
	4	0	30	100	120	120
C	1	-	300	100	100	100
	2-3-4	-	125	100	100	100
D	1-2-3	0	290	210	250	250
	4-5	0	0	150	200	200

Table A7. Physical dimensions of transmission lines of the circuit model: Sections of output access lines for different Scenario versions. Obtained from Table A5 by simple inspection of transition geometry. Units in μm.

Scenario	Version	L_{out4}	L_{out3}	L_{out2}	L_{out1}	L_{out_term}
A	1-2	-	200	150	300	300
	3-4	-	300	150	300	300
B	1	0	350	100	200	200
	2-3	200	80	100	120	120
	4	250	30	100	120	120
C	1	-	300	100	100	100
	2-3-4	-	125	100	100	100

Scenario	Version	L_{out4}	L_{out3}	L_{out2}	L_{out1}	L_{out_term}
D	1-2-3	0	350	150	250	250
	4-5	0	0	150	200	200

Table A8. Electrical parameters associated to coaxial line and lumped elements of the circuit model. Obtained from Tables A1, A2, and A5 by closed expressions. Impedances in (Ω) and capacitances in (fF).

Scenario	Version	Z_{coax} (*)	C_{in_term} (**)	C_{out_term}	C_{I1} (***)	C_{I2}
A	1	79.3	17.3	17.3	10.0	10.0
	2	68.1	17.3	17.3	13.0	13.0
	3	56.1	17.3	17.3	2.7	2.7
	4	51.3	17.3	17.3	2.7	2.7
B	1	62.0	9.8	11.5	1.6	1.6
	2	55.8	9.8	11.5	16.0	1.8
	3	65.1	9.8	11.5	11.8	1.5
	4	62.9	9.8	11.5	17.5	1.5
C	1	53.4	10.5	10.5	2.0	2.0
	2	56.8	10.5	10.5	12.5	12.5
	3	58.8	10.5	10.5	12.0	12.0
	4	61.0	10.5	10.5	11.5	11.5
D	1	62.4	14.0	29.1	9.4	9.4
	2	75.2	14.0	29.1	6.4	6.4
	3	53.0	14.0	29.1	4.8	4.8
	4	68.1	14.0	29.1	41.0	41.0
	5	62.4	14.0	29.1	52.0	52.0

(*) [11, eq. (2.32)].
(**) [13, eq. (9.1)–(9.7)].
(***) [10, eq. (1a)–(1c) Sec. 5.3b].

Table A9. Cutoff frequencies of transmission lines and maximun usable frequency of the model, $f_{\max}$. Units in GHz.

S.	Version	$f_{GCPW\_accessline}$	$f_{SMCPW\_accessline}$	f_{coax}	$f_{\max}$
A	1-2	30	-	41	30
	3-4	30	-	46	30
B	1	46	49	45	36
	2-3-4	46	49	61	46
C	1-2-3-4	47	-	53	44
D	1-2-3-4-5	39	22	40	22
		2D analysis HFSS	2D analysis HFSS	[14, Eq. (5-16)]	Eq. (1)

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