Progress In Electromagnetics Research, Vol. 128, 331–346, 2012

DESIGN OF LOW-LOSS AND HIGHLY-SELECTIVE CMOS ACTIVE BANDPASS FILTER AT K-BAND

S. Wang* **and B.-Z. Huang**

Graduate Institute of Computer and Communication Engineering, National Taipei University of Technology, 1, Sec. 3, Chung-hsiao E. Road, Taipei 10608, Taiwan, R.O.C.

Abstract—In this paper, a second-order Chebyshev active bandpass filter (BPF) with three finite transmission zeros is presented. The filter utilizes a tapped-inductor feedback technique to compensate resistive losses of on-chip inductors, and a shunt-feedback inductor between input and output ports to achieve the transmission zeros. Moreover, one transmission zero is in the lower stopband, and two transmission zeros are in the upper stopband, thus improving the selectivity of the filter significantly. The filter is designed and fabricated in a standard 0.18-μm CMOS technology with a chip area of 0.57 mm × 0.65 mm including all testing pads. The circuit draws 6 mA from a 0.7-V supply voltage. Additionally, the filter achieves a 1.65-dB insertion loss and 13.2-dB return loss with a 17% 3-dB bandwidth at 23.5 GHz. The measured NF and input $P_{1\,\mathrm{dB}}$ is 6.7 dB and −3.5 dBm. The rejection levels at the transmission zeros are greater than 15.2 dB. Finally, the large-signal characterizations are also investigated by the 1-dB compression point ($P_{1\,\mathrm{dB}}$) of the filter.

1. INTRODUCTION

Scalable and advanced CMOS technologies demonstrate low-cost, high-integration, and good-reliability potentials which make digital, analog, and radio-frequency (RF) circuitry in a single chip realistic [1–5]. However, significant losses of CMOS inductors resulting from its low-resistivity substrate limit their system applications and integrations at radio frequencies [6, 7]. The inherent losses degrade performances of BPFs such as insertion losses, return losses, and out-of-band attenuation rates. Therefore, bulky and expensive off-chip BPFs

Received 13 March 2012, Accepted 24 May 2012, Scheduled 1 June 2012

* Corresponding author: Sen Wang (wangsen@ntut.edu.tw).

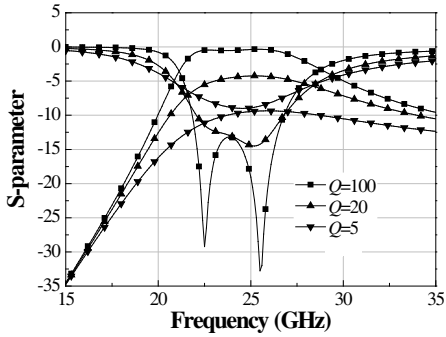

Figure 1. Frequency responses of 2nd-order series-C coupled BPF.

are still required to attenuate large out-of-band interferences and to pass in-band signals with minimal losses. Once high-quality (Q) factors of CMOS inductors and on-chip BPFs are achieved, it would enable a greater variety of transceiver architectures to be realized in a monolithic form [8]. Fig. 1 shows an example on a 2nd-order series-C coupled BPF at K-band BPF. The BPF features better frequency responses such as insertion and return losses with higher Q-factor inductors. Moreover, the filter becomes loss-free with a Q-factor of 100 at least.

Typically, Q-enhanced techniques such as silicon-on-insulator (SOI) or micro-electro-mechanical systems (MEMS) for purely passive inductors require special and additional post-processes to minimize resistive losses in the silicon substrate [9, 10]. However, the inductors consume large chip area, and their Q-enhanced factors are also limited (typically $Q_{\text{peak}} < 30$). On the contrary, purely active inductors take advantage of CMOS transistors to realize superior-Q factors [11–13]. The inductors feature an ultra-compact chip size, and can be a tunable design including inductance and Q-factor tuning. However, these transistor-based inductors consume high-power consumption and the operating frequencies are also limited to gigahertz. In addition to purely passive and active inductors, many semi-passive inductors or resonators consisting MOS transistors and passive transformers or transmission lines are presented [14–19]. These circuits utilizing transformer feedback architectures [14–16] or complementary cross-coupled pairs [18, 19] to compensate resistive losses achieve high-Q factors and high operating frequencies with moderate power consumption. Recently, a novel Q-enhanced inductor using tapped-inductor feedback has been presented [20, 21]. Compared with conventional transformer feedback architectures, the tapped-

inductor feedback architecture features high inductance, low-power consumption, and compact size. Therefore, this Q-enhanced technique using tapped-inductors is adopted in the proposed K-band CMOS BPF.

A main drawback of on-chip BPFs is their inferior selectivity due to the low order of the filters [14–20]. As shown in Fig. 1, the stopband attenuation of the 2nd order BPF is not significant, especially in upper stopband. Typically, higher order of LC-based CMOS filters results in higher insertion losses and larger chip area. Previously reported BPFs with high selectivity are achieved by placing transmission zeros on both sides of their passband skirts [22–28]. The compact and highly-selective BPFs using modified coupled inductors or a shunt-feedback capacitor to generate two or three transmission zeros appearing on both sides of the passband are all realized in low-temperature cofired ceramics (LTCC) technologies [22–24]. Furthermore, the BPFs using a series-feedback capacitor and a shunt-feedback capacitor to introduce transmission zeros are all realized in CMOS technologies [25–27]. These CMOS BPFs operate above K-band because of loss considerations of transmission lines or inductors. Recently, a filter with a shunt-feedback inductor between input and output to generate three transmission zeros was successfully verified [29]. The shunt-feedback inductor topology contributes an additional transmission zero in the upper stopband compared with a shunt-feedback capacitor topology.

In this paper, we present the design and implementation of a K-band active BPF with low-power consumption in 0.18-μm CMOS technology. To the best of authors' knowledge, this design is the first active BPF using the proposed Q-enhanced technique while maintains three finite transmission zeros achieved by a shunt-feedback inductor. This paper is organized as follows. In Section 2, the proposed BPF using a feedback inductor to introduce three finite transmission zeros will be derived mathematically and graphically. Then the design, nonlinearity, stability, and noise considerations of the Q-enhanced technique using negative resistances to compensate resistive losses of inductors will be investigated. Section 3 details the implementation and experimental results of the filter. Finally, a conclusion is provided in Section 4.

2. DESIGN METHODOLOGY OF THE ACTIVE BPF

2.1. Derivation of the Transmission Zeros

Coupled-resonator topologies utilize either series or parallel resonators with reasonable component values which are practical in a standard CMOS process. A conventional second-order series-C coupled BPF

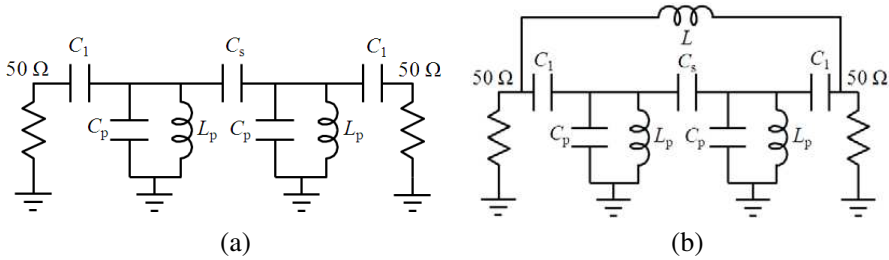

Figure 2. (a) A conventional second-order series-C coupled BPF. (b) Schematic of the proposed BPF.

using admittance (J) inverters to minimize the number of inductors is shown in Fig. 2(a). One advantage of coupled-resonator filters is the repeatability of the same resonator, which simplifies the filter circuitry. However, the conventional prototype features poor selectivity due to its two transmission zeros at dc and infinite frequencies. The proposed circuit is the conventional BPF with a shunt-feedback inductor (L) between the input and output as shown in Fig. 2(b). It will be demonstrated in this section that the feedback inductor will introduce three additional transmission zeros at finite frequencies. One is in the lower stopband, and two are in the upper stopband.

The location of the transmission zeros can be derived from the overall admittance matrix which is the sum of a conventional second-order coupled resonator filter and the shunt-feedback inductor. The y_{12} of the coupled-resonator filter without the feedback inductor can be expressed as

$$y_{12} = \frac{s^3 C_1^2 C_s}{(sC_a + 1/sL_a)^2 - s^2 C_s^2}, \tag{1}$$

where $C_a = C_1 + C_p$ and $L_a = L_p \,//\, \frac{1}{s^2 C_s}$.

And the overall admittance matrix of the proposed filter in Fig. 2(b) can be obtained as

$$Y_t = \begin{pmatrix} \frac{1}{sL} + y_{11} & -\frac{1}{sL} + y_{12} \\ -\frac{1}{sL} + y_{21} & \frac{1}{sL} + y_{22} \end{pmatrix} \tag{2}$$

Therefore the transmission zeros can be obtained by solving the following equation:

$$-\frac{1}{sL} + y_{12} = 0 \tag{3}$$

And (3) can be also given as

$$s^6 C_1^2 L_a^2 C_s L + s^4 L_a^2 \left(C_a^2 - C_s^2\right) + 2s^2 L_a C_a + 1 = 0. \tag{4}$$

As shown in (3), a sixth-order polynomial is obtained, and the locations of the three finite transmission zeros will be the three positive roots of the polynomial.

A second-order Chebyshev BPF of 0.2-dB passband ripple, 24-GHz center frequency, and 4-GHz bandwidth is used to demonstrate the proposed methodology. Thus, the corresponding components values in Fig. 2(b) are $C_1 = 50.13\,\text{fF}$, $C_s = 20.56\,\text{fF}$, $C_p = 38.8\,\text{fF}$, and $L_p = 0.426\,\text{nH}$. Moreover, the feedback inductor L equals 1.4 nH. Fig. 3 plots the simulated results of the circuit model with and without the feedback inductor. It is observed that the passband characteristics such as bandwidth and return losses of the filter with and without L are different slightly. As shown in Fig. 3, the introduction of L results in one transmission zero in the lower stopband, and two transmission zeros in the upper stopband. The two transmission zeros in the upper stopband improve the selectivity of the filter significantly. And the three transmission zeros of the proposed topology are 20 GHz, 36.6 GHz, and 48 GHz, with good rejection levels.

Generally, to determine the three transmission zeros of the proposed filter, the roots in (4) are difficult to be solved mathematically. Therefore, (3) is more practical to determine the three roots graphically by intersection of curves of $1/sL$ and y_{12}. Fig. 4 plots the suspectance of $1/sL$ and y_{12}. The results of the filter with $L = 1.4\,\text{nH}$ are used to demonstrate the design methodology. Two of the transmission zeros are close to the center frequency of the filter, and are at opposite sides of the passband, thus improving the selectivity of the filter. One of the transmission zeros is at high frequencies.

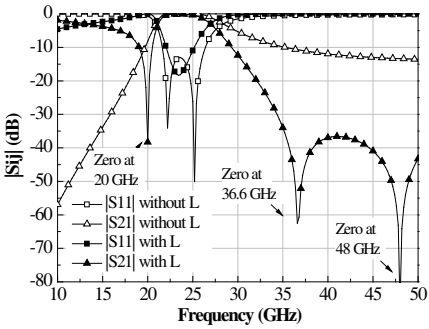

Figure 3. Simulated $|S_{21}|$ and $|S_{11}|$ of the series-C coupled BPF with and without the feedback inductor.

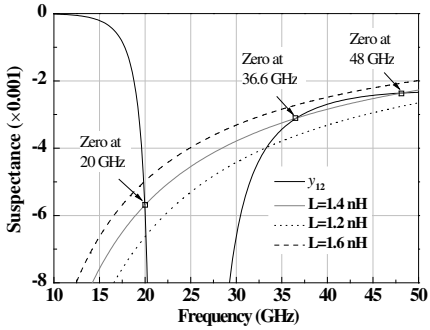

Figure 4. Locations of the transmission zeros.

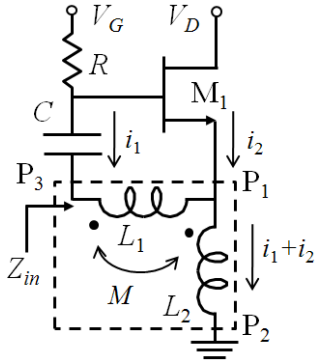

Figure 5. Schematic of the proposed Q-enhanced inductor.

Moreover, an appropriate value of L should be chosen to maintain the existence of three transmission zeros. For examples, the 1.6-nH inductor introduces only one transmission zero at the lower stopband, and no transmission zero at the upper stopband as shown in Fig. 4.

2.2. Q-Enhanced Inductor

The proposed Q-enhanced inductor using a tapped-inductor feedback topology is shown in Fig. 5. V_G and V_D are the bias for the gate and drain terminals of the NMOS (M_1), respectively. R is a high-resistive resistor providing RF signal blocking, and eliminating the need for an RF choke. The tapped-inductor is tapped to the source of M_1 resulting in a current flow $i_1 + i_2$ into L_2. The current flow and the mutual inductance (M) will increase the equivalent inductance of the circuit drastically. The input impedance Z_{in} of the proposed inductor can be approximated as

$$Z_{\text{in}} \cong \left(R_1+R_2-\frac{Mg_m}{C}-\frac{L_2g_m}{C}\right)+j\omega\left(L_1+L_2+2M+\frac{g_mR_2}{\omega C}\right). \quad (5)$$

where R_1, R_2, and g_m are resistive losses of L_1, resistive losses of L_2, and transconductance of M_1, respectively. The real part of Z_{in} consists of resistive losses of L_1 and L_2, and negative resistances related to M, L_2, g_m, and C. Therefore, the overall resistive losses of Z_{in} can be compensated by both M and L_2. Compared to conventional transformer feedback topologies whose resistive losses are merely compensated by M, the proposed topology demonstrates a low-power design. The Z_{in} is inductive from DC to high frequencies as shown in (5) since the effects of high impedance of the RC series network and the input impedance of M_1 at the gate terminal can be

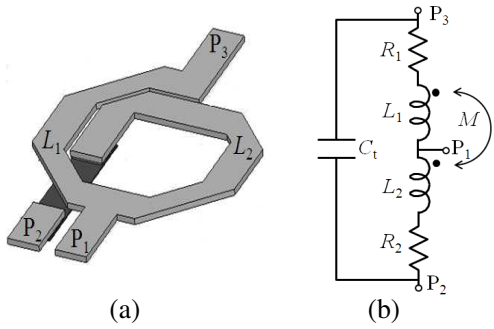

Figure 6. (a) Physical layout and (b) simplified model of the proposed non-center-tapped spiral inductor.

neglected. Moreover, the imaginary part of Z_{in} not only consists of L_1 but also L_2 and $2M$. Unlike conventional transformer feedback topologies, the proposed topology also demonstrates an inductance-enhanced characteristic.

Figure 6(a) shows the physical layout of the proposed non-center-tapped spiral inductor. The inductor can be regarded as an equivalent transformer circuit model with a common node, or the tapped node (P_1). The polarity and port connection of the equivalent transformer formed by L_1 and L_2 are shown in Fig. 5. P_1, P_2, and P_3 are connected to the corresponding node Z_{in}, source terminal of M_1, and ground, respectively. As shown in the physical layout, the inductance of L_2 is higher than that of L_1 for the non-center-tapped inductor, since L_2 contributes the negative resistance in (5). A simplified model of the tapped inductor is shown in Fig. 6(b). C_t is the total capacitance including metal coupling capacitance, oxide capacitance between the inductor and substrate, and other parasitic capacitance. Therefore, the self-resonant frequency (f_{res}) of the proposed inductor can be approximated as

$$f_{res} = \frac{1}{2\pi\sqrt{\left(L_1 + L_2 + 2M + \frac{g_m R_2}{\omega C}\right) \cdot C_t}}. \tag{6}$$

To verify the circuit concept and analysis mentioned above, assuming R, C, V_D, and aspect ratio of M_1 in Fig. 5(a) are 20 kΩ, 0.9 pF, 0.7 V, and (36 μm/0.18 μm), respectively. Moreover, the width, spacing, and inner radius of the tapped inductor in Fig. 6(a) are 15 μm, 3 μm, and 25 μm, respectively. The passive components and parasitic extraction of the layout has been fully characterized by HFSS (Ansys Inc.), and the transistor models provided by TSMC foundry are

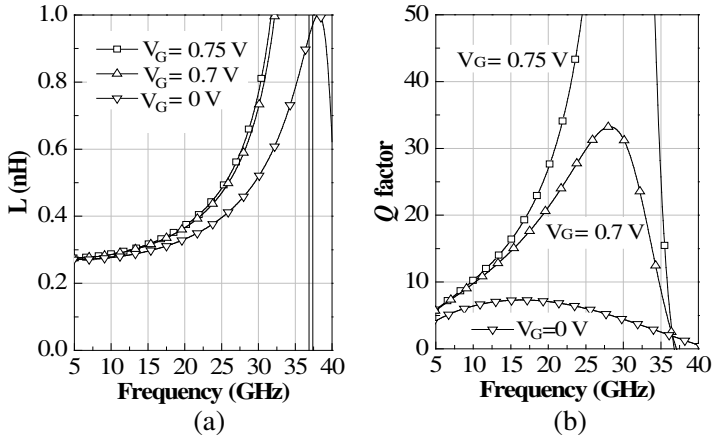

Figure 7. (a) Simulated inductance and (b) Q factor of the proposed inductor under different bias conditions.

also characterized by ADS (Agilent Technology Inc.). The simulated inductances and Q factors of the proposed circuit under different bias conditions are shown in Fig. 7. Increasing V_G increases the equivalent inductance, and lowers the self-resonant frequency due to the term of g_m in (5) and (6). The simulated inductances at 24 GHz are 0.435 nH, 0.425 nH, and 0.375 nH under V_G of 0.75 V, 0.7 V, and 0 V. The simulated self-resonant frequencies with V_G of 0.75 V, 0.7 V, and 0V are 36.8 GHz, 37.1 GHz, and 41.6 GHz, respectively. As shown in Fig. 7(b), with V_G of 0 V, 0.7 V, and 0.75 V, the Q factors at 24 GHz are 6.3, 28.1, and 46.1, respectively. Moreover, the V_G of 0.75 V merely draw a current flow of 2.3 mA.

The simulated values of the inductance, resistance, and Q factor are related to by the g_m, which is considered constant under the small-signal approximation. Therefore, it is not accurate for the inductor operating in the large-signal region. As the incident signal power levels (Pin) increase, the excess voltage swing leads to a decrease in g_m of M_1. The electrical characteristics would deviate from their small-signal values and result in undesirable signal distortion because of the nonlinearity of the active device (M_1). Based on the same bias condition mentioned above, the large-signal behavior of the Q-enhanced inductor is characterized by different Pin. The impact of Pin on the equivalent inductance and Q factor are shown in Fig. 8. The equivalent inductance is reduced with Pin due to the decrease in g_m. Moreover, the Q factor is degraded at higher input power levels since the M_1 would operate in the triode regions at large-signal operations.

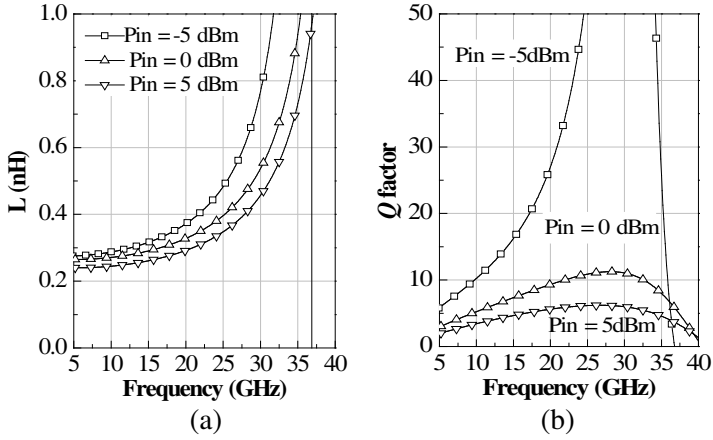

Figure 8. (a) Simulated inductance and (b) Q factor of the proposed inductor under different incident signal power levels.

It is noted that the curves with Pin of -5 dBm seems identical to the curves with V_G of 0.75 V in Fig. 7, and therefore it demonstrates that the input ($P_{1\,\mathrm{dB}}$) of the Q-enhanced is larger than -5 dBm.

2.3. Stability and Noise Consideration

The negative resistance of the positive feedback circuit to compensate resistive losses of an inductor could result in potential instability depending on the g_m, power consumption, and the terminating impedances. Moreover, if the positive feedback circuit is applied to an unconditionally stable filter design, the stability factor (k) of the two port network must be large than 1 for all frequencies. Fig. 9 shows the resonator of the active BPF with the resistive losses (R_c) of C_p and the negative resistance (R_{neg}) of the Q-enhanced circuit. In order to achieve a lossless resonator, the negative resistance R_{neg} must compensate the capacitor losses R_c. Too much negative resistance (R_{neg}) or power consumption (g_m) of the resonator would result in circuit instability. As a result of it, the g_m must comply with the following equation which can be derived from (5).

$$R_{neg}\left(1+Q_L^2\right) = -R_c \tag{7}$$

where $R_{neg} = (R_1 + R_2 - \frac{Mg_m}{C} - \frac{L_2 g_m}{C})$ and $Q_L = \frac{\omega L_p}{R_{neg}}$.

The detailed noise analysis of Q-enhanced inductor and transistors has been presented in [30–32]. With reference to the circuit shown in Fig. 5 and Eq. (5), three main noise sources are the thermal noise

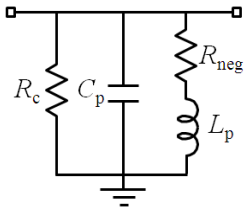

Figure 9. The resonator of the active BPF.

($\overline{v_{1n}^2} = 4kTR_1\Delta f$) of R_1, the thermal noise ($\overline{v_{2n}^2} = 4kTR_2\Delta f$) of R_2, and the thermal drain current noises ($\overline{i_{d1}^2} = 4kT\gamma g_m\Delta f$) of M_1. The RF signal block/bias resistor R, although typically large (20 kΩ), does not contribute significantly to the overall noise of the circuit. Therefore, the total noise voltage ($\overline{v_{\text{in}}^2}$) that appears at the input terminal is mainly contributed by the three noise sources. Moreover, the in-band noise figure of the second-order coupled-resonator BPF using active devices can be derived from [31, 32] as follow:

$$F = 1 + \frac{2\sqrt{g_1 g_2}}{Q_c}\left(\frac{2\pi f_o}{\text{BW}}\right)\left\{1 + Z_o\frac{F_{50} - 1}{R_c}\right\}. \tag{8}$$

where g_1 and g_2 are the lowpass filter prototype parameters. Q_c and F_{50} are the quality factor of C_p and the 50-Ω noise figure of the NMOS. Eq. (8) reveals that Q_c, center frequency (f_o), and bandwidth (BW) of the filter dominate its noise figure.

3. IMPLEMENTATION AND MEASUREMENT

Figure 10(a) presents the schematic of the CMOS active BPF using two Q-enhanced inductors to compensate resistive losses and one feedback inductor to introduce three finite transmission zeros. Since the passband characteristics such as bandwidth and return losses of the filter with and without L are different slightly. Therefore, some components of the prototype filter are tuned finely by EM simulations to achieve better insertion and return losses. The filter is fabricated in a standard 0.18-μm CMOS process which provides one poly layer and six metal layers (from M_1 to M_6). Capacitors in the design are composed by metal-insulator-metal (MIM) capacitors with a 1-fF/μm^2 capacitance density. The two non-center-tapped inductors and the feedback inductor are all realized on the top metal layer (M_6) to minimize resistive losses. Fig. 10(b) shows the chip photo of the filter with a chip area of 0.57 mm× 0.65 mm including all testing pads. The upper inductor in Fig. 10(b) is the feedback inductor L. The width,

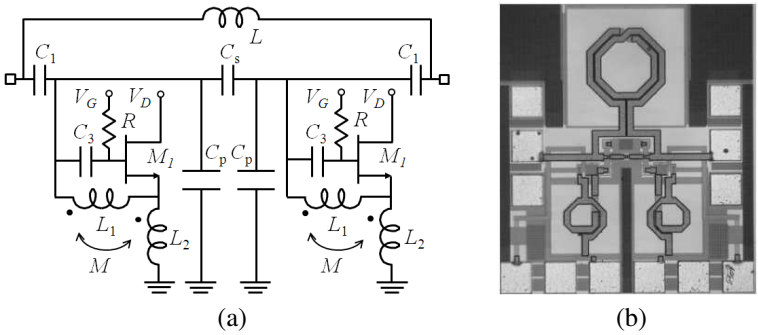

Figure 10. (a) Schematic and (b) chip photo of the proposed CMOS active BPF with a chip size of 0.57 mm × 0.65 mm.

spacing, and inner radius of the 2-turn symmetrical inductor are 15 μm, 2 μm, and 54 μm, respectively.

S-parameters, noise figure, and nonlinearity measurements of the active BPF were performed after the short-open-load-through (SOLT) calibration procedures to eliminate the undesired parasitic of the ground-signal-ground (GSG) pads. The power for calibration was set as −20 dBm at 50-Ω system. Additionally, the small-signal characterizations for the filter are conducted based on the same conditions mentioned above. The supply voltage is at $V_G = 0.8$ V and $V_D = 0.7$ V with a total current of 6 mA and dc power consumption of 4.2 mW. Compared to the simulated power consumption (1.61×2 mW) of Q-enhanced inductors in Section 2, the higher measured power consumption results from interconnectons of the layout and resistive losses of C_p. Good agreement between the simulated and measured results of the filter can be also observed in Fig. 11.

The measured results demonstrate the center frequency of the filter is 23.5 GHz, and the bandwidth is 4 GHz with 1.65-dB insertion loss and 13.2-dB return loss as shown in Fig. 11(a). The 1.65-dB insertion loss is mainly contributed by the feedback inductor L since the negative resistances are merely used to compensate the resistive losses of L_p and C_p. Moreover, the introduction of L results in one transmission zero in the lower stopband and two transmission zeros in the upper stopband. The three measured transmission zeros are at 20.6 GHz, 27.6 GHz, and 41.7 GHz, with a 15.2-dB, 25.5-dB, and 35.2-dB rejection level. The measured transmission zeros differ from the results in Fig. 4 slightly because electromagnetic simulations must be considered for the practical design. The measured NF and input $P_{1\,\mathrm{dB}}$ at 23.5 GHz is 6.7 dB and −3.5 dBm, respectively. The three peak NF

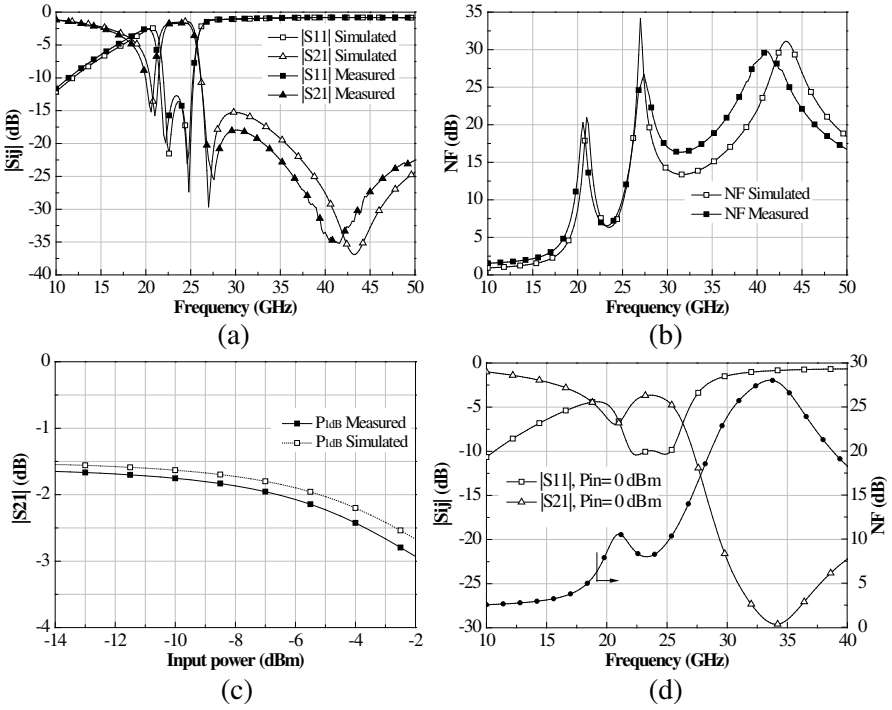

Figure 11. (a) Measured and simulated S-parameters, (b) NF, and (c) input $\mathrm{P}_{1\,\mathrm{dB}}$. (d) Measured S-parameters and simulated NF with Pin of 0 dBm.

values of the filter are related to the corresponding transmission zeros. Fig. 11(d) shows the large-signal measurement of the filter when the input power level is increased from −20 dBm to 0 dBm. The measured results demonstrate the return loss is about 10 dB, the insertion loss is increased from 1.65 dB to 3.86 dB, and the simulated NF is 8.1 dB at 23.8 GHz. Finally, a figure of merit (FOM) which allows comparison between active RF BPFs is given as follows [14]:

$$\mathrm{FOM} = 10\log\left(\frac{N \times P_{1\,\mathrm{dBw}} \times f_o}{\mathrm{BW} \times P_{\mathrm{DC}} \times \mathrm{NF}}\right). \tag{9}$$

where N is the order of a filter, $\mathrm{P}_{1\,\mathrm{dBw}}$ is the in-band input compression point in Watt, f_o is the center frequency in Hertz, BW is the ratio of the 3-dB bandwidth at f_o, P_{DC} is the power consumption in Watt, and NF is the noise factor. Table 1 summarizes the previously reported active BPF. This work demonstrates a high FOM while maintains three finite transmission zeros.

Table 1. State-of-the-art of previously reported active bandpass filters.

Reference	[14]	[15]	[16]	[17]	[18]	[19]	This Work
Process	0.18 µm CMOS	0.25 µm CMOS	0.18 µm CMOS	0.15 µm GaAs	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Order (N)	4	3	3	2	2	2	2
f_o (GHz)	2	2.14	2.36	22.6	34.2	22.7	23.5
BW (%)	6.5	2.8	2.5	4	18.8	7.3	17
Number of Transmission Zeros	0	0	0	0	0	0	3
P_{DC} (mW)	16.6	5	8.8	50.4	3.7	3.3	4.2
NF (dB)	15	18.9	19	17	7*	14.1	6.7
$P_{1\,dB}$ (dBm)	−6.6	−13.4	−20.4	−19	−4.6	−7.7	−3.5
Chip Size (mm^2)	1.21	1.89	2.25	1	0.12**	0.13**	0.37
FOM (dB)	77.1	69	65.6	67.5	98.3	91	98

* Simulated results
** Without testing pads

4. CONCLUSION

A highly-selective and low-loss CMOS active BPF with three finite transmission zeros is designed, implemented, and verified experimentally in a standard 0.18-µm CMOS process. Firstly, the theory of the additional transmission zeros by using a feedback inductor in the filter is investigated mathematically and graphically. Secondly, a Q-enhanced inductor by using the tapped-inductor feedback topology to compensate resistive losses is also presented. Therefore, the developed filter provides three finite transmission zeros to reject undesired interferences while maintains the low-loss passband characteristics. The large-signal characterizations of the circuit are also discussed, revealing the limitation on the filter. Furthermore, the good agreement between measured and simulated results demonstrates the feasibility and application of the low-loss, low-power, and highly-selective BPF design.

ACKNOWLEDGMENT

The authors would like to thank the National Science Council (NSC) and Chip Implementation Chip (CIC) of Taiwan for financial and

technical supports. This work was supported by the NSC under Contract NSC-100-2221-E-027-088-.

REFERENCES

1. Lerdsitsomboon, W. and K. O. Kenneth, "Technique for integration of a wireless switch in a 2.4 GHz single chip radio," *IEEE J. Solid-State Circuits*, Vol. 46, No. 2, 368–377, Feb. 2011.
2. Lee, J., Y.-A. Li, M.-H. Hung, and S.-J. Huang, "A fully-integrated 77-GHz FMCW radar transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, Vol. 46, No. 12, 2746–2756, Dec. 2010.
3. Kwon, I., Y. Eo, H. Bang, K. Choi, S. Jeon, S. Jung, D. Lee, and H. Lee, "A single-chip CMOS transceiver for UHF mobile RFID reader," *IEEE J. Solid-State Circuits*, Vol. 43, No. 3, 729–738, Mar. 2008.
4. Wong, S.-K., F. Kung Wai Lee, S. Maisurah, and M. N. B. Osman, "A wimedia compliant CMOS RF power amplifier for ultra-wideband (UWB) transmitter," *Progress In Electromagnetics Research*, Vol. 112, 329–347, 2011.
5. Shi, X., K. S. Yeo, W. M. Lim, M. A. Do, and C. C. Boon, "A spice compatible model of on-wafer coupled interconnects for CMOS RFICs," *Progress In Electromagnetics Research*, Vol. 102, 287–299, 2010.
6. Cao, Y., R. A. Groves, X. Huang, N. D. Zamdmer, J.-O. Plouchart, R. A. Wachnik, T.-J. King, and C. Hu, "Frequency-independent equivalent-circuit model for on-chip spiral inductors," *IEEE J. Solid-State Circuits*, Vol. 38, No. 3, 419–426, Mar. 2003.
7. Long, J. R. and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," *IEEE J. Solid-State Circuits*, Vol. 32, No. 3, 357–369, Mar. 1997.
8. Wang, S., K.-H. Tsai, K.-K. Huang, S.-X. Li, H.-S. Wu, and C.-K. C. Tzuang, "Design of X-band RF CMOS transceiver for FMCW monopulse radar" *IEEE Trans. on Microw. Theory and Tech.*, Vol. 57, No. 1, 61–70, Jan. 2009.
9. He, X. and W. B. Kuhn, "A 2.5-GHz low-power, high dynamic range self-tuned Q-enhanced LC filter in SOI," *IEEE J. Solid-State Circuits*, Vol. 40, No. 8, 1618–1628, Aug. 2005.
10. Park, E.-C., Y.-S. Choi, J.-B. Yoon, S. Hong, and E. Yoon, "Fully integrated low phase-noise VCOs with on-chip MEMS inductors," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 51, No. 1, 289–296, Jan. 2006.

11. Hsieh, H.-H., Y.-T. Liao, and L.-H. Lu, "A compact quadrature hybrid MMIC using CMOS active inductors," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 55, No. 6, 1098–1104, Jun. 2007.
12. Ler, C. L., A. K. B. A'ain, and A. V. Kordesh, "CMOS source degenerated differential active inductor," *IET Electron. Lett.*, Vol. 44, No. 3, 196–197, Jan. 2008.
13. Zheng, Y. and C. E. Saavedra, "Frequency response comparison of two common active inductors," *Progress In Electromagnetics Research Letters*, Vol. 13, 113–119, 2010.
14. Georgescu, B., I. G. Finvers, and F. Ghannouchi, "2 GHz Q-enhanced active filter with low passband distortion and high dynamic range," *IEEE J. Solid-State Circuits*, Vol. 41, No. 9, 2029–2039, Sept. 2006.
15. Soorapanth, T. and S. S. Wong, "A 0-dB IL 2140 ± 30 MHz bandpass filter utilizing Q-enhanced spiral inductors in standard CMOS," *IEEE J. Solid-State Circuits*, Vol. 37, No. 5, 579–586, May 2002.
16. Kulyk, J. and J. Haslett, "A monolithic CMOS 2368 ± 30 MHz bandpass filter," *IEEE J. Solid-State Circuits*, Vol. 41, No. 2, 362–374, Feb. 2006.
17. Fan, K.-W., C.-C. Weng, Z.-M. Tsai, H. Wang, and S.-K. Jeng, "K-band MMIC active band-pass filters" *IEEE Microw. and Wireless Compon. Lett.*, Vol. 15, No. 1, 19–21, Jan. 2005
18. Chiang, M.-J., H-S. Wu, and C.-K. C. Tzuang, "A 3.7-mW Zero-dB fully integrated active bandpass filter at Ka-band in 0.18-µm CMOS," *IEEE MTT-S Int. Microw. Symp. Dig.*, 1043–1046, Atlanta, GA, Jun. 2008.
19. Huang, K.-K., M.-J. Chiang, and C.-K. C. Tzuang, "A 3.3 mW K-band 0.18-µm 1P6M CMOS active bandpass filter using complementary current-reuse pair," *IEEE Microw. and Wireless Compon. Lett.*, Vol. 18, No. 2, 94–96, Feb. 2008.
20. Wang, S. and R.-X. Wang, "A tunable bandpass filter using Q-enhanced and semi-passive inductors at S-band in 0.18-µm CMOS," *Progress In Electromagnetics Research B*, Vol. 28, 55–73, 2010.
21. Wang, S. and R.-X. Wang, "Q-enhanced CMOS inductor using tapped-inductor feedback," *IET Electron. Lett.*, Vol. 47, No. 16, 921–922, Aug. 2011.
22. Tang, C.-W., C.-W. Shen, and P.-J. Hsieh, "Design of low-temperature co-fired ceramic bandpass filters with modified coupled inductors," *IEEE Trans. on Microw. Theory and Tech.*,

Vol. 57, No. 1, 172–179, Jan. 2009.

23. Tang, C.-W., "Design of four-ordered cross-coupled bandpass filters with low-temperature co-fired ceramic technology," *IET Microw. Antennas & Propag.*, Vol. 3, 402–409, 2009.
24. Yeung, L. K. and K.-L. Wu, "A compact second-order LTCC bandpass filter with finite transmission zeros," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 51, No. 2, 337–341, Feb. 2003.
25. Huang, P.-L., J.-F. Chang, Y.-S. Lin, and S.-S. Lu, "Micromachined V-band CMOS bandpass filter with 2 dB insertion loss," *IET Electron. Lett.*, Vol. 45, No. 2, 100–101, Jan. 2009.
26. Yang, C.-L., S.-Y. Shu, and Y.-C. Chiang, "Analysis and design of a chip filter with low insertion loss and two adjustable transmission zeros using 0.18-μm CMOS technology," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 58, No. 1, 176–184. Jan. 2010.
27. Yang, C.-L., S.-Y. Shu, and Y.-C. Chiang, "Design of K-band chip filter with three tunable transmission zeros using a standard 0.13-μm CMOS technology," *IEEE Trans. on Circuit and Systems-II*, Vol. 57, No. 7, 522–526, Jul. 2010.
28. Zhou, L., S. Liu, Y.-N. Guo, X.-K. Kong, and H. F. Zhang, "A high selectivity quadruple-mode BPF with two short-circuited stub-loaded sirs," *Progress In Electromagnetics Research Letters*, Vol. 24, 43–50, 2011.
29. Wang, S. and B.-Z. Wang, "Design of CMOS active bandpass filter with three transmission zeros," *IET Electron. Lett.*, Vol. 47, No. 20, 1130–1131, Sept. 2011.
30. Georgescu, B., H. Pekau, J. Haslett, and J. McRory, "Tunable coupled inductor Q-enhancement for parallel resonant LC tanks," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 50, No. 10, 705–713, Apr. 2003.
31. Chun, Y.-H., J.-R. Lee, S.-W. Yun, and J.-K. Rhee, "Design of an RF low-noise bandpass filter using active capacitance circuit," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 53, No. 2, 687–695. Feb. 2005.
32. Cheng, K.-K. M. and H.-Y. Chan, "Noise performance of negative-resistance compensated microwave bandpass filter — Theory and experiments," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 49, No. 5, 924–927, May 2005.