

A WIDEBAND CMOS CURRENT-MODE DOWN-CONVERSION MIXER FOR MULTI-STANDARD RECEIVERS

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Abstract—This paper presents a low voltage wideband down-conversion mixer using current-mode approach for multi-standard receivers. The proposed mixer uses a current mirror amplifier with an embedded passive switching core to achieve mixing function, which can combine the advantages of active and passive mixers simultaneously. The mixer is implemented using a 0.18 μm CMOS technology and covers frequency band from 0.5 GHz to 4.0 GHz. A comparison with conventional CMOS down-conversion mixer shows that this current-mode mixer has advantages of large conversion gain, low noise figure and high linearity. Over the entire bandwidth, the mixer features a measured power conversion gain of 8.9 \sim 9.6 dB, a double-sideband (DSB) noise figure of 6.9 \sim 9.3 dB and an input third-order intercept point (IIP3) of 2.0 \sim 5.8 dBm, while consuming 8 mA from a 1.2 V supply voltage. The mixer occupies the active area of 0.43 \times 0.46 mm² including testing pads.

1. INTRODUCTION

Recently different communication standards, such as global system for mobile communications (GSM), wideband code-division multiple access (WCDMA), Bluetooth, wireless local area networks (WLAN) and ultra-wideband communication (UWB), are playing important roles in specific wireless communication fields [1–9]. While the number of standards is still growing, the needs for multi-standard operations which can support various wireless standards have been rapidly increased. The idea of designing a multi-standard communication

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system is definitely fascinating for its low cost and low power consumption. However, building a system suitable for different frequency bands and various requirements would be quite challenging with the advanced CMOS technologies [10–15].

One of the key components in the multi-standard receiving path is the down-conversion mixer [16–19]. A lot of effort has now been spent on the development of wideband radio frequency (RF) CMOS mixers. Active wideband double balanced Gilbert mixer has been the mainstay of integrated multi-standard receiver systems due to their superior conversion gain and good port-to-port isolations performance [20–22]. However, the supply voltage available to Gilbert mixer decreases with CMOS technology scaling, and therefore the issue of voltage headroom and high flicker noise remains in low supply voltage design. Another wideband bulk-injection mixer has been designed with a four-terminal MOS transistor [23, 24]. The RF and local oscillator (LO) signals are applied to the gate and the back gate while the mixing product is extracted from the drain. This kind of mixer can be working on a low supply voltage and low power dissipation, but it suffers from limited gain and relatively poor noise performance. Passive mixer has a great reduction of the flicker noise from the switching core and good linearity performance, but they have conversion loss and require a high LO drive for operation [25, 26]. To generate large LO signals for passive mixer can significantly increase the power consumption of the integrated multi-standard receiver systems. The above RF CMOS mixers are mostly based on voltage-mode operation with frequency of several gigahertz, but some features such as supply voltage, linearity, noise figure or/and conversion gain are not suitable for multi-standard receivers.

As for voltage-mode circuits, the impedance of internal nodes is usually large so that the signal information can be mostly carried with the time-varying voltage signals. Since large enough voltage swing is required to keep signal information, it is difficult for voltage-mode circuits to use reduced voltage headroom under a low supply voltage. Unlike voltage-mode circuits, current-mode circuits have low impedance at internal nodes and signal information is carried by the time-varying current signals. Thus, the voltage at each node can be small, resulting in higher linearity and wider bandwidth. However, linearity and bandwidth requirements have become more stringent as recent wireless systems adopted multi-standard operation. Thus, a current-mode approach can be used to improve the linearity and bandwidth of RF receiver/transmitter front-end operating with a low supply voltage and low power dissipation [27–29].

In this paper, we propose a wideband current-mode down-

conversion mixer covering frequency band from 0.5 GHz to 4.0 GHz. The proposed mixer is based on a current mirror amplifier combined with passive switching core and minimizes the number of passive components. The mixer requires almost no voltage headroom across the passive switching core that works quadrature with the direction of supply voltage. Compared with the previously published active and passive CMOS mixers, the proposed current-mode down-conversion mixer has a similar or better performance in conversion gain, linearity, noise figure and operation bandwidth at a low supply voltage.

The contents of this paper are as follows. In Section 2, the design concept of the novel current-mode mixer is described with operating principles of the current mirror amplifier and passive switching core. The experimental results are reported in Section 3 to verify the performances of the proposed CMOS down-conversion mixer, while the conclusion is summarized in Section 4.

2. CIRCUIT DESCRIPTIONS

Based on the conventional active and passive mixers topology, a wideband current-mode down-conversion mixer is proposed. The current mirror amplifier is used to implement the input and output stages of the mixer, and a passive switching core is embedded between the gates of the input and output transistors of the current mirror to achieve mixing function. The current mirror amplifier and passive switching core are, therefore, merged seamlessly into a single mixer component, as shown in Figure 1. The detailed circuit designs and analyses are presented in the following.

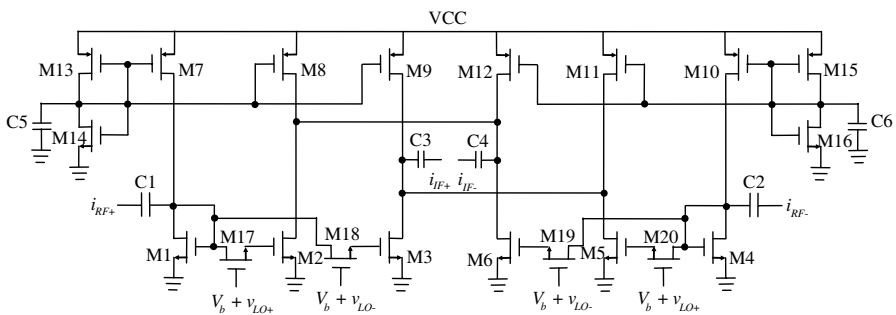


Figure 1. The proposed wideband current-mode down-conversion mixer.

2.1. Current Mirror and Current Mirror Amplifier

In the voltage-mode circuits, the conventional Gilbert mixers convert RF input voltage into current for mixing and then convert the current into voltage for IF output. Thus, there appear two unnecessary voltage-to-current (V-I) and current-to-voltage (I-V) conversions which can cause nonlinearity and power dissipation in the down-conversion mixer. Here, the current mirror amplifier is used for the input and output stages of the current-mode mixer as shown in Figure 2, just like the input transconductance and output load stages of the conventional Gilbert mixer. By using the current mirror amplifier, the output current from the transconductance low noise amplifier (LNA) is directly connected to the input stage of the mixer, and the output current of the mixer is directly connected to the next current-mode filter input. This eliminates a redundant voltage-current-voltage conversion as well as the linearity is hardly affected by voltage swing and headroom.

Shown in Figure 2 is the circuit diagram of the differential current mirror amplifier which is based on the basic current mirror circuit. The current gain relies on the scaling factor of the four basic current mirrors M1-M3 and M4-M6. M7-M9 and M10-M12 work as current sources to bias the current mirrors M1-M3 and M4-M6. The transistors M1-M12 are biased to operate in the saturation region. Both M13-M14 and M15-M16 are diode-connected to provide bias voltage for M7-M9 and M10-M12. C1 and C2 are the dc blocking capacitor. The input differential current signals i_{in+} and i_{in-} are amplified to two pair identical output differential current signals i_{o1+} , i_{o2+} and i_{o1-} , i_{o2-} , where $i_{o1+} = i_{o2+}$ and $i_{o1-} = i_{o2-}$. The current gain of the current

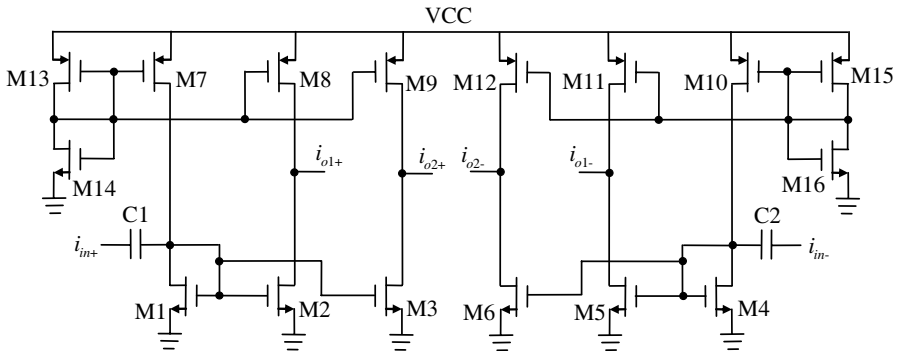


Figure 2. The current mirror amplifier is used for the input and output stages of mixer.

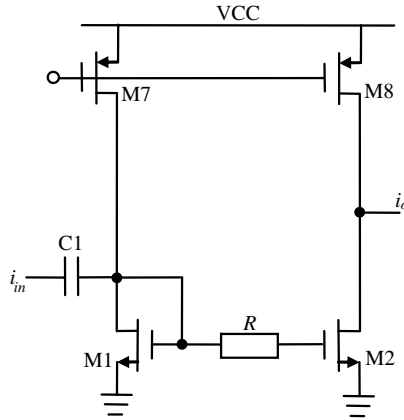


Figure 3. The basic current mirror with the resistive series peaking technique.

mirror amplifier can be easily set through appropriate scaling factor between the current mirror transistors.

To increase the current gain of the current mirror amplifier, the size of the transistors in the output side of the current mirror amplifier can be made large, however, at the cost of reduced bandwidth. Selecting a basic current mirror shown in Figure 3 for analysis, with $R = 0$, has a first-order transfer function. Neglecting the effect of channel length modulation and the high-order effect of MOS transistors, it can be shown that the current gain is given by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m2}}{g_{m1}} \frac{1}{1 + s \frac{C_{gs1} + C_{gs2}}{g_{m1}}} \quad (1)$$

The bandwidth of the basic current mirror is given by

$$\omega_{-3\text{dB}} = \frac{g_{m1}}{C_{gs1} + C_{gs2}} = \frac{g_{m1}}{(1 + N)C_{gs1}} \quad (2)$$

and

$$N = \frac{g_{m2}}{g_{m1}} = \frac{(W/L)_2}{(W/L)_1} \quad (3)$$

where g_{mk} and C_{gsk} ($k = 1, 2$) are the transconductance and gate source capacitance of transistor M_k , respectively. $C_{gs2} \gg C_{gs1}$, $C_{gsk} \gg C_{gdk}$, and C_{gdk} is the gate drain capacitance of transistor M_k . W/L is the channel width to channel length ratio of the MOS transistors and N is the scaling factor of current mirror transistors M1 and M2. Because the scaling factor N is usually large, C_{gs2}

dominates the frequency response, and the bandwidth is given by $\omega_{-3\text{dB}} = g_{m1}/C_{gs2}$ approximately. From Equations (1) and (2), it can be seen that the current gain and bandwidth of the basic current mirror are conflicting design parameters.

As shown in Figure 3, a series peaking resistor R can be embedded between the gates of the input and output transistors of the current mirror. The added series peaking resistor does not affect the supply voltage and the dc biasing conditions of the current mirror, which works quadrature with the direction of supply voltage. The first-order transfer function of the current mirror is then transposed into a second order transfer function with one zero and two poles as given by

$$\frac{I_o(s)}{I_{in}(s)} = \left(\frac{g_{m2}}{g_{m1}} \right) \frac{sRC_{gs1} + 1}{s^2 \frac{RC_{gs1}C_{gs2}}{g_{m1}} + s \frac{C_{gs1} + C_{gs2}}{g_{m1}} + 1}. \quad (4)$$

With one zero as

$$Z_1 = -1/RC_{gs1}. \quad (5)$$

And the two poles are located at

$$p_{1,2} = \frac{C_{gs1} + C_{gs2}}{2RC_{gs1}C_{gs2}} \left[-1 \pm \sqrt{1 - \frac{4RC_{gs1}C_{gs2}g_{m1}}{(C_{gs1} + C_{gs2})^2}} \right]. \quad (6)$$

From a control theory prospective, the value of the series peaking resistor R can exhibit three distinct characteristics of the circuit [30]. In the proposed current-mode down-conversion mixer, R is the on-resistor R_{on} of the passive switching transistor which will be introduced later. By choosing a proper resistor R , the current mirror can achieve two complex conjugate poles separated by $\pi/2$ and a maximally flat bandwidth response, called Butterworth response. The resistive series peaking technique will enhance the bandwidth of the basic current mirror significantly, and maintain the large current gain at the same time.

2.2. Passive Switching Core

The conventional active Gilbert mixer is known to create flicker noise at the crossover point, when the switching transistors are both on and their flicker noise is visible at the output. The flicker noise of the switching transistors is directly proportional to the dc bias current which is commutated by the switching core. Therefore, reducing these dc bias current results in less output flicker noise. This is usually implemented by injecting part of the input transconductor bias current into the tail of the switching core [31–33]. This method has a few drawbacks such as increased white noise level due to the additional

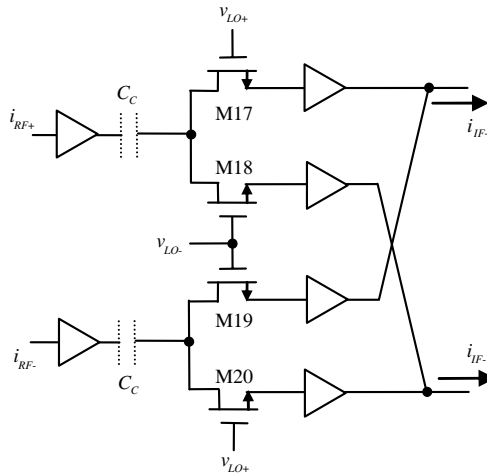


Figure 4. The double balanced current-mode passive switching core.

current source plus linearity degradation. Moreover, reducing the bias current of the active switching core results in a smaller switching transconductance.

An alternative approach is to use a passive switching core, as shown in Figure 4, which allows for a great reduction of the flicker noise from the switching transistors. Setting the commutated dc bias current to zero, instead of just reducing it. This leads us to a passive switching core which only commutates the ac current signal. Passive switching core in Figure 4 consists of four quadrature NMOS transistors M17-M20, driven by the input current signals i_{RF+} and i_{RF-} of the current mirror amplifier and loaded with the output current signals i_{IF+} and i_{IF-} of the current mirror amplifier. Due to the equivalent ac coupling capacitor C_C between the input transconductance of the current mirror amplifier and the passive switching core, the transistors in the passive switching core are operated in the deep triode region with $V_{DS} = 0$. Assume that the transistor gates of the passive switching core are driven by an ideal square wave LO signal, at any instant time, either the switches driven by v_{LO+} or the switches driven by v_{LO-} is on. The main noise sources of the proposed mixer are considered in the analysis: the equivalent transconductance G_m and equivalent output resistance R_{O,G_m} of the input side of the current mirror amplifier, the on-resistance R_{on} of the passive switching transistors (M17-M20), and the equivalent capacitive loading impedance Z_L of the output side of the current mirror amplifier. The main output noise contributions can

be derived as

$$\begin{aligned} \overline{v_{no,G_m}^2} &= 4kT \left(\frac{2}{3} G_m \right) R_{O,G_m}^2 \int \frac{1}{1 + [2\pi f (R_{on} + R_{O,G_m}) Z_L]^2} df \\ &= \frac{2kT G_m R_{O,G_m}^2}{3Z_L (R_{on} + R_{O,G_m})}. \end{aligned} \quad (7)$$

$$\begin{aligned} \overline{v_{no,R_{O,G_m}}^2} &= 4kT R_{O,G_m} \int \frac{1}{1 + [2\pi f (R_{on} + R_{O,G_m}) Z_L]^2} df \\ &= \frac{kT R_{O,G_m}}{Z_L (R_{on} + R_{O,G_m})}. \end{aligned} \quad (8)$$

$$\begin{aligned} \overline{v_{no,R_{on}}^2} &= 4kT R_{on} \int \frac{1}{1 + [2\pi f (R_{on} + R_{O,G_m}) Z_L]^2} df \\ &= \frac{kT R_{on}}{Z_L (R_{on} + R_{O,G_m})}. \end{aligned} \quad (9)$$

Because of the finite equivalent output resistance R_{O,G_m} of the current mirror amplifier, the noise contribution of the on-resistance R_{on} of the switching transistors is not zero, but negligible from Equation (9) when the on-resistance R_{on} is much smaller than the equivalent output resistance R_{O,G_m} of the current mirror amplifier. In the proposed current-mode down-conversion mixer, different equivalent noise sources are typically uncorrelated and $R_{O,G_m} \gg R_{on}$, so the on-resistance R_{on} of the switching transistors is not the dominant noise contributor in the current-mode mixer. On the other hand, from the later simulation of the current mirror amplifier with and without the embedded passive switching transistors, it also reveals that the noise contributions of the current-mode mixer due to G_m and R_{O,G_m} are dominant, just like the noise of the current mirror amplifier. Meanwhile, operating the passive switching core in the current-mode domain improves linearity, since it reduces the distortion caused by large voltage swing at the source and drain of the switching transistors. Such large voltage swing occurs in both active Gilbert mixers and voltage-mode passive mixers. Moreover, no dc bias current is required in the passive switching core and low power dissipation can be achieved.

2.3. Circuit Design

The circuit diagram of the proposed wideband CMOS current-mode down-conversion mixer is shown in Figure 1. The current mirror amplifier as the input and output stages of the mixer, is consist of the four basic current mirrors M1-M3 and M4-M6. Through the current mirror amplifier, the input RF current signals i_{RF+} and i_{RF-} are

directly down-converted to the output IF current signals i_{IF+} and i_{IF-} by mixing with LO signals. The LO signals are achieved by passive switching core M17-M20 which is embedded between the input and output side of the current mirror amplifier. The passive switching core is double balanced topology with the advantages of rejecting the feedthrough of LO and RF signals and the even-order distortion products. The dc bias voltage V_b at the gate of the transistors M17-M20 switches two pair of transistors in such a way that for one half-cycle input is connected to the output directly and for another half-cycle with opposite polarity, and the conversion gain of the passive switching core is theoretically equal to $2/\pi$ [34]. When the RF signals $i_{RF\pm}(t) = \pm I_{RF} \cos \omega_{RF} t$ and LO signals $v_{LO\pm}(t) = \pm V_{LO} \cos \omega_{LO} t$ are applied, the switching action generates a down-converted signal which is same as that the RF current is multiplied by a square wave. Equation (10) describes the multiplication process of the current-mode mixer as

$$\begin{aligned}
 i_{IF} &= i_{IF+} - i_{IF-} = N \times (i_{RF+} - i_{RF-}) \times \text{square} [\cos(\omega_{LO} t)] \\
 &= 2N \times I_{RF} \cos(\omega_{RF} t) \times \frac{2}{\pi} \left[\cos(\omega_{LO} t) + \frac{1}{3} \cos(3\omega_{LO} t) + \dots \right] \\
 &= \frac{2N \times I_{RF}}{\pi} \cos(\omega_{RF} - \omega_{LO}) t + \frac{2N \times I_{RF}}{\pi} \cos(\omega_{RF} + \omega_{LO}) t \\
 &\quad + \frac{2N \times I_{RF}}{3\pi} \cos(\omega_{RF} \pm 3\omega_{LO}) t + \dots
 \end{aligned} \tag{10}$$

This expression is the same as that of the conventional double balanced active Gilbert mixer. From Equation (10), the double sideband mixing is achieved and the signal at ω_{RF} is converted into the signals at $\omega_{RF} - \omega_{LO}$ and at $\omega_{RF} + \omega_{LO}$. The ω_{IF} in this design is set to $\omega_{RF} - \omega_{LO}$. Besides, On-chip capacitors (C1-C4) are applied to be the dc-blocking capacitors to isolate the input or output ports from the dc source. C5-C6 is the on-chip filtering capacitors to lower the noise induced by the supply voltage, which can be used to maintain a constant bounce between VCC and ground.

In the proposed current-mode down-conversion mixer, there are several advantages. Firstly, it has only two stacked transistors connected between the supply voltage and ground rails. Here, the direction of the passive switching core is quadrature with the direction of supply voltage. It requires no voltage headroom across the passive switching core, so that the full supply voltage headroom can be reserved for the current mirror amplifier. Thus the constraint on the upper limit of supply voltage can be avoided. Secondly, the on-resistor R_{on} of the passive switching transistors is sized based on the criterion that a fast switching response and the maximum

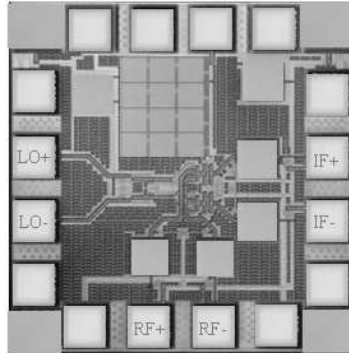


Figure 5. Photomicrograph of the proposed mixer with the size of $0.43 \times 0.46 \text{ mm}^2$.

bandwidth simultaneously. As demonstrated in the Section 2.1, when properly valued the size of passive switching transistors, the on-resistor R_{on} helps increase the bandwidth of the mixer by canceling out the dominant pole with a compensating zero. Thirdly, no inductor is needed in the proposed mixer, which is another added advantage of this design.

3. MEASURED RESULTS AND DISCUSSION

The proposed wideband current-mode down-conversion mixer has been realized using a TSMC $0.18 \mu\text{m}$ single-poly six-metal CMOS technology, and simulated using Cadence SpectreRF simulator. A photomicrograph of the fabricated current-mode down-conversion mixer is shown in Figure 5. The die size of the test chip is only $0.43 \times 0.46 \text{ mm}^2$ including testing pads. The PCB testing board has been built by directly bonding the chip on a two-layer FR4 substrate. To make sure that the input signal can be injected into the proposed mixer and reduce the signal distortion, an input matching network at RF and LO ports are constructed using external surface mount components; while external passive baluns are used to convert the single-ended signals into fully differential signals or vice versa. All following measurements are done with a spectrum analyzer or a network analyzer both of which have 50 Ohm port. The gain and power loss caused by the off-chip baluns and bonding wires have been de-embedded from the measurement.

The measured RF port input return loss is better than -13 dB across the whole desired frequency range from 0.5 GHz to 4.0 GHz .

Hence, the input impedance in the RF port can easily be matched to 50 Ohm over a wide bandwidth. Fixing the IF frequency to 100 MHz, the measured power conversion gain variations of the mixer as a function of LO power are shown in Figure 6. The RF frequency is set to be 2.5 GHz, and the LO power is chosen to be 2 dBm to achieve the maximum power conversion gain of 9.6 dB. The measured results at different RF frequencies are performed with a LO power of 2 dBm. The circuit shows a power conversion gain of 8.9 ~ 9.6 dB from 0.5 GHz to 4.0 GHz as shown in Figure 7, which shows a large RF bandwidth of 3.5 GHz. Apart from the IF frequency at 100 MHz, the power conversion gain of the mixer as a function of IF frequencies for various RF frequency are also measured. As shown in Figure 8, the power conversion gains versus IF frequencies show a flat frequency response with a less than 1 dB variation from 1 MHz to 500 MHz.

When characterizing the noise performance of a mixer, either

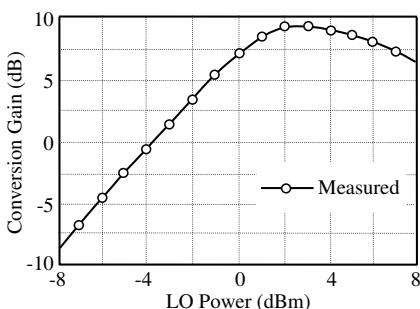


Figure 6. Measured power conversion gain versus LO power.

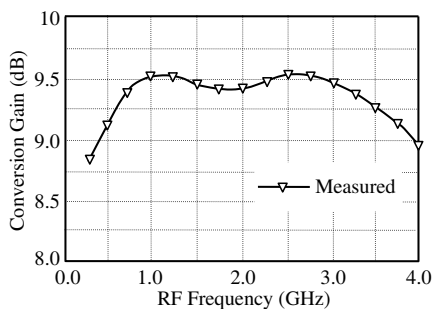


Figure 7. Measured power conversion gain versus RF frequency.

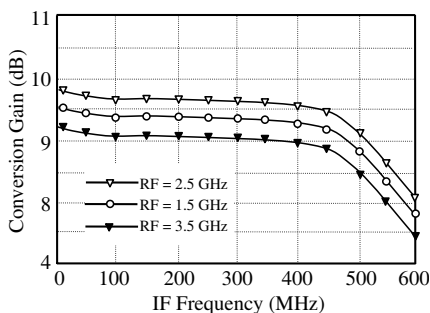


Figure 8. Measured power conversion gain versus IF frequency.

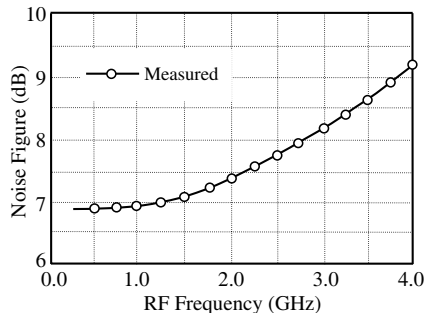


Figure 9. Measured DSB noise figures against RF frequency.

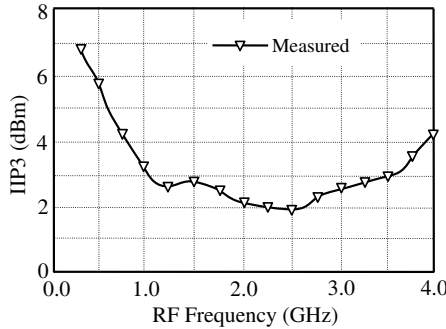


Figure 10. The measured IIP3 of the mixer as a function of the RF frequency.

the double-sideband or single-sideband noise figure (NF) can be used. Figure 9 shows the measured double-sideband NF of the mixer against RF frequency from 0.5 GHz to 4.0 GHz. This mixer has a low and relatively flat NF across a large 3.5 GHz bandwidth. It shows that NF below 9.3 dB can be achieved up to 4.0 GHz. The minimum double-sideband NF is 6.9 dB at 0.5 GHz and the maximum double-sideband NF is 9.3 dB at 4.0 GHz, with an average of 8.1 dB across the entire frequency range.

At a RF frequency of 2.5 GHz, a two-tone inter-modulation power measurement of the mixer with a frequency spacing of 10 MHz is measured, which features an input third-order intercept point (IIP3) of 2.0 dBm and an input 1 dB compression point ($P_{1\text{dB}}$) of greater than -7.8 dBm. With the fixed LO power at 2 dBm, the measured IIP3 of the down-conversion mixer varies from 5.8 dBm to 2.0 dBm when the RF frequency increases from 0.5 GHz to 4.0 GHz, as shown in Figure 10. From the comparisons below, this results validate that good linearity can be obtained using the current-mode approach.

Meanwhile, the measured LO-to-IF, LO-to-RF, and RF-to-IF isolations from 0.5 GHz to 4.0 GHz are better than -45 dB, -50 dB and -48 dB, respectively (not shown here). It can be found that the current mirror amplifier combined with passive switching core in the proposed double balanced mixer topology have a good port-to-port isolations performance. Besides, the current consumption of the mixer is 8 mA at the supply voltage of 1.2 V, which results in a power consumption of 9.6 mW. Because this mixer architecture is scalable in term of the supply voltage, the proposed mixer can be expected to offer smaller power consumption with CMOS technology scaling, such as 90 nm and 65 nm CMOS technology.

Table 1. Performance summaries of the proposed mixer and comparison with other work.

Reference	Technology (μm)	Frequency (GHz)	Conversion gain (dB)	DSB NF (dB)
[20]	0.18 CMOS	2.3–5.8	3.7	16.2
[21]	0.18 CMOS	0.2–16	6.4	-
[23]	0.18 CMOS	0.5–7.5	5.7	15
[31]	0.065 CMOS	1.0–10.5	14.5	6.5
[32]	0.18 CMOS	5.2	5.8	13
[33]	0.18 CMOS	5.8	7.5	10.9
This work	0.18 CMOS	0.5–4.0	9.6	6.9

Reference	IIP3 (dBm)	Supply voltage (V)	Power dissipation (mW)	Area (mm^2)
[20]	7.4	1.8	8.3	-
[21]	-6	1.8	15	0.68×0.65
[23]	-5.7	0.77	0.48*	0.86×0.72
[31]	-3.8	1.2	14.4	0.57×0.37
[32]	-6	1.0	3.8*	1.04×1.10
[33]	-5	1.8	8.1	0.88×0.88
This work	5.8	1.2	9.6	0.43×0.46

*The result is not included the output buffers dissipation.

The overall measured performance of the wideband current-mode down-conversion mixer is summarized in Table 1, where comparisons with other published designs are also provided. From Table 1, the proposed current-mode down-conversion mixer combines the advantages of both an active mixer and a passive mixer such as large conversion gain and low noise figure with high linearity while, at the same time, meets the requirement of wideband operations.

4. CONCLUSION

A wideband CMOS down-conversion mixer using current-mode approach is demonstrated in this paper. It commutates the ac current of the input side current mirror amplifier through the passive switching core, and passes it to the output side of the current mirror amplifier, which realizes the function of mixing. The intrinsic large bandwidth and high linearity of the current mirror amplifier and the low flicker noise of the passive switching core are maintained in the

proposed current-mode mixer. From 0.5 GHz to 4.0 GHz, this mixer has a maximum power conversion gain of 9.6 dB, a minimum double-sideband noise figure of 6.9 dB and an IIP3 of better than 2.0 dBm, while consumes 8 mA from a 1.2 V supply voltage. This performance is obtained without using inductor hence making this current-mode solution extremely compact and suitable for multi-standard receivers.

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