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BEHAVIORAL MODEL OF SYMMETRICAL MULTI-LEVEL T-TREE INTERCONNECTS

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Abstract—An accurate and behavioral modeling method of symmetrical T-tree interconnect network is successfully investigated in this paper. The T-tree network topology understudy is consisted of elementary lumped L-cells formed by series impedance and parallel admittance. It is demonstrated how the input-output signal paths of this single input multiple output (SIMO) tree network can be reduced to single input single output (SISO) network composed of L-cells in cascade. The literal expressions of the currents, the input impedances and the voltage transfer function of the T-tree electrical interconnect via elementary transfer matrix products are determined. Thus, the exact expression of the multi-level behavioral T-tree transfer function is established. The routine algorithm developed was implemented in Matlab programs. As application of the developed modeling method, the analysis of T-tree topology comprised of different and identical RLC-cells is conducted. To demonstrate the relevance of the model established, lumped RLC T-tree networks with different levels for the microelectronic interconnect application are designed and simulated. The work flow illustrating the guideline for the application of the routine algorithm summarizing the modeling method is proposed. Then, 3D-microstrip T-tree interconnects with width 0.1 μm and length 3 mm printed on FR4-substrate were considered. As results, a very good agreement between the results from the reduced behavioral model proposed and SPICE-computations is found both in frequency- and time-domains by considering arbitrary binary sequence "01001100" with 2 Gsym/s rate. The model proposed in this paper presents significant benefits in terms of flexibility and very less computation times. It can be used during the design process of the PCB and the microelectronic circuits for the signal integrity prediction. In the continuation of this

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work, the modeling of clock T-tree interconnects for packaging systems composed of distributed elements using an analogue process is in progress.

1. INTRODUCTION

Since the invention of the integrated circuits (ICs) by Jack S. Kilby from Texas Instruments [1], the mankind way of life has been increasingly conditioned by the evolution of electronic systems toward the use of personal computers and multifunction mobile gadgets. To meet this spectacular progress, high performance reconfigurable processors and ultra-high speed wired and wireless communicating systems operating up to tens of GHz were deployed [2–9]. Due to the unceasing increase of the electronic system integration, the modern high-speed electronic equipment meets different technological roadblocks due to the interconnect complexity [10–15]. In addition to the investigation on the apparition of electromagnetic interferences (EMI) and electromagnetic compatibility (EMC), many works stating the power loss and the interconnect delay effects for example, in the RF/digital devices were done [6, 16–23]. Because of the undesired interconnection perturbations, it has been evidenced that the interconnect delays of high speed digital IC dominate widely gate delays [5]. During the data stream transmission, these technological issues can be sources of signal distortions, asynchronous effects of the transmitted analog signals and erroneous symbols. So, intensive researches were performed on the modeling of the interconnect networks in order to predict the signal integrity (SI) [9, 11–15, 17–24]. To minimize the cost and energy consumption and also for sharing data and clock signals through multipath circuits can be composed of ICs packaged in different levels this later is fundamental [25–28]. In this optic, different topologies as a typical H-tree interconnect [17, 25] were investigated. Figure 1 shows the implementation of the H-tree structure with four levels as a typical surface-layout used in Caltech SCORE [4] and Quicksilver's ACM [8].

In order to deal with the bottleneck caused by the interconnect imperfection, intensive researches for the enhancements of on-chip interconnect have been conducted [29–36]. Different techniques enabling VLSI interconnect optimization have been deployed. For example, with various topological approaches for wire sizing and crosstalk optimizations, signal path algorithms (Steiner tree algorithm, Greedy-BST/DME algorithm, planar-clock routing) and classical models have been explored [24]. By exploiting the moment matching of the transfer response, simulation technique of the high-speed clock

tree is presented by considering buffer insertions. But as reported succinctly in [29], such a technique is more adapted to the lumped tree network with few numbers of cells. Moreover, topologies of on-chip interconnects with arbitrary numbers of levels is presented [30]. Thus, by deeming with MOS distribution networks, optimized computation techniques of clock-tree level have been introduced for mixed-system [31]. In other hand, based on the investigation of row and input flit width in compiled message, a modeling method of hardware performance analysis with Hamming product codes is presented in [32] for the improvement of on-chip interconnect energy. Moreover, new characterization method of serial link bus delay in mobile terminal antennas operating at multi-gigabits speed is described in [33]. Furthermore, a correction method of interconnect degradation by using active circuits with negative group delay is introduced in [34–36].

To estimate the SI parameters as the interconnect delay, the most popular method is based on the use of RC-models as introduced by Elmore in 1948 [37]. The main advantage of this model lies on its simplicity and its possibility for fast delay estimation when considering sophisticated signal paths of integrated system. However, its drawback consists on its high imprecision compared to other high order delay models. It was reported that Elmore model can involve to more than 30% relative errors [38, 39]. For this reason, more accurate approximated second order RLC model were developed in [39–41]. Furthermore, as developed in [39, 40], authors determine the step unit response of lumped RLC tree networks via second moments of the polynomial transfer function. The main advantage of this second order delay model is that it enables to investigate the signal delay with good accuracy even for non-monotone time-domain responses. Till now, most of employed algorithms and modeling methods for computing the transient responses induced by lumped tree mesh networks are calculated from the sum of the estimated polynomial transfer function between the branches of different nodes [17, 25, 41–48]. In [48–50], more general modeling approach enabling to predict the UWB responses of microstrip interconnections is proposed. With the increase of the circuit complexity, the interconnections are more and more complex as the case of tree networks [41–48]. But accurate and more relevant models are still needed for the multilevel T-tree interconnections as proposed in [51, 52].

In order to face out this technical limitation, an accurate reduced method for extracting the behavioral transfer function of multi-level T-tree networks is developed in this paper. It is organized in four different sections. In Section 2, a general topology of symmetrical T-tree

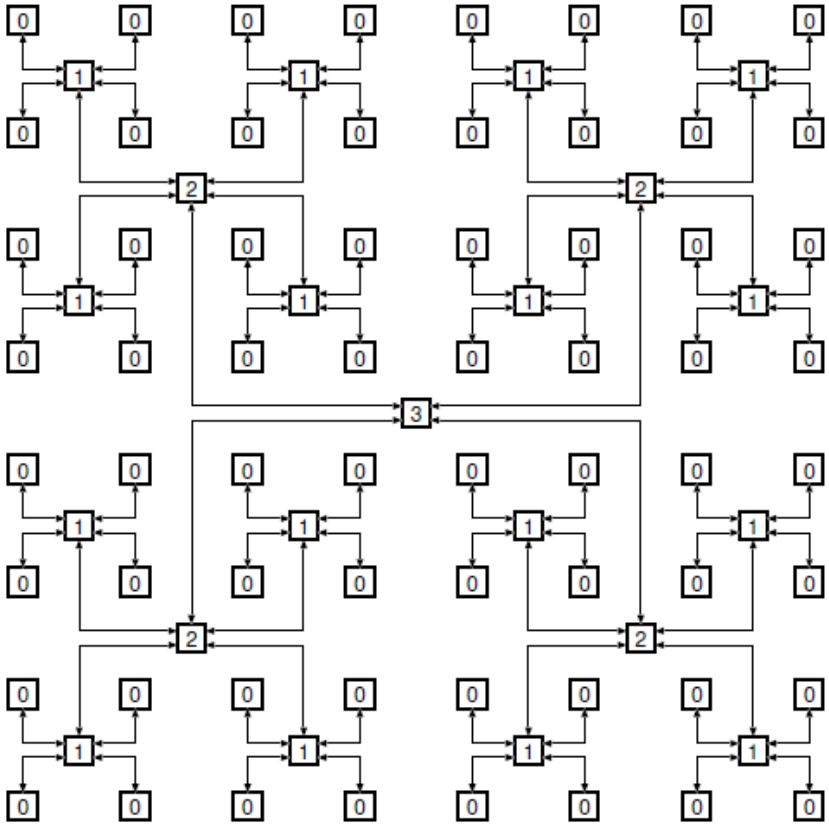

Figure 1. H-tree with four levels [4, 8, 17, 25].

networks consisted of lumped L-cells is analyzed. The transformation of this typical single input multiple output (SIMO) circuit to single input single output (SISO) networks is established. By using the Transfer matrix operation and analysis, the mathematical expression of the whole network transfer function is developed. Section 3 is focused on the particular application based on the characterization of the T-tree networks comprised of different and identical RLC-cells. With the transfer function model, an estimation of the whole tree signal attenuation will be provided. To check the efficiency of the analytical formulae established, comparative studies between the models developed and SPICE-computations based on realistic examples of T-tree interconnect structures will be made in Section 4. Lastly, concluding remarks will be drawn in Section 5.

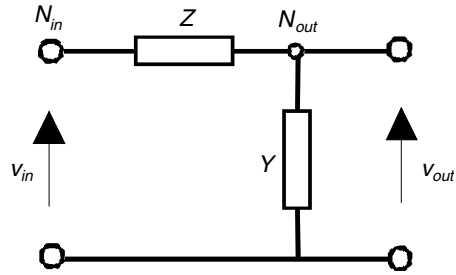

Figure 2. Unit L-cell formed by Z-series impedance and Y-parallel admittance.

2. GLOBAL MODELING OF LUMPED TREE DISTRIBUTION

Before the examination of the most important parts of this paper which is mainly focused on the T-tree electrical network modeling methodology, the clarification of the preliminary fundamental theory used along the study is presented in the following subsection.

2.1. Basic Theory on the L-cell Circuit

For the beginning, let us consider the unit L-cell composed of Z-series impedance and Y-parallel admittance depicted in Figure 2. This fundamental circuit which behaves as a passive four-terminal network is excited by the input voltage v_{in} at the node N_{in} and generates an output voltage v_{out} at the node N_{out}.

According to the circuit and system theory, it is well known that the Transfer matrix of the L-cell shown in Figure 2 is merely written as:

$$[T] = \begin{bmatrix} 1 + Z \cdot Y & Z \\ Y & 1 \end{bmatrix}. \tag{1}$$

The expressions of the transfer function $H(s)$ and the input impedance $Z_{in}(s)$ associated to this Transfer matrix are written as:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{T_{11}} = \frac{1}{1 + Z \cdot Y}, \tag{2}$$

$$Z_{in}(s) = \frac{T_{11}}{T_{21}} = Z + \frac{1}{Y}, \tag{3}$$

where s is the Laplace variable. A mathematical analogy related to these elementary relations will serve us for the proposed

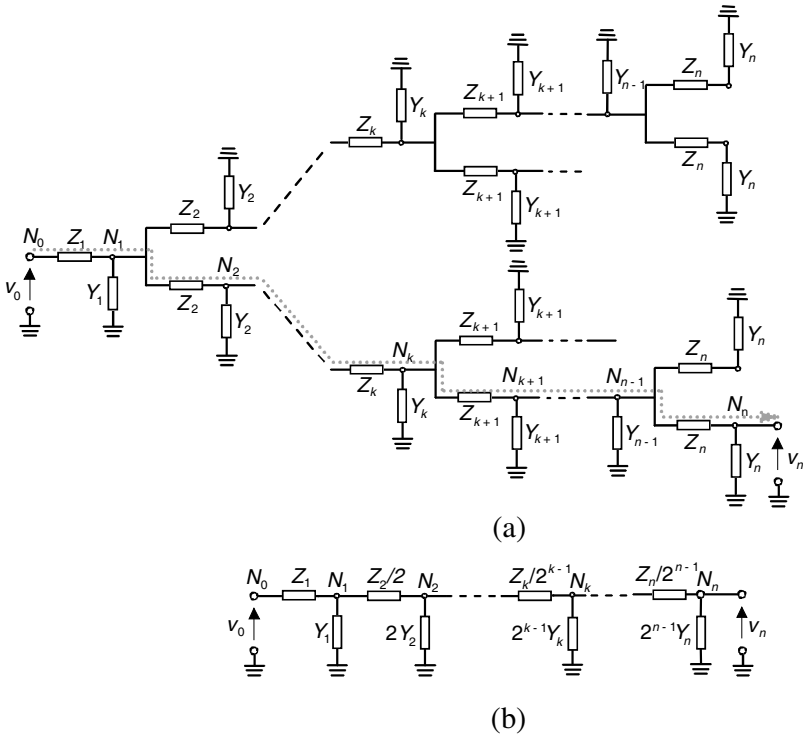

Figure 3. (a) Symmetrical tree network composed of different cells formed by Z_k-series impedance and Y_k-parallel admittance ($k = \{1 \dots n\}$) and (b) its reduced electrical SISO-circuit equivalent to the grey dashed signal path.

characterization of multi-level global T-tree network formed by L-cell in the next subsections.

2.2. Analysis Proposed for the Modeling of T-tree Networks Composed of Different L-cells

Along this paper, the topological analysis of multi- or n-level symmetrical lumped T-tree distribution as a single input multiple output (SIMO) system is focused on the representation introduced in Figure 3(a). One can see that at each node N_k ($k = \{1 \dots (n-1)\}$), two identical L-cells are connected in parallel. So, according to the voltage division rule, the input equivalent impedance $Z_{eq}(k)$ seen at node N_k is the half of the input impedance of the next branch $Z_{eq}(k) = Z_{in}(k)/2$. Similarly, the equivalent admittance is the double

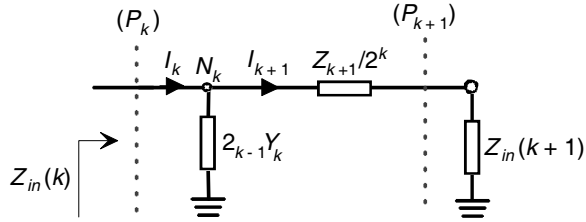

Figure 4. Basic cell at the kth-stage of the reduced circuit shown in Figure 3(b).

of the input admittance of the next branch, $Y_{eq}(k) = 2Y_{in}(k)$. This finding explains the electrical equivalence between the branch N_0N_n of Figure 3(a) as traced in grey dashed path and the single input single output (SISO) circuit depicted in Figure 3(b).

As highlighted in Figure 4, between the consecutive planes (P_k) and (P_{k+1}), the piece of circuit connected in the branch (N_kN_{k+1}) is formed by L-cell having $Z_{k+1}/2^k$-series impedance and 2^kY_{k+1}-parallel admittance. For the sake of simplification, the input current and the input impedance seen at the plane (P_k) are respectively, denoted by I_k and $Z_{in}(k)$. By considering the circuit of Figure 3(b), the input impedance seen at the node N_n which is located at the whole network termination is equal to $Z_{in}(n) = 1/(2^{n-1}Y_n)$. Based on the equivalent impedance calculation applied to the basic cell shown in Figure 4, it is known that the input impedance $Z_{in}(k)$ seen at the node N_k is equal to $(2^{1-k}/Y_k)/[Z_{k+1}/2^k + Z_{in}(k+1)]$. So that, for $k = \{1 \dots n\}$, the partial input impedance $Z_{in}(k)$ can be expressed as:

$$Z_{in}(k) = \begin{cases} \frac{2^{-k}Z_{k+1}+Z_{in}(k+1)}{1+2^{k-1}Y_k\left[2^{-k}Z_{k+1}+Z_{in}(k+1)\right]}, & \text{if} \quad k \leq n-1 \\ \frac{1}{2^{n-1}Y_n}, & \text{if} \quad k = n \end{cases} . \tag{4}$$

The current divider principle applied again to the piece of circuit shown in Figure 4 enables to write the expression of current I_k flowing through electrical branch $N_{k-1}N_k$ for $k = \{2 \dots n\}$. For the initial case $k = 1$, I_1 can be determined directly with Ohm's law. Therefore, the general expression of the current, I_k is given by:

$$I_{k+1} = \begin{cases} \frac{V_i}{Z_{in}(1)+Z_1}, & \text{if} \quad k = 0 \\ \frac{I_k}{1+2^{k-1}Y_k\left[2^{-k}Z_{k+1}+Z_{in}(k+1)\right]}, & \text{if} \quad k \geq 1 \end{cases} . \tag{5}$$

By denoting $[T_{k-1}]$ the elementary Transfer matrix of the $(k-1)$-th cell in the branch $N_{k-1}N_k$, similarly to the basic equation of L-cell Transfer matrix expressed earlier in (1), one surmises the following

formulation:

$$[T_{k-1}] = \begin{bmatrix} 1 + Z_k \cdot Y_k & \frac{Z_k}{2^{k-1}} \\ 2^{k-1} Y_k & 1 \end{bmatrix}. \tag{6}$$

Subsequently, the association of n-cells in cascade represented in Figure 4 should generate a global whole Transfer matrix equal to the product of $[T_{k-1}]$ when $k = \{1 \dots n\}$. In the remainder of the paper, the whole Transfer matrix corresponding to the reduced matrix of the first branch of a n-branch clock-tree is denoted $[T_{1,n}]$. According to the equivalent reduced circuit of Figure 3(b), it is mathematically defined as:

$$[T_{1,n}] = \prod_{k=1}^{k=n} \begin{bmatrix} 1 + Z_k \cdot Y_k & \frac{Z_k}{2^{k-1}} \\ 2^{k-1} Y_k & 1 \end{bmatrix}. \tag{7}$$

This matrix product explains that the voltage global transfer function denoted $H_n(s)$ corresponding to this matrix must be calculated recursively from the last elementary matrix $[T_{k,n}]$. Though, the latter can be determined progressively via the following matrix recursive relation:

$$[T_{k-1,n}] = \begin{cases} [T_k] & \text{for} \quad k = n \\ [T_{k,n}] \cdot [T_{k-1}] & \text{for} \quad k < n \end{cases}. \tag{8}$$

For more explicit representation of literal expressions, in the next part of this paper, $[T_{1,k}]$ will be expressed as follows:

$$[T_{1,k}] = \begin{bmatrix} T_{11}(k) & T_{12}(k) \\ T_{21}(k) & T_{22}(k) \end{bmatrix}. \tag{9}$$

By combining former Equations (6), (8) and (9), and varying the integer k from 0 to $(n-1)$, the following recursive relations between the two elements T_{11} and T_{21} of matrices $[T_{1,k-1}]$ and $[T_{1,k}]$ are established:

$$T_{11}(k) = \begin{cases} (1 + Z_k \cdot Y_k) T_{11}(k+1) + 2^{1-k} Z_k \cdot T_{21}(k+1) & \\ & \text{for} \quad 1 \le k < n \\ 1 + Y_n \cdot Z_n & \text{for} \quad k = n \end{cases}, \tag{10}$$

$$T_{21}(k) = \begin{cases} 2^{k-1} Y_k T_{11}(k+1) + T_{21}(k+1) & \text{for} \quad 1 \le k < n \\ 2^{n-1} Y_n & \text{for} \quad k = n \end{cases}. \tag{11}$$

Accordingly, through successive calculations from the output termination of cascaded network presented in Figure 3, the following partial transfer function is yielded:

$$H_{n-k}(s) = \frac{V[N(n)]}{V[N(k)]} = \frac{1}{T_{11}(k)}. \tag{12}$$

At noted that this partial transfer function is also equal to the whole transfer function of n-level tree distribution, $H_n(s)$ if $k = 0$. Hence,

knowing $[T_{1,n}]$, the global transfer function with the following relation can be deduced:

$$H_n(s) = \frac{V[N(n)]}{V[N(0)]} = \frac{1}{T_{11}(n)}. \tag{13}$$

Using the latter and by taking into account recursive relations (10) and (11), literal analytical calculations were established for the four transfer functions corresponding to $n = \{1 \dots 4\}$. Therefore, the literal expressions of $H_n(s)$ are addressed in Table 1 according to the lumped tree network formed by different Z_kY_k-cells for $k = \{1 \dots n\}$.

2.3. Analysis of T-tree Interconnect Network with Identical L-cells

As particular case of previous study, in this subsection, the T-tree interconnect network with identical L-cells is investigated by taking $Z_k = Z$ and $Y_k = Y$ for all the values of integer k. In this case, expression (4) of the input impedance, $Z_{in}(k)$ seen at the plan (P_k) becomes:

$$Z_{in}(k) = \begin{cases} 2^{1-k}Z + \frac{Z_{in}(k+1)}{1+2^{k-1}\cdot Y\cdot Z_{in}(k+1)}, & \text{if} \quad k \leq n-1 \\ \frac{1}{2^nY}, & \text{if} \quad k = n \end{cases}. \tag{14}$$

The expression of current I_k flowing through the electrical branch $N_{k-1}N_k$ induced from Equation (8) will be transformed as:

$$I_{k+1} = \begin{cases} \frac{V_i}{Z+Z_{in}(1)}, & \text{if} \quad k = 0 \\ \frac{I_k}{1+2^{k-1}Y\cdot Z_{in}(k+1)}, & \text{if} \quad k \geq 1 \end{cases}. \tag{15}$$

Moreover, the elementary Transfer matrix of the $(k-1)$-th cell which constitutes the branch $N_{k-1}N_k$ will be simplified as:

$$[T_{k-1}] = \begin{bmatrix} 1 + Z\cdot Y & \frac{Z}{2^{k-1}} \\ 2^{k-1}Y & 1 \end{bmatrix}. \tag{16}$$

Table 1. Transfer functions of L-cell tree networks for $n = \{1 \dots 4\}$.

n	Transfer function, $H_n(s)$
1	$H_1(s) = \frac{1}{1+Z_1Y_1}$
2	$H_2(s) = \frac{1}{(1+Z_1Y_1)(1+Z_2Y_2)+2Z_1Y_2}$
3	$H_3(s) = \frac{1}{(1+Z_1Y_1)[(1+Z_2Y_2)(1+Z_3Y_3)+2Z_2Y_3]+2Z_1[Y_2(1+Z_3Y_3)+2Y_3]}$
4	$H_4(s) = \frac{1}{(1+Z_1Y_1)[(1+Z_2Y_2)[(1+Z_3Y_3)(1+Z_4Y_4)+2Z_3Y_4] +2Z_2[Y_3(1+Z_4Y_4)+2Y_4]]+Z_1[2Y_2[(1+Z_3Y_3)(1+Z_4Y_4) +2Z_3Y_4]+4Y_3(1+Z_4Y_4)+8Y_4]}$

It implies that the equivalent whole transfer matrix, $[T_{1,n}]$ expressed in (7) will become:

$$[T_{1,n}] = \prod_{k=1}^{k=n} \begin{bmatrix} 1+ZY & \frac{Z}{2^{k-1}} \\ 2^{k-1}Y & 1 \end{bmatrix}. \tag{17}$$

Hence, previous recursive relations (10) and (11) governing the two elements of the $[T_{1,k-1}]$-matrix will be expressed as follows:

$$T_{11}(k-1) = (1+Z\cdot Y)T_{11}(k) + 2^{-k+1}Z\cdot T_{21}(k), \tag{18}$$

$$T_{21}(k-1) = 2^{k-1}Y\cdot T_{11}(k) + T_{21}(k). \tag{19}$$

The elements of the last transfer matrix, $[T_n]$ introduced in (10) and (11) become:

$$T_{11}(n) = 1 + Y\cdot Z, \tag{20}$$

$$T_{21}(n) = 2^{n-1}Y. \tag{21}$$

Owing to these four last expressions, literal analytical calculations were realized for the six transfer functions of n-level tree network comprised of identical L-cells for $n = \{1\dots 6\}$. Table 2 addresses the analytical results calculated. Furthermore, according to expression (14), the input impedance literal expressions exposed in Table 3 are derived.

Table 2. Transfer functions of L-cell tree networks formed by Z-series impedance and Y-parallel admittance for $n = \{1\dots 6\}$.

n	Transfer function, $H_n(s)$
1	$H_1(s) = \frac{1}{1+ZY}$
2	$H_2(s) = \frac{1}{1+4ZY+Z^2Y^2}$
3	$H_3(s) = \frac{1}{1+11ZY+7Z^2Y^2+Z^3Y^3}$
4	$H_4(s) = \frac{1}{1+26ZY+30Z^2Y^2+10Z^3Y^3+Z^4Y^4}$
5	$H_5(s) = \frac{1}{1+57ZY+102Z^2Y^2+58Z^3Y^3+13Z^4Y^4+Z^5Y^5}$
6	$H_6(s) = \frac{1}{1+120ZY+303Z^2Y^2+256Z^3Y^3+95Z^4Y^4+16Z^5Y^5+Z^6Y^6}$

3. T-TREE MODELING WITH LUMPED RLC-NETWORK

By taking $Z_k = R_k + L_k s$ and $Y_k = C_k s$, the modeling method of previous Subsection 2.2 can be transposed to the theoretical analysis of the $R_kL_kC_k$-tree network distribution ($k = \{1\dots n\}$).

Table 3. Input impedances, Z_{in} $(k+1)$ seen at the plan, (P_k) for n-cell tree networks formed by Z-series impedance and Y-parallel admittance.

n	Input impedance, $Z_{in}(N_k)$
1	$Z_n(s) = \frac{1+ZY}{2^{n-1}Y}$
2	$Z_{n-1}(s) = \frac{1+4ZY+Z^2Y^2}{2^{n-2}Y(3+ZY)}$
3	$Z_{n-2}(s) = \frac{1+11ZY+7Z^2Y^2+Z^3Y^3}{2^{n-3}Y(7+6ZY+Z^2Y^2)}$
4	$Z_{n-3}(s) = \frac{1+26ZY+30Z^2Y^2+10Z^3Y^3+Z^4Y^4}{2^{n-4}Y[(1+ZY)(3+ZY)(5+ZY)]}$
5	$Z_{n-4}(s) = \frac{(1+ZY)(1+56ZY+46Z^2Y^2+12Z^3Y^3+Z^4Y^4)}{2^{n-5}Y[31+72ZY+48Z^2Y^2+12Z^3Y^3+Z^4Y^4]}$
6	$Z_{n-5}(s) = \frac{1+120ZY+303Z^2Y^2+256Z^3Y^3+95Z^4Y^4+16Z^5Y^5+Z^6Y^6}{2^{n-6}Y(3+ZY)(3+6ZY+Z^2Y^2)(7+6ZY+Z^2Y^2)}$

3.1. Analysis of Tree Network Constituted by Different $R_kL_kC_k$-cells

In this case, the SISO-network exposed in Figure 3(b) will become the lumped $R_kL_kC_k$-networks in cascade presented in Figure 5. Acting as a linear circuit, the transfer matrix of this network should be typically governed also by linear differential equations.

This finding leads us to suppose that the elements of the transfer matrix, $[T_{1,k-1}]$ as polynomial expressions defined by the real coefficients denoted $\lambda_{11,k}$ and $\lambda_{21,k}$ for k varying from 1 to $(n-1)$:

$$T_{11}(k) = \begin{cases} 1 + \sum_{l=1}^{k} \lambda_{11,k}(l)s^l & \text{for } 1 \le k \le n-1 \\ 1 + R_n \cdot C_n \cdot s + L_n \cdot C_n \cdot s^2 & \text{for } k = n \end{cases}, \quad (22)$$

$$T_{21}(k) = \begin{cases} \sum_{l=1}^{k} \lambda_{21,k}(l)s^l & \text{for } 1 \le k \le n-1 \\ 2^{n-1}C_n \cdot s & \text{for } k = n \end{cases}, \quad (23)$$

In this case, the whole transfer function of the circuit described in Figure 5 can be written as follows:

$$H_n(s) = \frac{1}{1 + \sum_{l=1}^{n} \lambda_{11,n}(l)s^l}. \quad (24)$$

The real coefficients $\lambda_{11,n}$ can be calculated easily via substitutions of (22) and (23), respectively, into the iterative relations expressed in (10) and (11) introduced earlier in Subsection 2.2. Hence, this yields the following iterative relations enabling the determination of

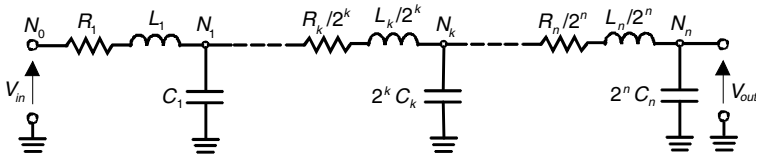

Figure 5. Schematic of the reduced SISO circuit equivalent to n-level RLC-tree network.

the two first coefficients corresponding to $\lambda_{11,n-k}(l)$ and $\lambda_{21,n-k}(l)$ for $l = \{1, 2\}$:

$$\lambda_{11,n-k}(1) = \begin{cases} R_n \cdot C_n & \text{if} \quad k = 0 \\ \lambda_{11,n-k+1}(1) + R_{n-k}\left[2^{1-n+k}\lambda_{21,n-k+1}(1) + C_{n-k}\right], & \text{if} \quad k \geq 1 \end{cases}, \tag{25}$$

$$\lambda_{11,n-k}(2) = \begin{cases} L_n C_n & \text{if} \quad k = 0 \\ \lambda_{11,n-k+1}(2) + R_{n-k}\left[C_{n-k}\lambda_{11,n-k+1}(1) + 2^{1-n+k}\lambda_{21,n-k+1}(2)\right] + L_{n-k} \\ \left[2^{1-n+k}\lambda_{21,n-k+1}(1) + C_{n-k}\right] \quad \text{if} \quad k \geq 1 \end{cases}. \tag{26}$$

The combination of polynomial expressions (22) and (23) with iterative expression (11) implies the hereafter two coefficients of the element T_{21}:

$$\lambda_{21,n-k}(1) = \begin{cases} 0 & \text{if} \quad k = 0 \\ 2^{n-k-1}C_{n-k} + \lambda_{21,n-k+1}(1) & \text{if} \quad k \geq 1 \end{cases}, \tag{27}$$

$$\lambda_{21,n-k}(2) = \begin{cases} 0 & \text{if } k = 0 \\ 2^{n-k-1}C_{n-k}\lambda_{11,n-k+1}(1) + \lambda_{21,n-k+1}(2) & \text{if } k \geq 1 \end{cases}. \tag{28}$$

3.2. Behavioral Model of Identical RLC T-tree Network

The modeling method of the identical RLC T-tree network can be realized from the former subsection analysis by taking $R_k = R$ and $C_k = C$. So that, the two elements of transfer matrix $[T_{1,n-k}]$, T_{11} and T_{21} are supposed written as follows:

$$T_{11}(n-k) = 1 + \sum_{l=1}^{n-k} \lambda_{11,n-k}(l) \cdot s^l, \tag{29}$$

$$T_{21}(n-k) = \sum_{l=1}^{n-k} \lambda_{21,n-k}(l) s^l, \tag{30}$$

and

$$T_{11}(n) = 1 + R \cdot C \cdot s + L \cdot C \cdot s^2, \tag{31}$$

$$T_{21}(n) = 2^{n-1} C \cdot s. \tag{32}$$

By identification and turning over the k-integer values, the two first real coefficients $\lambda_{11,n-k}$ and $\lambda_{21,n-k}$ are respectively, expressed as:

$$\lambda_{11,n-k}(1)=\begin{cases} R\cdot C & \text{if} \quad k=0 \\ R\cdot C+\lambda_{11,n-k+1}(1)+2^{1-n+k}R\cdot\lambda_{21,n-k+1}(1) & \text{if} \quad k\geq 1 \end{cases}, \quad (33)$$

$$\lambda_{11,n-k}(2)=\begin{cases} L\cdot C & \text{if} \quad k=0 \\ R\cdot C\cdot\lambda_{11,n-k+1}(1)+\lambda_{11,n-k+1}(2) & \\ +2^{1-n+k}\left[R\cdot\lambda_{21,n-k+1}(2)+L\cdot\lambda_{21,n-k+1}(1)\right] & \\ +L\cdot C & \text{if} \quad k\geq 1 \end{cases}, \quad (34)$$

and

$$\lambda_{21,n-k}(1)=\begin{cases} 2^{n-1}C & \text{if} \quad k=0 \\ 2^{n-k-1}C+\lambda_{21,n-k+1}(1) & \text{if} \quad k\geq 1 \end{cases}, \quad (35)$$

$$\lambda_{21,n-k}(2)=\begin{cases} 0 & \text{if} \quad k=0 \\ 2^{n-k-1}C\lambda_{11,n-k+1}(1)+\lambda_{21,n-k+1}(2) & \text{if} \quad k\geq 1 \end{cases}. \quad (36)$$

To illustrate the relevance of the literal model developed in more natural point of view, further analysis on the RLC T-tree network time-domain responses will be made in the next subsection.

3.3. Time Domain Analysis of the RLC T-tree Interconnect Proposed

During the analysis of analogue-digital or mixed SI propagating through the electronic interconnects as the T-tree networks; similar to most of mixed systems investigation, time-domain analyses constitute the fundamental way. It enables for example, to determine the relevant expressions of the output voltage attenuation prior to transient square wave input voltage. In this case, it is important to note that as reported in [39, 48, 49], the base bandwidth of the considered digital signal is usually linked to its rise time t_r by the following relation:

$$f_{\max}=\frac{0.35}{t_r}. \quad (37)$$

This frequency band limitation allows the reduction or simplification of the transfer function $H_n(s)$ denominator by proceeding with the polynomial limited expansion. For the case of n-level RLC-tree network, the second order approximated transfer function associated to the whole circuit represented in Figure 3(a) of Section 2 (by taking $Z=R+Ls$ and $Y=Cs$) can be formulated as follows:

$$H_n(s)=\frac{1}{1+\sum\limits_{l=1}^{n}\lambda_{11,n}(l)s^l}\approx\frac{1}{1+\lambda_{11,n}(1)s+\lambda_{11,n}(2)s^2+\ldots}, \quad (38)$$

This expression represents the under study symmetrical RLC-tree network transfer function in function of the level number n. So, one can determine easily the tree network SI parameters as the signal attenuation. By considering the unit step response of the transfer function first-order-model, the temporal signal attenuation at the time $t = T$ can be written as follow:

$$\alpha_n = \frac{v_n(T)}{v_0(T)} = 1 - \exp\left[-\frac{T}{\lambda_{11,n}(1)}\right]. \tag{39}$$

For the validation of all above theoretic concept, concrete examples of application based on the RLC-interconnect T-tree network modeling are proposed in the next section.

3.4. Routine Algorithm of the Modeling Method Proposed

As aforementioned, the modeling method of the transfer functions (summarized in Tables 1 and 2) and the SIMO T-tree transfer impedances (see Table 3) versus the tree level n is illustrated by Figure 6.

In the first step, we need to determine the RLC-parameters of each piece of lines by using the methods reported in [49]. Then, we can establish the transfer matrix $[T_{1,n}]$ of the n-level T-tree network after the design of the SISO network equivalent to the tree understudy. At the calculation of the tree-network transfer function, one can determine the frequency- and/or time-domain responses. In the last step, it is possible to calculate the SI-parameters according to the targeted applications of the T-tree network.

4. APPLICATIONS WITH LUMPED RLC AND MICROSTRIP T-TREE INTERCONNECTS

For the verification of the developed modeling method, the routine algorithm was implemented into Matlab program and the results were compared with realistic EM and circuit co-simulations with one of the standard commercial tools. Examples of high-speed interconnect RLC T-tree networks with different levels were analyzed in this section. The application results proposed were designed and simulated in the SPICE and 3D EDMS environments run with electronic microwave simulators ADS-software from Agilent^{TM}.

4.1. Validation with Lumped RLC-tree

In this subsection, validation both in frequency- and in time-domains with T-tree circuits based on the lumped RLC-networks is presented.

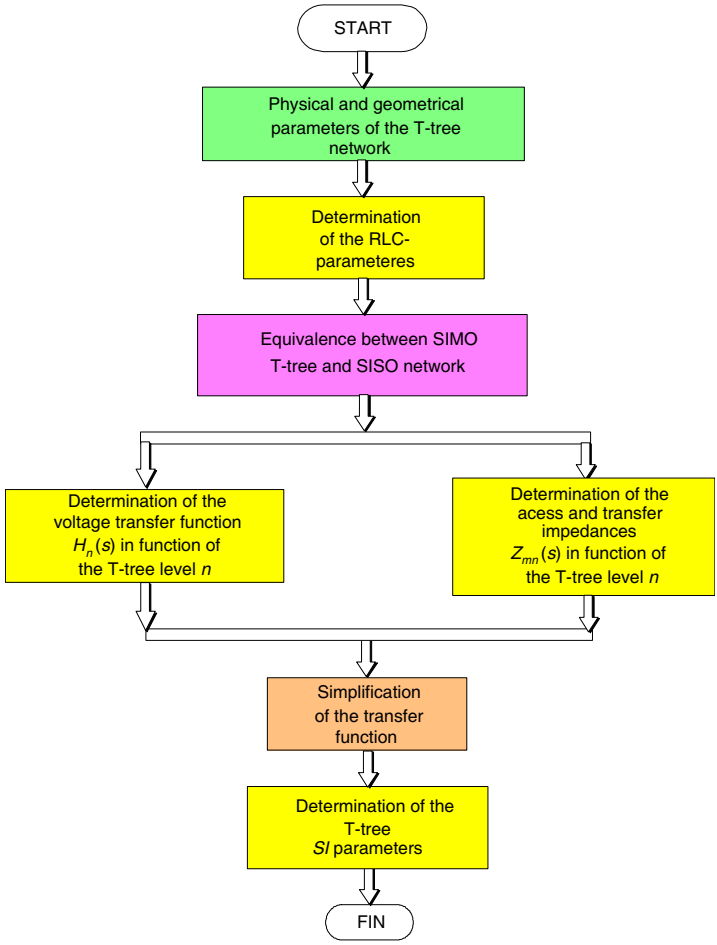

Figure 6. Work flow summarizing the application guideline of the modeling method proposed.

Then, predictions of the T-tree interconnects with levels more than tens will be made also in order to demonstrate the relevance of the expressions developed in previous section.

4.1.1. Description of the Structure Understudy

As depicted in Figure 7, a four-level RLC T-tree distribution network was considered. To demonstrate the feasibility of the modeling method vis-à-vis the tree network level number, $n = \{3, 4, 5\}$-level circuits are considered. Each branch of this RLC-tree network is consisted

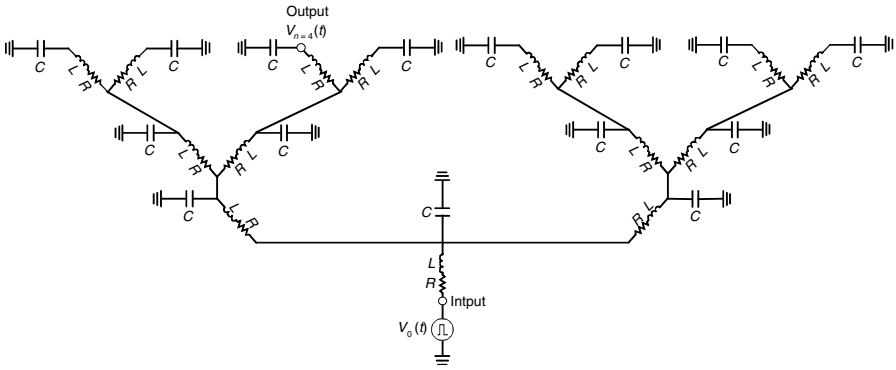

Figure 7. Schematic of the simulated RLC-tree circuit ($R = 38\,\Omega$, $L = 2.65\,\text{nH}$, $C = 1.3\,\text{pF}$ and $n = 4$).

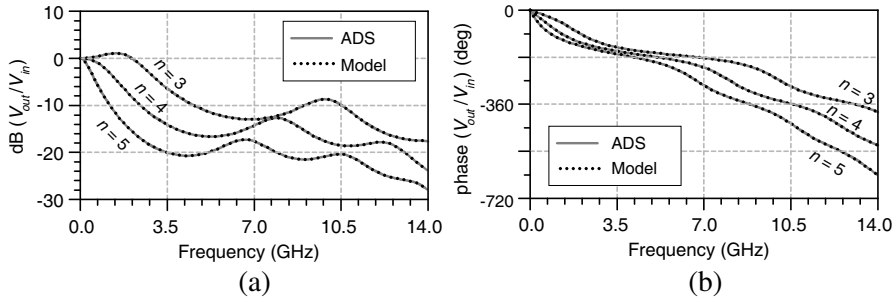

Figure 8. Comparisons of ADS and the proposed model frequency results of identical lumped RC-tree network for $n = \{3, 4, 5\}$. (a) Magnitude- and (b) phase-responses.

of global interconnect comprised of long wires for deep submicron technologies proposed in [15]. As a use case example, the RLC long inter-chip interconnect with per unit length parameters $R_u = 76\,\Omega/\text{cm}$, $L_u = 5.3\,\text{nH/cm}$ and $C_u = 2.6\,\text{pF/cm}$ for a physical length $d = 2\,\text{mm}$ are taken in this section.

For 0.25-μm CMOS technology, these interconnect parameters were established from conductor line with 2.4 μm width [15]. Meanwhile, the equivalent lumped parameters are equal to $R = R_u \times d$, $R = R_u \times d$ and $C = C_u \times d$. As aforementioned earlier, by reason of symmetry, the voltages, detected at the output terminals of the considered tree network are the same as the output of the equivalent SISO network ($v_n(t) = v_{out}(t)$) for $n = \{3, 4, 5\}$.

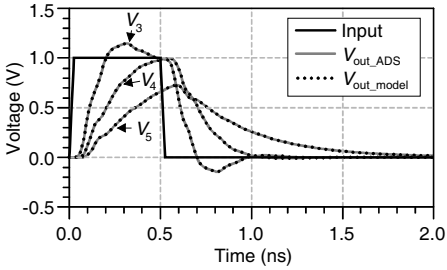

Figure 9. Comparisons of ADS and the proposed model time-domain results of lumped RLC-tree network for 2-Gbits/s rate input trapezoidal voltage excitation for $n = \{3, 4, 5\}$.

4.1.2. Numerical Validation Results in Frequency- and Time-domains in UWB

As depicted in Figures 8 and 9, an excellent agreement between the frequency- and time-domain results was realized between the models proposed from Table 2 computed in Matlab programming environment (plotted in black dashed curve) and SPICE simulations (plotted in full grey curve). Figure 8 views the frequency responses of the RLC-tree networks shown in Figure 7 from DC to 14 GHz. As can be seen here the attenuations and phase values of the isochrone transmittances, $H_n(j\omega) = V_n(j\omega)/V_0(j\omega)$ are obviously; more important when n is greater.

To carry out the time domain analysis, the understudy RLC-tree networks were excited by a periodical trapezoidal transient source with normalized amplitude, $V_{\max} = 1\,\text{V}$, pulse width, $T_w = 0.5\,\text{ns}$, rise-/fall-time $t_r = 25\,\text{ps}$ and having a time duration, $T = 4T_w = 2\,\text{ns}$. As illustrated in Figure 9, the calculated responses with the proposed model plotted in full grey lines coincide very well with SPICE transient-responses plotted in dotted black lines. As predicted intuitively in theory, one observes that the output tree networks, v_n are more and more degraded when n is higher.

These results confirm the exactitude of the established transfer function and the effectiveness of the proposed method for the SI analysis. Compared to the method introduced in [29, 52], the introduced global transfer function presents technical benefits in terms of precision and its flexibility for the high-level tree networks. So, it can be used by the microelectronic circuit designers notably for the fast and accurate estimation of the distortions caused by the tree network whatever its level number.

By using expression (39), the tree network voltage attenuations

$\alpha_n = v_n(T)/v_0$ were evaluated. To check the accuracy of this formula, comparison with SPICE-computation was also made in Table 4. So, the analytical results present relative errors lower than 5-% fit very compared to the SPICE-computation.

4.1.3. Investigation on More than 10 Levels T-tree Structure

In order to evidence the operability of the proposed modeling method for very high values of tree level, n (more than 10), quantitative time-dependent analysis on the variations of the attenuation generated by the tree network was performed. The Matlab implementation of the transfer function coefficients expressed in recursive relations (33)–(39) established earlier in Subsection 3.2, one can evaluate easily the temporal response parameters for very high value of n. The value of attenuation α_n in function of the number of tree level n was calculated. This enables to investigate the influence of n for example, when its value is widely higher than 5. To do so, by using expression (39), the plot of $\alpha_n(T)$ versus n displayed in Figure 10 is realized.

With these examples, it can be pointed out that when the RLC-level number n is higher than 20, the output level is strongly attenuated and less than 1-% of the input amplitude. For $T = 0.5\,\text{ns}$ and n

Table 4. Comparison of multi-level interconnect attenuations from SPICE-computations and the proposed model.

	$\alpha_n = v_n(T)/V_{\max}$	
n	SPICE	Proposed model
3	0.994	0.996
4	0.951	0.903
5	0.660	0.652

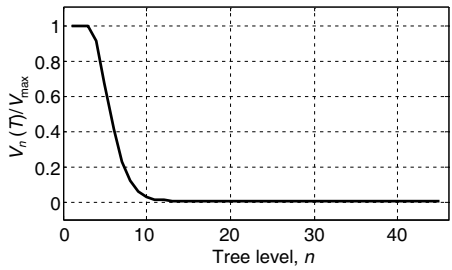

Figure 10. Attenuation $\alpha_n = v_n/V_{\max}$ versus number of RLC-tree level, n for $T = 0.5\,\text{ns}$.

higher than 40, the output voltages are completely negligible compared to the input one. Otherwise, it is noteworthy that this calculation was made over the computation in order of some ms. Compared to previous studies [28, 52], the proposed method enables to estimate the attenuations and delays in function of level numbers which can be in order of hundreds.

4.2. Validation with Distributed Microstrip T-tree Interconnect

More concrete validations of the modeling method proposed were made by considering microstrip T-tree interconnect with two- and three-levels. To do this, frequency- and time-domain responses from the tested structures were computed and generated. The next paragraphs of this section draw the description of the interconnect under test (IUT) and also interpret the comparative results for the validations. It is interesting to note that the frequency- and time-domain simulations carried out in this paper were performed first in the 3D EDMS environment and then associated to the lumped elements co-simulated in the SPICE schematic environment of ADS. In time-domain, the transient source was introduced in the SPICE schematic and then interacting with the S-parameters from the 3D numerical tests.

4.2.1. Description of the Structure under Test

To verify the feasibility of the method developed by considering the models of transfer functions established in Table 2 and the input impedances in Table 3, T-tree IUTs were considered with $n = 2$ and $n = 3$ levels. Figure 11 represents the layout diagram of the IUT understudy, comprised of three levels of microstrip line with geometrical parameters width $w = 0.1\,\mu\text{m}$ and length $d = 3\,\text{mm}$.

The IUTs considered in this section are printed on the dielectric substrate having permittivity $\varepsilon_r = 4.4$ and thickness $y = 1.6\,\text{mm}$. The metallization are in Cu with thickness $t = 35\,\mu\text{m}$. I point out that design and simulations of structures presented in this section were made in Schematic and Momentum environments of ADS software. By applying the RLCG modeling technique developed in [49–51], the per unit length parameters of each interconnect single line constituting the interconnect under test are $R_u = 74.6\,\Omega$, $L_u = 9\,\text{nH}$ and $C_u = 35\,\text{pF}$. By using these parameters, the formulation of the global reduced model established considered in Section 3 was applied by supposing that the IUT is loaded by parallel RC-network $Z_L = R_L/C_L$. During the simulations, the capacitance C_L was fixed to $2\,\text{pF}$ and the resistance R_L was varied from $100\,\Omega$ to $300\,\Omega$.

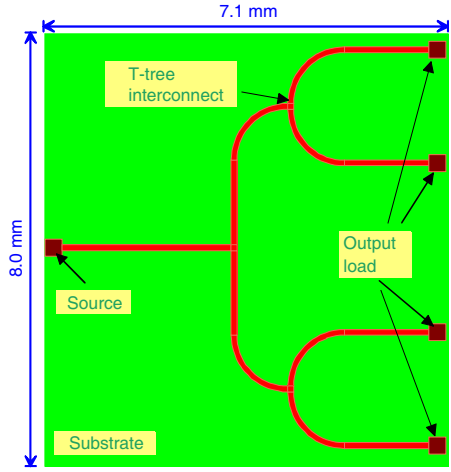

Figure 11. Layout of the three level T-tree interconnect under test.

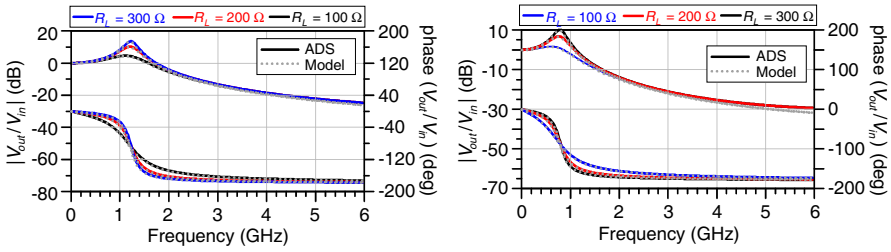

Figure 12. Comparisons of the voltage transfer function frequency responses of interconnect T-tree simulated with ADS and from the model proposed. (a) Two levels. (b) Three levels.

4.2.2. Frequency Analysis Results

Figure 12 displays the voltage transfer function frequency responses generated from the 3D environment of ADS and the transfer functions addressed in Table 2 from DC to 6 GHz. We can see that good correlations were realized both for $n = 2$ and $n = 3$ levels for different values of the resistance load. Resonances can be forecasted at about 1.35 GHz and 0.78 GHz respectively for $n = 2$ and $n = 3$. Furthermore, this resonance effect is more and more accentuated when R_L is increased.

Despite this aspect, due to the dispersive effects on the RLCG model as the skin depth effects, an absolute difference of about 4 dB is found for the frequencies higher than 4 GHz.

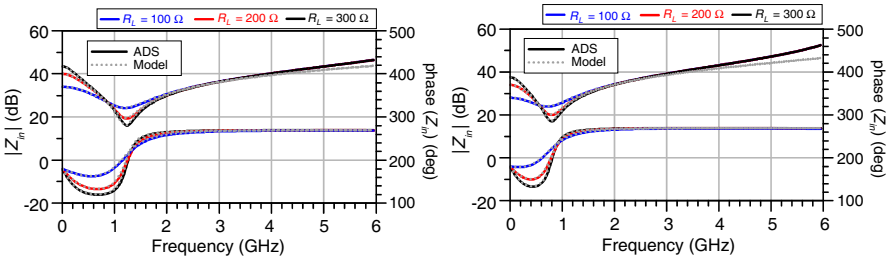

Figure 13. Comparisons of the input impedances of interconnect T-tree simulated with ADS and from the model proposed. (a) Two levels. (b) Three levels.

The same comparisons were made by considering the behavioral models of the T-tree IUT input impedances $Z_{in} = V_{in}/I_{in}$ offered in Table 3. Figure 13 displays the plots of the magnitudes and the phases of $Z_{in}(f)$ from DC to 6 GHz. Once again, very good agreements between the behavioral models (plotted in dotted lines) and the reference results (plotted in full lines) from ADS-EMDS were achieved both for $n = 2$ and $n = 3$. We can found that the same resonance effects are forecasted. This SI prediction is particularly interesting during the design stage for the matching between the T-tree IUTs and the signal source.

An absolute difference of about 0.1 dB is realized in base band frequencies lower than 3 GHz between the behavioral input impedances and ADS results. However, for $n = 2$ and $n = 3$, we can find that this difference is respectively of about 4 dB and 9 dB for the frequency higher than 5.5 GHz. According to the frequency limitations of the operating data as defined in (37), it is possible to predict the SI for the case of signals presenting bandwidth lower than some GHz. The improvement of the models can be performed by considering the non-polynomial mathematical models as introduced in [49].

4.2.3. Time-domain Analysis Results

More illustrating representation of the validity of the behavioral analytical model developed was also carried out by using high rate numerical data. To do this, the time domain responses of the T-tree IUTs were generated by considering an arbitrary binary 8 bits sequence "01001100" with rate 2 Gsym/s presenting a rise time of about 50 ps. The amplitude of the operating data was normalized ($V_m = 1$ V).

Figure 14 displays the comparative results from 3D EMDS and SPICE-schematic co-simulations and the behavioral models established

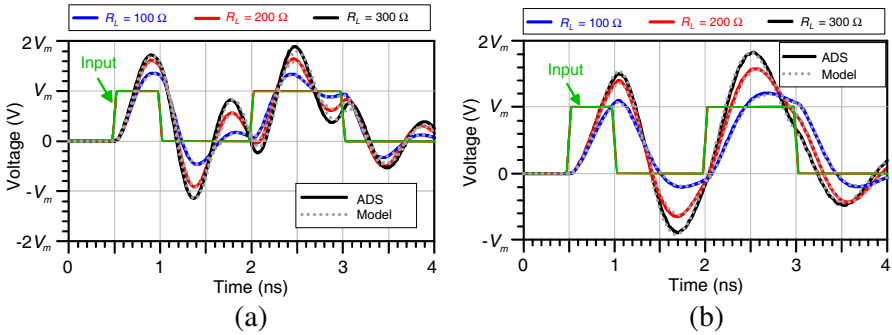

Figure 14. Comparisons of the time-domain responses of interconnect T-tree simulated with ADS and from the model proposed. (a) Two levels. (b) Three levels.

for the both cases $n = 2$ and $n = 3$. Once again, very good correlations were found. We can point out that a significant degradation of the operating data is found due to the T-trees. Moreover, the distortion increases with the value of the load resistance R_L. An overshoot voltage more than 70% of the operating signal amplitude is generated by the IUTs.

It is worth noting that the PC used during the simulations of the structure presented in Figure 11 is equipped a single-core processor XEON 3.4 GHz and 4 GB physical memory with 32-bits Windows XP. The computation time with the co-simulation with EDMS and SPICE schematic environments was more than five of minute against tens seconds by using the routine algorithm introduced in Figure 6 implemented in Matlab.

Compared to the commercial 3D EM standard software (EDMS, HFSS, CST, Inca3D) [54–57], the behavioral models of T-tree networks developed in this paper presents a very less computation time hundreds times lower.

To sum up all above theoretical and application analysis concluding remarks are provided in the following section.

5. CONCLUSION

An innovative methodology of global behavioral modeling of the symmetrical T-tree distribution networks constituted by lumped element L-cell four terminal circuits is successfully presented. The mathematical ways enabling the simplifications of the typical SIMO T-tree circuit into its equivalent SISO circuit is investigated. The here described modeling method is purely based on the direct analytical

calculation based on the mathematical operations of L-cell transfer matrices in cascade. Formulations of the voltage transfer functions and the input impedances of multi-level the T-tree networks in function of the tree level are established and simplified for the case of linear circuits. These exact expressions representing the behavioral voltage transfer functions and input impedances are implemented into Matlab.

More importantly, regarding the typical RLC T-tree networks, the mathematical recursive expressions for the determination of the considered tree characteristic equation coefficients are also established. From where, the possibility to evaluate the SI parameters of the T-tree network as attenuation, under-/over-shoots and propagation delays according to existing well-known models was evidenced. Compared to the modeling methods published in [29, 53] which are based on the moment calculation of linear transfer function, the proposed method is more efficient in terms of precision and computation time consuming, in particular, if the tree level is higher (more than tree). Moreover, by using 3D EM and SPICE-schematic co-simulations run with the commercial ADS software, a very good agreement between the simulations and the proposed behavioral models is observed. The obtained results reveal the effectiveness of the developed circuit theoretic analysis which is aimed to the global n-level symmetrical RLC-tree network transfer function. Thus, it was demonstrated also that the established model permits an easy and more accurately estimation of signal distortions and losses caused by the clock tree distribution network.

Further investigation for more concrete application environment is in progress owing to the clock tree networks comprised of distributed elements. In the future, I envisage to use the tree network model introduced for the improvement of the clock tree distribution network performance regarding the influence in on chip-to-chip integrated system interconnects like SiP, PiP/PoP, MCM and SoC. Finally, I plan also to correct the signal degradation through the high speed tree network by using the negative group delay circuit.

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