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LOW-INSERTION LOSS PIN DIODE SWITCHES USING IMPEDANCE-TRANSFORMATION NETWORKS

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Abstract—Two SPDT switches that have low insertion loss with impedance-transformation networks are presented. The proposed SPDT switches are comprised of two shunt *PIN*s and two quarter-wavelength microstrip lines together with impedance transformation networks, which canceled the capacitance effect at off-state and the inductance effect at on-state simultaneously. The simulated insertion loss performance is less than 0.3 dB and the fabricated ones exhibit on-state low insertion loss of 0.5 dB within the range of 4.6–4.8 GHz.

1. INTRODUCTION

The switch is one of the key components for many applications, such as radars, phased array antennas and direction modulators. In TDD system, a low insertion loss SPDT switch is needed in the transmit model in order to transmit power at a minimum loss from the PA (power amplifier) to the antenna and protect the sensitive receiver circuits from high power reflected signal from antenna. At the same time the low-insertion switch is critical because it causes direct reduction of noise figure of the receiver. *PIN* diode type is preferred due to high powering handling abilities and fast switching speed [1]. The p-i-n junction effect of the diode, however, leads to bad performance such as more insertion loss and low isolation compared with MEMS switch [2].

Resonant method is demonstrated in [3] by tuning with a parallel inductance to compensate the elements capacitive effects. They achieve as high isolation as 40 dB at the cost of worse insertion loss which is more than 1 dB. Another technique mentioned in [4, 5] is to insert a filter to absorb the switch elements parasitic parameters. Good

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insertion loss and isolation performances have been obtained in both of them but the topologies are complicated and large circuit size is unavoidable. Multi-stage type in [6] is demonstrated to achieve a high isolation. However, the use of many switch elements leads to deterioration of insertion loss and puts limit on enhancing of the switching speed. Impedance-transformation technique is used in [7] but inductor effect was not taken considered which is not suitable for the circuits where the inductive effects can not be neglected.

In this paper, two novel parallel matching methods are proposed with which the capacitive and inductive effect can be canceled simultaneously so that the low insertion loss and relatively high isolation performance can be expected. Switches with this principle also have high-speed switching potential because fewer *PIN*s are used. Two shunt *PIN* SPDT switches were fabricated and both of them achieved low insertion loss of 0.5 dB and maximum isolation of 30 dB at 4.7 GHz.

2. DESIGN PRINCIPLE

Two schematic circuit diagrams of the switches are shown in Fig. 1. Both of the switches consist of two output arms symmetrically, each comprised of only one diode embedded in the transformation network which is marked by the red dash line. Signal-line segments in the input-to-out1 path, as well as in the input-to-out2 path, have a characteristics impedance of 50 Ω.

Switch operation is performed by changing control voltages VC and $\overline{\text{VC}}$, which causes an *PIN* to be in either on-state or off-state. The on-state *PIN* together with the transformation network provides a transmission arm and the RF signal pass through the input-to-out1 port. The quarter-wavelength transmission line Q_2 incorporated the off-state *PIN* with the transformation networks provides a high input-to-out2 isolation. The capacitors are used to block DC current.

Simple diodes models are used to explain the operation principles. A simplified model consisting of a series combination of a resistance R_{on} and an inductance L_{on} is represented the on-state diode. Similarly, in the off-state diode the junction capacitance dominates, and a capacitance C_{off} can model this impedance.

Two kinds of impedance transformation networks are proposed as shown in Fig. 1 in the dash-line blocks. In Fig. 1(a) the *PIN* is series to the transformation network while the diode is shunt to ground in Fig. 1(b). The electrical length of L_1 and L_2 in Fig. 1 are θ_1, θ_2 respectively and the characteristics impedances are 50 Ω. The bias circuits designs shown in the solid-line blocks are made of single radial

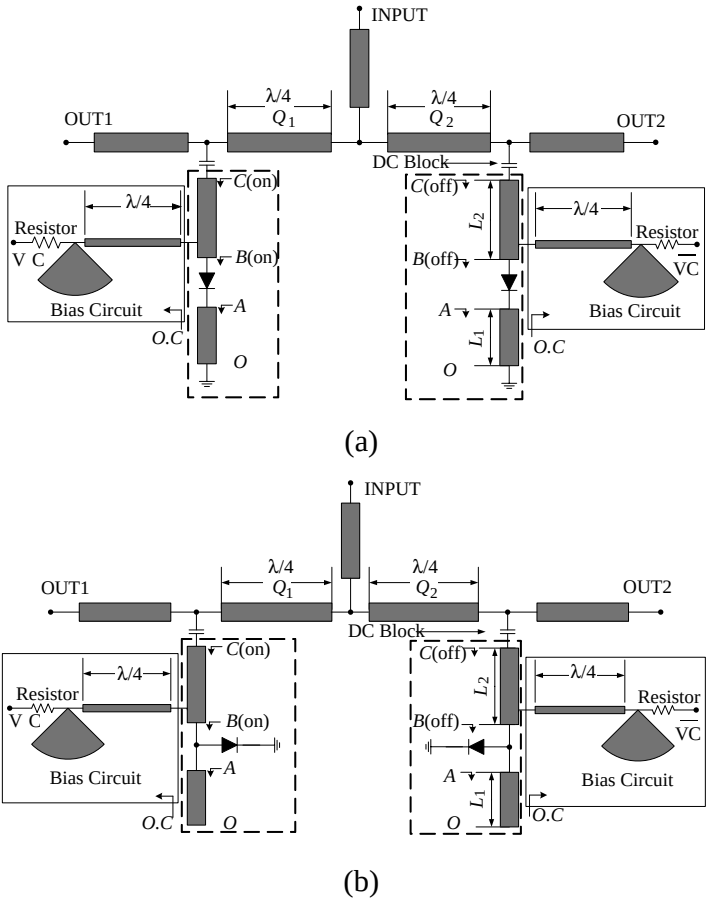


Figure 1. Impedance-transformation networks and topologies. (a) Series-type. (b) Shunt-type.

stubs, followed by high-characteristic-impedance quarter-wavelength transmission lines. Each bias circuit connected to L_2 is regarded as open circuit point in order to prevent RF leakage.

In Fig. 1(a), named series-type switch, we insert transmission L_1 with a short end and L_2 on both sides of *PIN*. The input impedance values looking into points (A–C) for both on and off states are indicated on the Smith chart, as shown in Fig. 2(a). Beginning with a short point O, segment L_1 leads the impedance to point A. This point physically corresponds to the cathode contact. Then, depending on the on/off state of the diode, the corresponding impedances get to the points

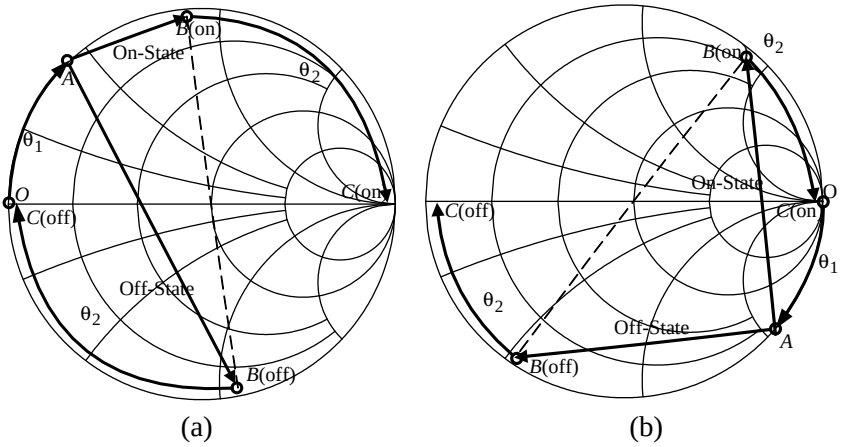


Figure 2. Matching methods shown in smith chart. (a) Series-type. (b) Shunt-type.

B(on) and B(off). Finally, line L_2 possessing an electrical length of θ_2 is added leading the impedance to C(on) and C(off) respectively. By selecting the length of transmission line L_1 and L_2 making B(on) and B(off) in a straight line passing through the center of the Smith chart, the effects of both C_{off} and L_{on} of the *PIN* can be reduced. Certainly, the use of electrical length of the lines L_1 and L_2 is an approximation, and accurate calculation is needed as the frequency increases to account for the losses and dispersion.

The principle of the shunt-type switch shown in Fig. 1(b) is similar. Starting from an open circuit point O, the input impedance looking into points (A–C) are illustrated in Fig. 2(b). The input impedance values of both the on and off states can be successfully transferred to a near open circuit and a near short circuit (point C's), respectively.

Consequently, transmission line L_1 and L_2 compensate the parasitic elements of *PIN* by resultant parallel resonance at on-state and series resonance at off-state in both of the structure. Thus, the signal will be transmitted by causing the *PIN* to be at on-state. On the other hand, by causing the *PIN* to be at off-state, the signal path becomes "short" and the signal is blocked by the quarter-wavelength transmission. The input impedance of both on and off states circuits resonates at the same transformation network, so a minimum insertion loss and a maximum isolation can be expected. Theory analysis can help to decide the electrical length of L_1 and L_2.

In series-type analysis, the on- and off-state input impedances of

the *PIN* are:

$$Z_{PIN(\text{on})} = R_{\text{on}} + j\omega L_{\text{on}} \tag{1}$$

$$Z_{PIN(\text{off})} = \frac{1}{j\omega C_{\text{off}}} \tag{2}$$

The input on- and off-state impedances looking into point C are: $(Z_0 = 50\,\Omega)$

$$Z_{C(\text{on})} = Z_0 \frac{R_{\text{on}} + j\omega L_{\text{on}} + jZ_0 \tan\theta_1 + jZ_0 \tan\theta_2}{Z_0 + j\tan\theta_2 \left(R_{\text{on}} + j\omega L_{\text{on}} + jZ_0 \tan\theta_1\right)} \tag{3}$$

$$Z_{C(\text{off})} = Z_0 \frac{\frac{1}{j\omega C_{\text{off}}} + jZ_0 \tan\theta_1 + jZ_0 \tan\theta_2}{Z_0 + j\tan\theta_2 \left(\frac{1}{j\omega C_{\text{off}}} + jZ_0 \tan\theta_1\right)} \tag{4}$$

The position of $C(\text{off})$ locates near the short circuit point, the numerator in $Z_{C(\text{off})}$ fraction on must be zero. Then we get:

$$Z_0\omega C_{\text{off}} \tan\theta_1 + Z_0\omega C_{\text{off}} \tan\theta_2 = 1 \tag{5}$$

Under the condition of (5), we noticed the numerator in $Z_{C(\text{on})}$ a constant. So we only let the denominator be minimized.

$$\min \left\| Z_0 - Z_0 \left(\tan\theta_1 \tan\theta_2\right) - \omega L_{\text{on}} \tan\theta_2 + jR_{\text{on}} \tan\theta_2 \right\| \tag{6}$$

The approximate solution is that the real part of (6) is zero, because R_{on} is small and can be neglected, thus we have:

$$Z_0 - Z_0 \left(\tan\theta_1 \tan\theta_2\right) - \omega L_{\text{on}} \tan\theta_2 = 0 \tag{7}$$

For the given frequency ω the electrical length of θ_1 and θ_2 can be resolved through (5) and (7) when (8) is fulfilled.

$$\omega L_{\text{on}} + \frac{1}{\omega C_{\text{off}}} > 2Z_0. \tag{8}$$

Similar analysis method in a parallel type one may get: $(Y_0 = \frac{1}{Z_0})$

$$\omega L_{\text{on}} Y_0 \tan\theta_1 + \omega L_{\text{on}} Y_0 \tan\theta_2 = 1 \tag{9}$$

$$Y_0 - Y_0 \tan\theta_1 \tan\theta_2 - \omega C_{\text{off}} \tan\theta_2 = 0 \tag{10}$$

$$\omega C_{\text{off}} + \frac{1}{\omega L_{\text{on}}} > 2Y_0 \tag{11}$$

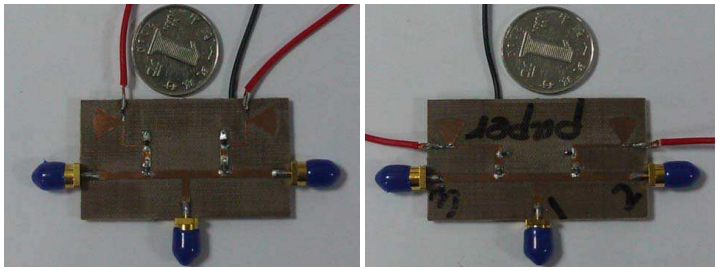
For the given frequency, the electrical length of θ_1 and θ_2 can be resolved through (9) and (10) when the condition of (11) is fulfilled The above resonances can be realized to compensate the *PIN*'s small inductance and large capacitance effect under the condition of inequality (8) or (11).

3. RESULTS AND DISCUSSION

The switches are designed at 4.7 GHz and implemented on the 0.762 mm-thick substrate with dielectric constant of 2.55. We use Skyworks surface mount *PIN* diode SMP1321-079. We choose a large DC capacitor to avoid the DC block capacitive effect influencing the impedance transformation network. The optimized parameters are listed in Table 1. The two proposed SPDT switches with a size of 34 mm × 59 mm are fabricated as illustrated in Fig. 3.

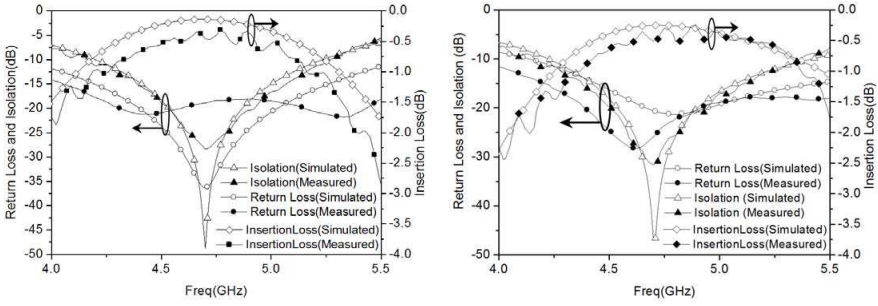
Table 1. Optimized design parameters of the prototype.

Design	Resistor (Ω)	L_1/L_2 (mm)	DC Block (μF)
Series-type	100	2.9/5.9	1
Shunt-type	100	2.3/4.5	1



(a) (b)

Figure 3. Photographs for proposed switches. (a) Series-type. (b) Shunt-type.



(a) (b)

Figure 4. Measured results for proposed types. (a) Series-type. (b) Shunt-type.

Simulated and measured results are shown in Fig. 4. Both of the simulated insertion loss is less than 0.3 dB through 4.6 GHz to 4.8 GHz and the isolation is more than 20 dB. Considering the insertion loss of the *SMA*, insertion loss is a bit larger in measurement which is around 0.5 dB. Due to the low quality factor of the *DC* block capacitor and the off-state *PIN*, the measured isolation performance is inferior to the simulation results. The maximum isolation is about 30 dB at 4.7 GHz. The agreements between simulated results and measured results indicate the feasibility of the design principle.

4. CONCLUSION

Two SPDT switches that have low insertion loss with impedance-transformation networks are presented. The proposed switches exhibit a low insertion loss of 0.5 dB, a maximum isolation of around 30 dB. The measured results indicate the validity of this design concept which will become important in high-frequency hybrid circuits where the diode package inductance is no longer negligible. Also the simple topology and small size make a cascading switching network easier.

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