FPGA IMPLEMENTATION OF SPACE-TIME ADAPTIVE PROCESSING (STAP) ALGORITHM FOR TARGET DETECTION IN PASSIVE RADARS

Zia Ul Mahmood[1, *], Mubashir Alam[1], Khalid Jamil[2], and Zeyad O. Al-Hekail[1, 2]

[1]Department of Electrical Engineering, King Saud University, Riyadh, Saudi Arabia

[2]Prince Sultan Advanced Technologies Research Institute, King Saud University, Riyadh, Saudi Arabia

Abstract—Space-Time Adaptive Processing (STAP) algorithm has recently been used in Passive Bi-static Radars (PBR) because it removes the clutter and non-cooperative transmitter effectively making the target detection easy in harsh environments like air-ground. Real-time implementation of STAP is a very challenging task as it is computationally-intensive, time-critical and resource-hungry process. This paper focuses on the Field-Programmable Gate Array (FPGA) implementation of STAP algorithm for passive radar using FM radio as transmitter of opportunity. The signals of interest were collected using an eight-channel software-defined radar with a uniform circular array (UCA). The STAP processing was simulated using MATLAB and hardware implementation was carried out on a Xilinx Virtex-6 FPGA. The system is tested using experimental radar data. Timing and Power analysis of hardware implementation justifies that FPGA provides a fast and reliable platform for STAP real-time radar processing.

1. INTRODUCTION

Passive bi-static radars (PBR) has received significant interest during the past few years among various defense entities for surveillance and defense applications. These radars exploit signals of opportunity from a wide variety of communication or broadcast emissions like FM, TV, GSM, DAB, DVB-T, WiMax, WLAN/WiFi, satellite, etc. [12–18, 24]. They offer a number of advantages over conventional active

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radar system: reduced operational cost, lower power requirements, covertness and anti-stealth.

A typical passive radar system consist of two channels connected with two antennas. One antenna, labeled as reference antenna, captures the direct (reference) signal from the transmitter. A second antenna captures the reflected signal from target. These two signals are processed together for target detection using match-filtering like cross-ambiguity processing [8, 9, 16, 23].

A more sophisticated multi-channel multi-frequency digital receiver system is developed using an array of antennas [19]. This type of advance system gives additional capabilities like digital beamforming and advance adaptive filtering for target detection and clutter rejection [9, 19, 20]. One of the candidate adaptive algorithm for this kind of radar processing is joint space-time adaptive processing (STAP). It is particularly useful in detecting weak and slow moving ground targets in airborne clutter environments.

Much of the research has been done on STAP with active radars using uniform linear array (ULA) [3, 10, 11] and circular array [4, 5, 7]. Some of the research exists on the clutter suppression of airborne radar [25–27]. Similarly, some adaptive filter algorithms were used for clutter cancellation in PBR [22]. A code was designed to maximize the detection performance of radar STAP [21]. A limited research exists on using STAP for a passive radar system. One such system and algorithm is presented in [8, 9], which uses a receiver setup of two antenna system to capture the signal of interests. Further research was conducted in an attempt to develop a more advanced receiver setup like ULA [1, 2] and UCA [6, 19, 20]. There is no notable research available on the FPGA implementation of STAP algorithm for PBR case while using UCA for effective target detection and tracking.

This paper presents modeling and implementation of STAP algorithm for target detection in passive bistatic radar case using a uniform circular array to capture the signals of interest. The antenna array consists of eight elements with uniform radial spacing. The UCA geometry is deployed due to its ability to steer the beam in azimuth digitally through 360° without any mechanical movement [6]. Also, a cooperative FM transmitter was used as an illuminator of opportunity. The actual experiment was performed with moving vehicle as a target.

This paper emphasizes the hardware implementation aspect of STAP algorithm in PBR. System model containing the data reception scenario and the pre-processing steps are explained in Section 2. The processing results are described in Section 3. Section 4 explains the FPGA implementation of the STAP processor. Concluding remarks are given in Section 5.
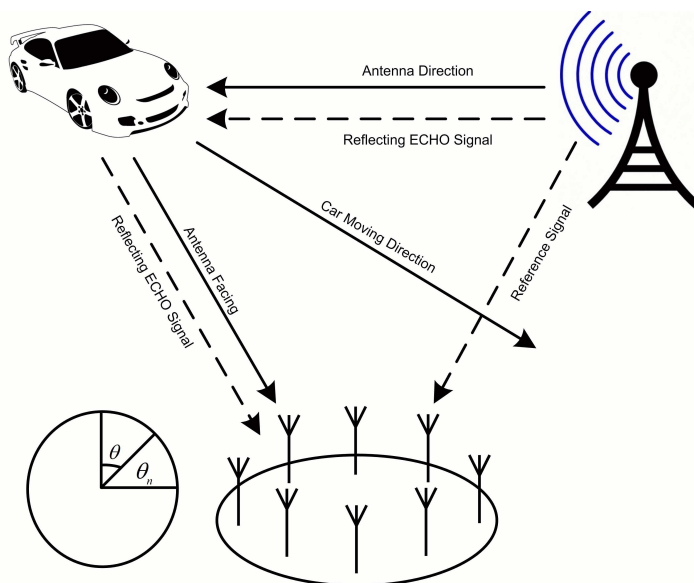
2. DATA RECEPTION SCENARIO

The experimental setup consists of an FM transmitter, a moving vehicle as a target and a circular eight-element antenna array as shown in Fig. 1. This is used to record the eight real time signals separately impinging on each antenna element of the uniform circular array.
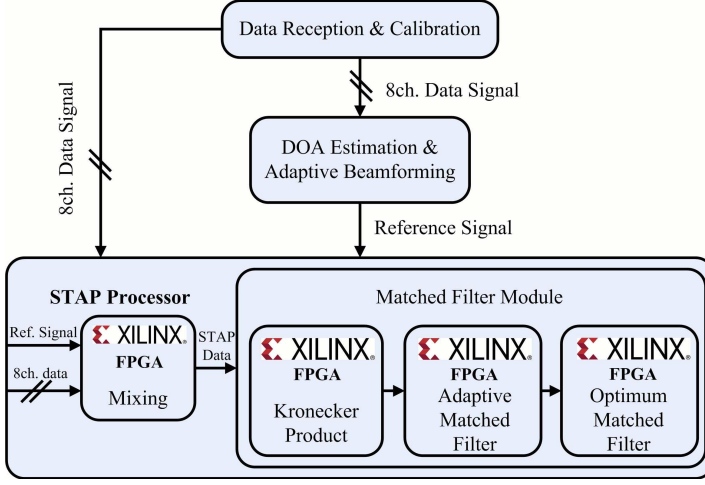
The signal processing block diagram is shown in Fig. 2 to elaborate the system setup. Pre-processing includes the calibration of phase and amplitude errors of the eight-channel real-time FM data. The calibrated array data are then subjected to Direction-of-Arrival (DOA) estimation and adaptive digital beam-forming in order to obtain pure reference signal from the transmitter without any echo return from targets. The pure reference and the eight-channel data containing the echoes from the targets is then used for STAP processing.

2.1. STAP Processing

The STAP processing needs a pure reference signal and eight channel data signal as its inputs. The algorithm used was the one presented in [8], with one major improvement in the term of multi-element circular array geometry, to achieve more flexibility and coverage. The mixing module as shown in Fig. 2 is used to combine the eight channel

Figure 1. Data reception scenario.

Figure 2. Signal processing block diagram of an array based passive radar.

data signal with time delayed version of the pure reference signal, $\mathbf{x_{ref}}(k-n)$. For the specific case of UCA, the spatial steering vector and temporal steering vector are given by (1) and (2) respectively.

$$\mathbf{a}(v_s) = \left[e^{(j\beta R \cos(\theta_1 - \theta))}, \ldots, e^{(j\beta R \cos(\theta_N - \theta))} \right]^T \tag{1}$$

$$\mathbf{b}(v_d) = \left[1, e^{j2\pi v_d}, \ldots, e^{j2\pi v_d(M-1)} \right]^T \tag{2}$$

where $\beta = \frac{2\pi}{\lambda}$ and λ is the wave-length, R the radius of the array. The angular position of each element in the array is given by $\theta_n = \frac{2\pi n}{N}$, where N is the number of antenna elements, and θ the incidence angle or the scanning angle. The spatial frequency is given by $v_s = \beta R \cos(\theta_n - \theta)$ and $v_d = \frac{f_d S}{f_s}$ is the reduced Doppler frequency, where f_d the Doppler frequency of the target, S and f_s denote the sub-sampling factor and sampling frequency respectively [8]. The combined spatio-temporal steering vector is given by:

$$\mathbf{v}(v_s, v_d) = \mathbf{a}(v_s) \otimes \mathbf{b}(v_d) \tag{3}$$

The size of the spatio-temporal steering vector depends on the temporal samples M and the number of antenna elements N used in the circular array. This spatio-temporal steering vector or the scanning vector $\mathbf{v}(v_s, v_d)$ will be used to scan the eight channel data denoted by $\mathbf{x}(k)$. At some specific range n, data received on each channel of array

is mixed with the time-delayed version of the reference signal. This mixing product $\mathbf{x_m}(k; n)$ is given by:

$$\mathbf{x_m}(k; n) = \mathbf{x}(k) \circ (1 \otimes \mathbf{x_{ref}}(k - n))^* \tag{4}$$

The mixing product was sub-sampled to obtain the lexically ordered sub-sampled signal $\mathbf{x_s}(n)$ given by [8]:

$$\mathbf{x_s}(n) = \left[\mathbf{x_m^T}(0; n), \mathbf{x_m^T}(S; n), \ldots, \mathbf{x_m^T}((M - 1)S; n)\right]^T \tag{5}$$

To find the angle-Doppler information of targets and main transmitter (clutter) from the received data, matched filtered output y_m can be calculated by using spatio-temporal steering vector in (3) and the sub-sampled signal in (5), which is given by:

$$y_m(v_s, v_d; n) = \mathbf{v}^\dagger(v_s, v_d)\mathbf{x_s}(n) \tag{6}$$

where, $\dagger$ represents Hermitian transpose operation. The last step in STAP processing, optimum matched filtering, was used to filter out the clutter contributions consisting of transmitter signature at zero Doppler frequency to get the target signature. This processing requires the calculation of interference and noise covariance matrix R. The model covariance matrix was used in our simulation. Many other approaches exist for calculating a more precise covariance matrix [8]. The optimum matched filter output can be calculated as:

$$y(v_s, v_d; n) = \mathbf{w}^\dagger(v_s, v_d)\mathbf{x_s}(n) \tag{7}$$

where, $\mathbf{x_s}(n)$ is the recorded sub-sampled signal and $\mathbf{w}$ is the optimum filter weight vector given by

$$\mathbf{w}(v_s, v_d) = R^{-1}\mathbf{v}(v_s, v_d) \tag{8}$$

where, R is the estimate of the interference covariance matrix. In practical, estimation of R requires large number of training data samples, and also is very difficult to estimate in the case of passive radar from actual data. Therefore, a model interference covariance matrix was used for this scenario [8, 28].

The basic steps involved in the STAP process from data reception to target detection are given by:

- First, the eight channel data signal received from the circular antenna array is pre-processed in order to remove the mutual coupling effects and apply the phase and amplitude correction [19].
- The pure reference signal is extracted from the received array data using adaptive beamforming [20].
- The eight channel data signal is mixed with the pure reference signal using the mixing product using (4).

- The spatial and temporal steering vectors given by (1) and (2) are used to calculate spatio-temporal steering vector also known as scanning vector given by (3).
- Matched filtering of (3) and (5) is performed in order to obtain angle-Doppler information of the targets and interferences using (6) as shown in Fig. 3.
- Interference covariance matrix is calculated to obtain the weight vector which suppresses the zero-Doppler direct path interferer given by (8).
- Finally, the weight vector is used by optimum matched filtering given by (7), in order to get pure target signature as shown in Fig. 4.
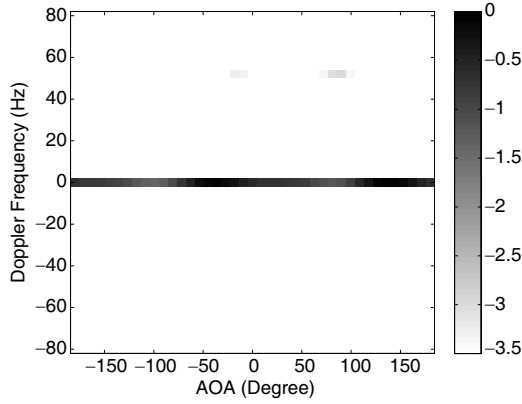
Figure 3. Matched filter output.
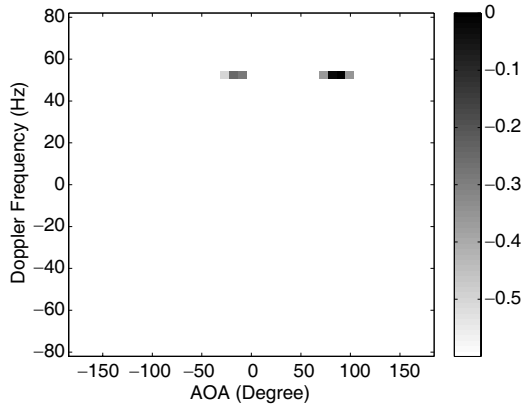
Figure 4. Optimum matched filter output.

3. DATA PROCESSING RESULTS

All the signal processing steps in Fig. 2, were first implemented in MATLAB environment which will be discussed in this section. Secondly, the signal processing steps for STAP processor, implemented on Xilinx Virtex-6 FPGA will be discussed in Section 4. The data reception scenario contains a non-cooperative FM transmitter at 924 MHz installed 600 meters away from the circular antenna array. A single target vehicle, moving towards the array at around 90° with a speed of 60 km/h. After receiving the eight channel signal, post-processing of the data was performed using MATLAB. This results in separating the pure reference signal from the received eight channel data signal [20]. The reference and eight-channel data signals are then fed to STAP processor. The adaptive matched filter output using (6) is shown in Fig. 3, which confirms the transmitter at −30° with zero-Doppler frequency and a very weak moving target signature at 90° with 52 Hz Doppler.

Optimum matched filtering using (7) is then used to effectively remove the zero-Doppler frequency components as shown in Fig. 4, and leaving the very strong target signature.
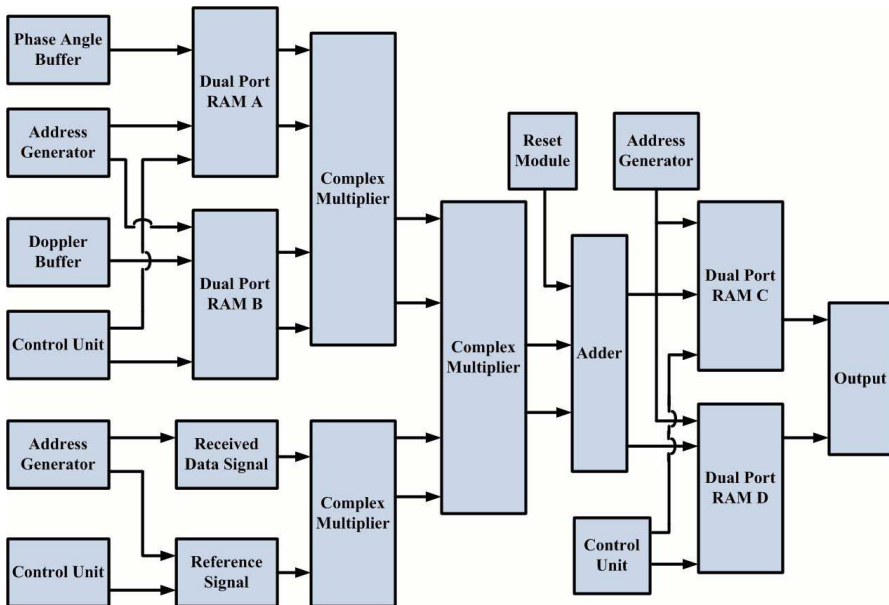

Figure 5. STAP processing blockset designed for FPGA.

4. HARDWARE IMPLEMENTATION

The challenging part of our research lies in the FPGA implementation of STAP algorithm on passive bistatic radar using uniform circular array. We want to develop a compact, light-weight and high-speed passive radar system on which STAP algorithm can be implemented. In this paper, Xilinx Virtex-6 FPGA was used to design the data processing steps of STAP, as shown in Fig. 5; initially for post-processing of the received data.

The designed model includes phase-angle and Doppler-bin buffers that scan the received data to find the respective target bearing angle and Doppler. Various control blocks were used to control the input data to perform respective tasks of STAP processor. Address generator block was used to assign the addresses to the input data when arrived at the input of dual-port RAM blocks. As the received data is complex, therefore, complex multipliers are needed for all multiplication operations. The adder block was used for multiplication operations to add every row of data and store the value at specific RAM address.

The FPGA implemented version of designed STAP processing block-set is shown in Fig. 6. The scanning matrix block-set generates
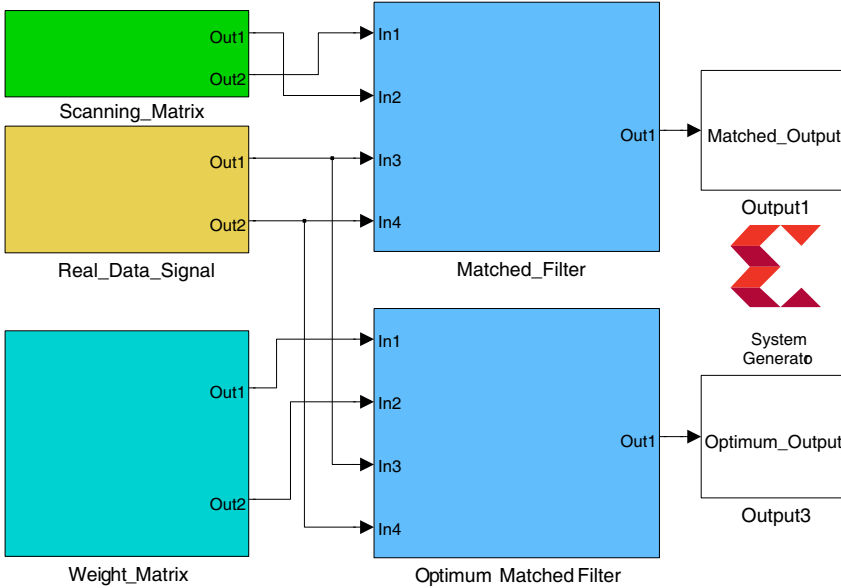
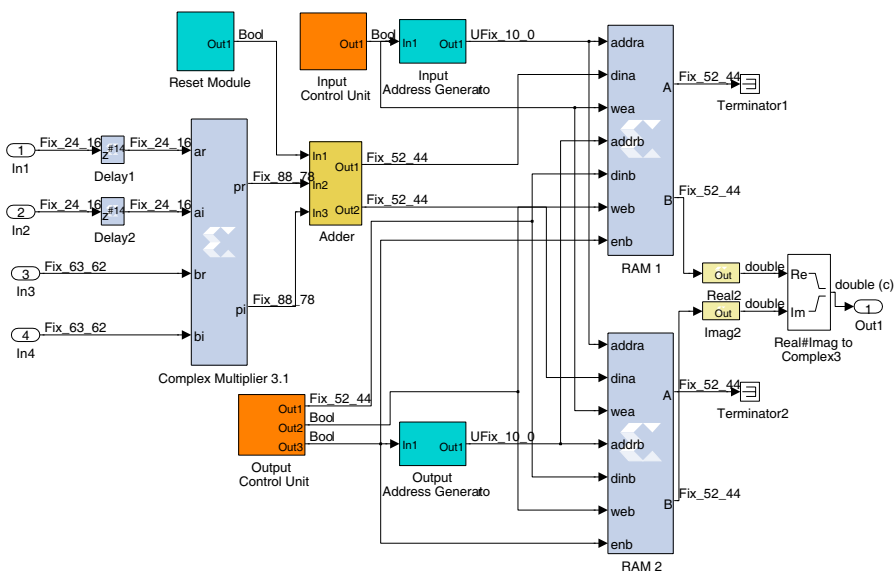**Figure 6.** FPGA implemented STAP processing.

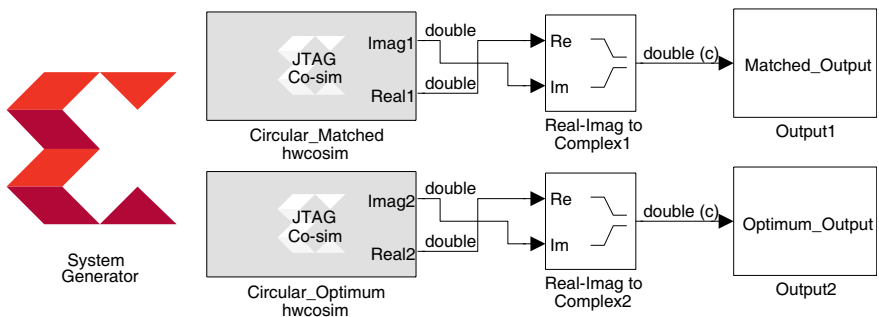**Figure 7.** FPGA matched filter processing.

Figure 8. Hardware co-simulation model.

the spatial and temporal scanning vectors to identify estimated location of the target. The real data signal block-set generates the target signal mixing module process. The weight matrix block-set directly loads the required weights for optimum matched filtering. A basic matched filter processing blockset was designed as shown in Fig. 7 which was used by both matched filter and optimum matched filter blocksets as shown in Fig. 6. By changing the inputs and FPGA clock, the matched filter blockset was reused for optimum matched filtering.

In order to run the STAP process directly over FPGA using Xilinx
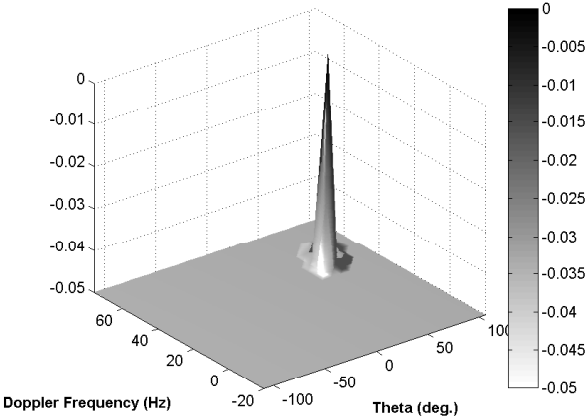
Figure 9. Optimum matched filter output from FPGA.

Table 1. Resources and power utilization summary of matched filtering.

On-Chip Components	Available	Matched Filtering		Power
		Used	Utilized (%)	(W)
Flipflops	301440	1993	0.7	0.09
Slice LUT's	150720	1704	0.01	0.03
Block RAM's	416	8	1.9	0.125
IO's	600	203	33.8	0.418
DSP48E1's	768	40	5.2	0.039
Leakage Power	-			3.443
Total Power	-			4.145

System Generator, hardware co-simulation model as shown in Fig. 8 was needed which takes the received target data from computer and manipulates it separately with matched filtering and optimum matched filtering and transfers the result back to computer to display the angle-Doppler plot of the target as shown in Fig. 9. The obtained results are in good agreement with MATLAB processing result as shown in Fig. 4.

4.1. Hardware Timing and Power Analysis

The next step in FPGA implementation is to find out the computational and the power requirements. The results of the timing

Table 2. Resources and power utilization summary of optimum matched filtering.

On-Chip Components	Available	Optimum Matched Filtering		Power (W)
		Used	Utilized (%)	
Flipflops	301440	1283	0.42	0.08
Slice LUT's	150720	3197	0.02	0.012
Block RAM's	416	336	80.77	0.068
IO's	600	209	34.83	0.248
DSP48E1's	768	24	3.125	0.011
Leakage Power	-			3.435
Total Power	-			3.854

Table 3. Computation time and frequency analysis.

Processing	MATLAB Processing (sec)	FPGA Processing (nsec)	Maximum FPGA Freq. (MHz)
Matched Filtering	7	4.964	201.450
Optimum Matched Filtering	9.8	9.944	100.563

and power analysis of matched filtering and optimum matched filtering are presented in Table 1 and Table 2 respectively. The results show that the process of matched filtering requires more power while utilizing less resources as compared to the process of optimum matched filtering which requires less power while utilizing more on-chip resources.

The timing analysis as shown in Table 3, shows a huge difference between MATLAB and FPGA processing time. It is also observed that the matched filtering process requires less FPGA clock period as compared to optimum matched filtering because it uses less resources as compared to optimum one. The maximum frequency required by FPGA depends on the FPGA clock period. The lesser the clock period of FPGA, greater will be the operating FPGA frequency and vice versa.

5. CONCLUSION

MATLAB Simulation and the hardware implementation of STAP algorithm for Passive Bi-static Radar (PBR) using uniform circular array was presented. This implementation was verified with the

real field experimental data using FM as transmitter of opportunity. The results are based on offline processing of the data, both for MATLAB and FPGA processing. The MATLAB processing results along with the FPGA output shows that the zero-Doppler clutter can be effectively filtered out by using optimum matched filtering. Future work will focus on real-time target detection using STAP processing to achieve a dedicated radar system for the proposed technique.

ACKNOWLEDGMENT

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