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A MODIFIED MICROSTRIP WILKINSON POWER DIVIDER WITH HIGH ORDER HARMONICS SUPPRESSION

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Abstract—In this paper, a modified Wilkinson power divider structure with three order harmonics suppression is presented. The quarter-wavelength microstrip lines in the traditional Wilkinson power divider (WPD) are replaced by two transmission line segments with ends connected (TTLWEC). The TTLWEC performs the functions of impedance transformation and three order harmonics suppression. The design equations are deduced by odd- and even-mode theory. An example of power divider operating at 1 GHz is designed and fabricated based on the printed circuit board technology. The measured results of 3.13 dB insert loss (IL) and 35 dB return loss (RL) are obtained at the operating frequency, and the first, second and third harmonic harmonics suppressions are −38 dB, −44 dB and −39 dB, respectively, which agree well with the simulated results and validate the availability of the proposed structure.

1. INTRODUCTION

The Wilkinson power divider (WPD) is widely used in various microwave modules and systems [1–4] for signal spitting or combining. The conventional WPD consists of two quarter-wavelength transmission-line sections at the operating frequency, which result in the presence of spurious passbands. In recent years, some new WPD with multiband operating frequencies [5–11] or harmonic suppression [12–18] have been proposed. These structures are proposed to simplify the circuit structure and reduce the circuit area. The WPD with harmonics suppression integrated the reject harmonic frequencies module in the WPD, thus extra filters for filtering the harmonic frequencies are left out, which makes the circuit more compact.

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In [12], Woo and Lee use defected ground structures (DGS) to finish two order harmonics suppression. In [13], electromagnetic band gap (EBG) structures are added to the conventional WPD for harmonics suppression. Both the DGS and EBG structures need additional etch process besides the standard printed circuit board process, which complicates the circuit fabrication. Meanwhile, these structures cannot obtain the closed solution for designing. In [14], a compact WPD with second order harmonics suppression by the anti-coupled line is proposed, which shows unsatisfied return loss for some mismatching at the input and output ports. In [15], Wang et al. use four microstrip high-low impedance resonator cells to achieve harmonics suppression. Spur-lines are used to achieve the stopband at the spurious frequency in [16]. In [17, 18], the methods for one order harmonic suppression are presented. It is significant to proposed a method for the design of a WPD with high orders harmonics suppression, closed form solution, and fully matching at the input and output ports.

Based on the wideband bandstop filters demonstrated in [19], we propose a new configuration for designing WPD with harmonics suppression. The design equations of the proposed WPD are deduced based on the odd-and even-mode theory. Section 2 deduces the design equations, and Section 3 gives the compassion of the circuit simulated and measured results.

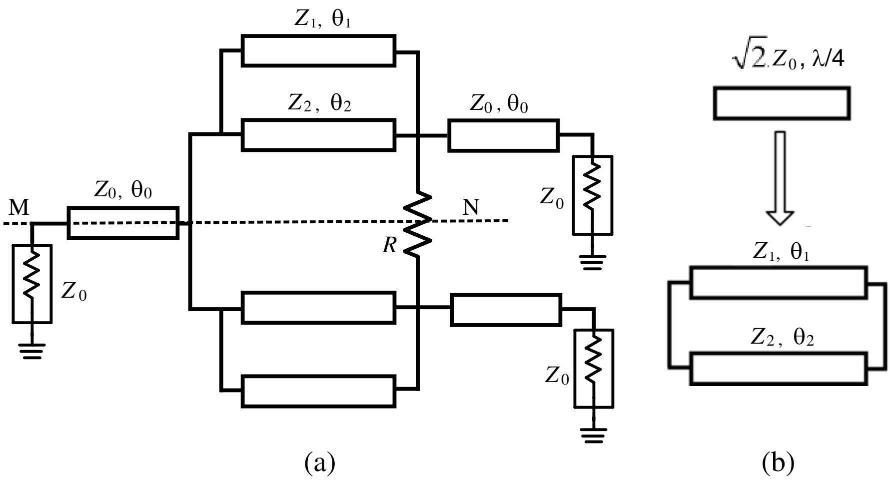

Figure 1. (a) The structure of the proposed WPD. (b) Distinction between the conventional and proposed WPD.

2. DESIGN AND ANALYSIS

The proposed structure is shown in Figure 1(a). The quarter-wavelength lines in the conventional WPD are replaced by two parallel transmission lines with ends connected (Figure 1(b)), whose characteristic impedances are Z_1 and Z_2, and electrical lengths are θ_1 and θ_2, respectively. Microstrip lines with impedance Z_0 and electrical length θ_0 act as feed lines. The structure is symmetric with plane M-N, thus we can apply even- and odd-mode analysis to obtain the circuit design equations.

2.1. Even-mode Analysis

Based on the lossless transmission line models, when the TTLWEC are terminated the load impedance Z_L as shown in Figure 2, the input impedance can be calculated as follows [19]

$$Z_{in} = \frac{Z_1 Z_2 - jZ_L(Z_2 \cot\theta_1 + Z_1 \cot\theta_2)}{Z_L(k + 1/k + 2h) - j(Z_2 \cot\theta_1 + Z_1 \cot\theta_2)} \tag{1}$$

where $k = Z_1/Z_2$, and

$$h = \csc\theta_1 \csc\theta_2 - \cot\theta_1 \cot\theta_2. \tag{2}$$

For even-mode excitation, there is no current flow through M-N plane, thus the circuit is bisected along MN. Figure 3(a) depicts the even-mode equivalent circuit. Input impedance can be calculated when substituting $Z_L = 2Z_0$ into (1)

$$Z_{\text{even}} = \frac{Z_1 Z_2 - j2Z_0(Z_2 \cot\theta_1 + Z_1 \cot\theta_2)}{2Z_0(k + 1/k + 2h) - j(Z_2 \cot\theta_1 + Z_1 \cot\theta_2)} \tag{3}$$

We suppose that the operating frequency of the WPD is f_0, thus the first, second and third harmonics are $f_1 = 2f_0$, $f_2 = 3f_0$ and $f_3 =$

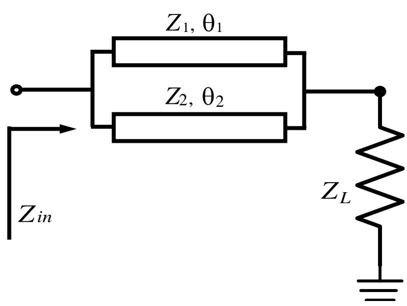

Figure 2. The TTLWEC terminated load impedance Z_L.

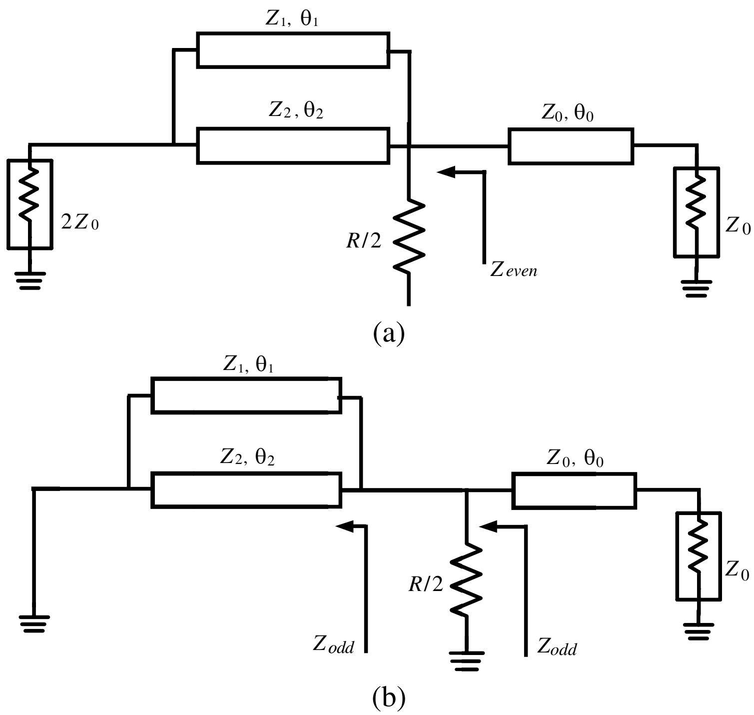

Figure 3. (a) Equivalent circuit for even-mode excitation. (b) Equivalent circuit for odd-mode excitation.

$4f_0$, respectively. For obtaining excellent suppression performances and keeping the area as compact as possible, the values $\theta_1 = \pi$ and $\theta_2 = 2\pi$ at f_2 are chosen [19]. The electrical lengths at f_0 give

$$\theta_1(f_0) = \pi/3 \tag{4}$$

$$\theta_2(f_0) = 2\pi/3 \tag{5}$$

From (1), (4) and (5), the input impedance at f_0 can be obtained as follows,

$$Z_{\text{even}}(f_0) = \frac{Z_1Z_2 - j2Z_0(Z_2 - Z_1)/\sqrt{3}}{2Z_0(k + 1/k + 10/3) - j(Z_2 - Z_1)/\sqrt{3}} \tag{6}$$

The condition for terminal impedance matching is

$$Z_{\text{even}}(f_0) = Z_0 \tag{7}$$

For the supposition of Z_0 is real impedance (usually $50\,\Omega$), the impedance of the parallel transmission lines should be satisfied

$$\text{imag}(Z_{\text{even}}(f_0)) = 0 \tag{8}$$

We can obtain,

$$Z_1 - Z_2 = 0 \tag{9}$$

Then substituting (7) and (9) into (6), after some calculating, the condition for even mode terminal impedances matching can be obtained as

$$Z_1 = Z_2 = 4\sqrt{2}Z_0/\sqrt{3} \tag{10}$$

2.2. Odd-mode Analysis

For odd-mode excitation, the virtual ground is along the middle of the proposed WPD. The equivalent circuit is illustrated in Figure 3(b). The input impedance (except $R/2$) $Z'_{\text{odd}} = \infty$, thus the impedance seen from port2 can be calculated as follows,

$$Z_{\text{odd}} = \frac{R}{2}//Z'_{\text{odd}} = \frac{R}{2}//\infty = R/2 \tag{11}$$

For the odd-mode port impedance matching condition, we can obtain the equation,

$$R = 2Z_0 \tag{12}$$

2.3. Harmonic Suppression Analysis

From the equations deduced in sections 2.1 and 2.2, it can be concluded that the TTLWEC performs impedance transverse in the proposed WPD. This section we will analyze the theory of harmonics suppression.

For analyzing the harmonics suppressions, we discuss the input impedance at port1. The structure in Figure 1(a) can be redrawn as shown in Figure 4 where R is removed since this situation is similar to an even mode excitation at port2 and port3 [20]. We now have the parallel connection of TTLWEC with terminal impedance $Z_L = Z_0$. From (1) and (10), after some calculations, the input impedance can be written as

$$Z_{in} = \frac{8Z_0 - j\sqrt{6}Z_0(\cot\theta_1 + \cot\theta_2)}{3(1+h) - j2\sqrt{6}(\cot\theta_1 + \cot\theta_2)} \tag{13}$$

For the value demonstrated in (4) and (5), we have $\theta_1 = 2\pi/3$ and $\theta_2 = 4\pi/3$ at f_1, thus the input impedance at f_1 is

$$Z_{in}(f_1) = \frac{8Z_0 - j\sqrt{6}Z_0(\cot(2\pi/3) + \cot(4\pi/3))}{3(1+h) - j2\sqrt{6}(\cot(2\pi/3) + \cot(4\pi/3))} = \infty \tag{14}$$

where $h = \csc(2\pi/3)\csc(4\pi/3) - \cot(2\pi/3)\cot(4\pi/3) = -1$.

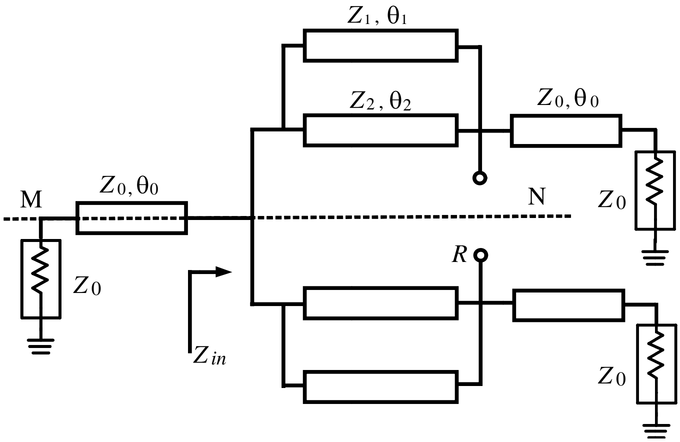

Figure 4. The circuit for analyzing harmonics suppression.

Thus the reflectance at f_1 (at port1) can be calculated as follows

$$S_{11}(f_1) = \lim_{Z_{in}(f_1)\to\infty} \frac{Z_{in}(f_1) - Z_0}{Z_{in}(f_1) + Z_0} = 1 \tag{15}$$

Equation (15) shows that the first order harmonic is suppressed totally.

For the value $\theta_1 = \pi$ and $\theta_2 = 2\pi$ at f_2, the input impedance is

$$Z_{in}(f_2) = \frac{8Z_0 - j2\sqrt{6}Z_L(\cot(\pi) + \cot(2\pi))}{3(1+h) - j2\sqrt{6}(\cot(\pi) + \cot(2\pi))} = 0 \tag{16}$$

where $h = \csc(\pi)\csc(2\pi) - \cot(\pi)\cot(2\pi) = \infty$. Thus the reflectance is

$$S_{11}(f_2) = \lim_{Z_{in}(f_2)\to 0} \frac{Z_{in}(f_2) - Z_0}{Z_{in}(f_2) + Z_0} = -1 \tag{17}$$

Similarly, substituting $\theta_1 = 4\pi/3$ and $\theta_2 = 8\pi/3$ (at f_3) into (13), the input impedance and reflectance can be deduced as follows,

$$Z_{in}(f_3) = \frac{8Z_0 - j\sqrt{6}Z_k(\cot(4\pi/3) + \cot(8\pi/3))}{3(1+h) - j2\sqrt{6}(\cot(4\pi/3) + \cot(8\pi/3))} = \infty \tag{18}$$

where $h = \csc(4\pi/3)\csc(8\pi/3) - \cot(4\pi/3)\cot(8\pi/3) = -1$.

$$S_{11}(f_3) = \lim_{Z_{in}(f_3)\to 0} \frac{Z_{in}(f_3) - Z_0}{Z_{in}(f_3) + Z_0} = 1 \tag{19}$$

Equations (15), (17) and (19) show that the signal is reflected totally at f_1, f_2 and f_3, thus the first three harmonics can be suppressed. So we can conclude that when TTLWECs replace the quarter-wavelength microstrip lines in the WPD, all the port impedances are fully matched at the operating frequency and the first three order harmonics suppression achieved simultaneously.

3. SIMULATION AND EXPERIMENT RESULTS

A modified Wilkinson power divider is designed based on the analysis in Section 2 for validating the proposed structure. The example WPD operates at 1 GHz, and the frequencies 2\3\4 GHz are the objective harmonics for suppression. A photograph of fabricated power divider is shown in Figure 5, where the dielectric substrate used for designing is Taconic TLX-8 with dielectric constant 2.55, thickness 1.575 mm, and loss tangent 0.002 at 10 GHz. Based on the formulas derived above, the widths of TTLWECs are set as 0.26 mm. An isolation resistance (100 Ω) is added between port2 and port3. Figure 6 and Figure 7 illustrate the measured and simulated IL as a function of frequency for the port1/port2 and port1/port3, respectively. The IL is about 3.13 dB at 1 GHz, and the attenuation of the signals at first threes orders harmonics is all above 35 dB. The results of $|S_{11}|$ and $|S_{22}|$ versus the frequency are depicted in Figure 8. The measured input port RL at operating frequency is about 27 dB, and the output port RL is better than 35 dB. Thus the circuit provides excellent RL both in the input port and output ports. Figure 9 demonstrates the measured and simulated results of the isolation between two output ports, which show good agreement with each other. The measured isolation is above 32 dB at the designing frequency, which is much better than the

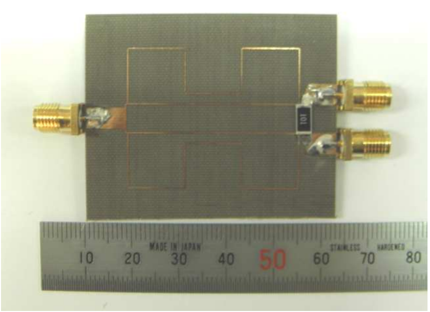

Figure 5. Photograph of the fabricated WPD.

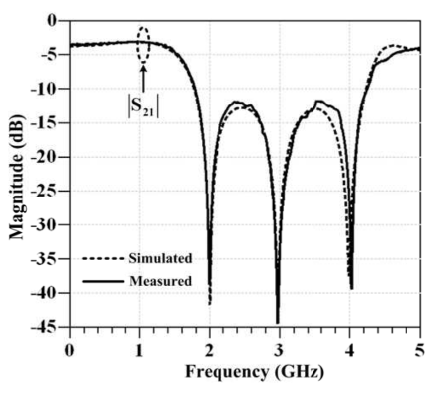

Figure 6. $|S_{21}|$ versus frequency.

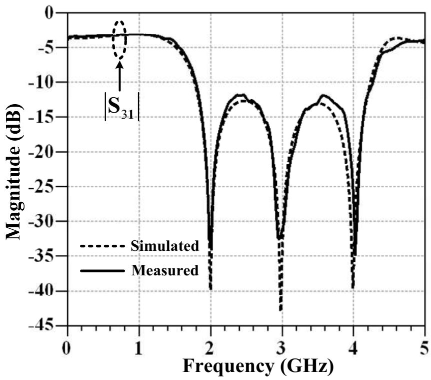

Figure 7. $|S_{31}|$ versus frequency.

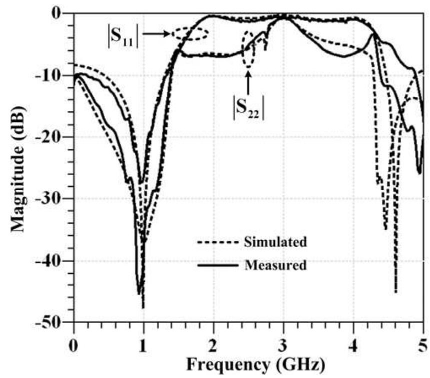

Figure 8. $|S_{11}|$ and $|S_{22}|$ versus frequency.

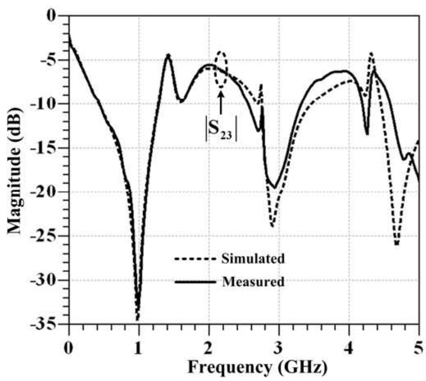

Figure 9. $|S_{23}|$ versus frequency.

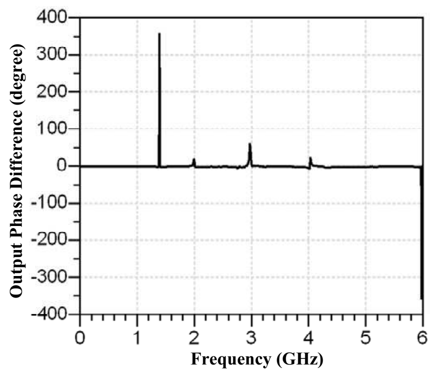

Figure 10. Output phase difference versus frequency.

results produced in [12–14]. The measured output phase difference between port2 and port3 is displayed in Figure 10, which shows pretty small difference at the operating frequency. All the results indicate that the proposed WPD performs well at operating frequency; meanwhile, the first three spurious passbands are suppressed to the excellent level. Additionally, the simulated results are implemented applying the software ADS 2009, and the measure results are performed using Agilent N5230A network analyze. The small discrepancies are attributed mainly to the tolerance (0.015 mm) in fabrication and implementation.

4. CONCLUSION

This paper presents a modified Wilkinson power divider with harmonics suppression. The designing equations are deduced based on the even- and odd-mode theory. A power divider operating at 1 GHz is designed and fabricated, and the measured results agree excellently with calculation and simulation, which fully demonstrate the validity of the structure. The main advantages of the proposed structure include: 1) planar structure; 2) closed-form design method; 3) three order harmonics suppression.

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