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DIFFERENTIAL TRANSFORMER USING BONDER-WIRES AND PATTERNS ON A PRINTED CIRCUIT BOARD FOR RF CIRCUIT APPLICATIONS

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Abstract—A transformer that uses bonder-wires and printed circuit board (PCB) patterns is proposed for RF circuit applications. The proposed transformer can be constructed without any additional processes. The PCB patterns are implemented using a typical FR4 substrate and gold bonder wires are used. The self-inductance of the transformer can be controlled according to the number of unit-transformers. Although the size of the transformer is larger than that of a fully-integrated transformer, the maximum available gain (MAG) is almost identical to that of other-types of transformers, which require additional cost or bulky size to obtain sufficient inductance. Additionally, we proposed a method to design the transformer with a symmetric structure for differential RF CMOS circuit applications. The transformer can applied to GHz-order RF CMOS circuits as an input and output matching component with low loss characteristics.

1. INTRODUCTION

A transformer is one of the key components of RFICs [1–8]. Recently most RFICs have been designed using a CMOS process to reduce overall cost [9–14]. However, gain reduction problems induced by the bonder-wires at the ground PAD have arisen, because, in general, no through substrate via process is provided in the CMOS process [15]. Thus, most RFICs implemented using CMOS processes are designed with a differential structure to generate a virtual ground node [16]. However, the input node of Tx and Rx antennas is designed with a single-ended structure.

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A balun is required to interconnect the antenna with a single-ended structure and RFICs with a differential structure [17]. One of the most widely used components for the balun is a transformer. The transformer is thus regarded as an essential component for the input/output matching networks of RF CMOS ICs. If a transformer is used as the output matching network, the quality-factor or maximum available gain (MAG) of the transformer directly influences the efficiency of the RFIC. On the other hand, if the transformer is used as an input matching network, the loss induced by the transformer degrades the noise figure of the overall circuits.

In this work, we propose a transformer using bonder-wires and PCB patterns aimed at reducing the overall cost and loss and enhancing the MAG.

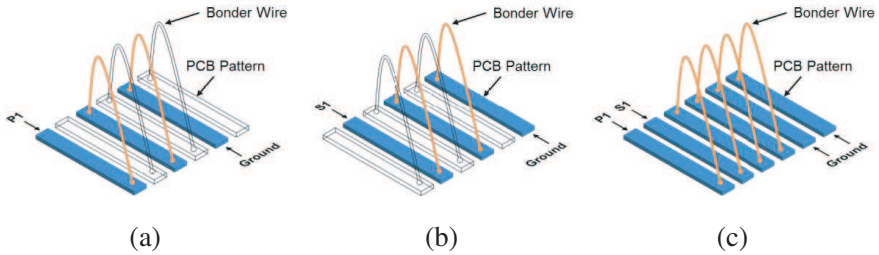
2. PROPOSED TRANSFORMER USING BONDER-WIRES AND PCB PATTERNS

2.1. Conventional Transformers

Although a fully-integrated transformer can reduce the overall system size and cost, the low MAG of the transformer seriously degrades the performance of RFICs. Numerous studies have attempted to improve the MAG of the transformer and reduce the bulky size [18].

On the other hand, some research groups have proposed RFICs that employ an off-chip transformer [19–21] to improve the overall efficiency. An off-chip transformer using a printed circuit board (PCB) pattern was introduced in a previous work [19]. Although a power amplifier using a PCB transformer provides high efficiency compared to a power amplifier using a fully-integrated transformer, bulky size is required to obtain the desired inductance of the primary part of the transformer. Additionally, the variation of PCB resolution directly distorts the operation frequency of the RFICs, because the PCB transformer is entirely implemented using a PCB pattern. It is therefore difficult to adapt the PCB transformer to GHz-order RFIC applications.

Another off-chip type of transformer using integrated passive device (IPD) technology for RF power amplifier applications has also been introduced [20, 21]. The IPD transformer has more compact size and higher resolution than the PCB transformer. The problems of the PCB transformer can be thus resolved by using the IPD transformer. However, cost problems compared to fully-integrated RFICs remain, because an additional process is required for the IPD transformer.



(a) (b) (c)

Figure 1. Conceptual structure of proposed transformer: (a) Primary part, (b) secondary part, and (c) overall structure.

2.2. Proposed Transformers

In this work, we propose a transformer using bonder-wires and PCB patterns. Unlike the IPD transformer, an additional process that increases the overall cost is not required for the proposed transformer. The desired inductance can be easily obtained compared to the PCB transformer. The proposed transformer can be a step towards realizing fully-integrated RFICs.

Figure 1 shows the conceptual structure of the proposed transformer. The transformer is composed of bonder wires and PCB patterns. As shown in Fig. 1, a primary part and a secondary part are located alternately. Magnetic coupling between the primary and secondary parts occurs at the PCB pattern and bonder-wires. Loss induced by the transformer is expected to be lower than a fully-integrated transformer, because the resistivity of the PCB patterns and bonder-wires is much lower than that of integrated metal lines in general.

Additionally, the inductance and magnetic coupling can be controlled by two different methods. First, a loop of the bonder wires can be used to control the inductance and magnetic coupling. The number of unit transformers, as shown in Fig. 2, can also be controlled to obtain desired inductance and magnetic coupling. The parasitic inductance induced by the transformer can be used to cancel out the parasitic capacitance that occurs at the input/output node of the RFICs. Thus, the proper parasitic inductance must be designed according to the operating frequency and the desired output power of RFICs. For example, the desired inductance decreases as the desired output power increases.

As described in the previous section, a differential structure is generally employed in RF CMOS ICs. Thus, if the transformer is used as a component of the output matching network, differential

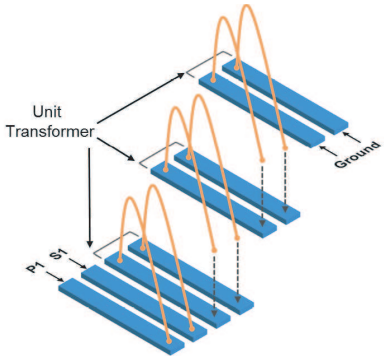
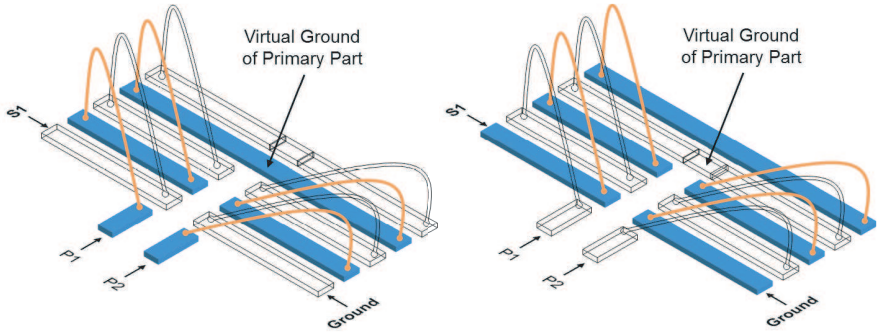


Figure 2. Unit transformer of the proposed transformer.



(a) (b)

Figure 3. Conceptual structure of proposed transformer for differential applications: (a) Primary part and (b) secondary part.

ports are required at the primary part to convert the differential signal to a single-ended signal. For the differential input of the transformer at the primary part, a symmetric structure using the unit transformer of Fig. 2 is required. The structure of the proposed transformer for differential ICs applications is shown in Fig. 3. To obtain symmetric properties of the primary part, P1 and P2, the transformer is constructed using the transformer shown in Fig. 2 as a unit transformer. A virtual ground occurs at the center of the primary part, as shown in Fig. 3.

3. EXPERIMENTAL RESULTS

We designed the proposed transformer using FR4 PCB and gold bonder-wires and measured the *s*-parameters using a 4-port network

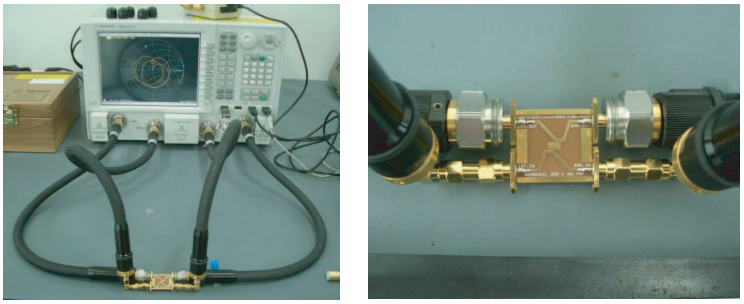


Figure 4. Measurement setup using 4-port network analyzer.

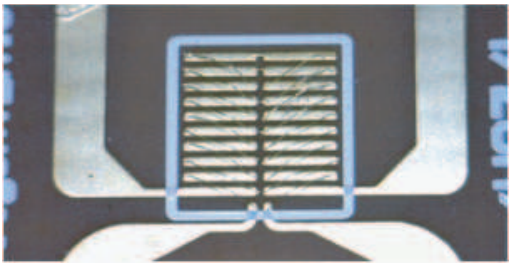


Figure 5. Photograph of designed transformers for differential applications with 20 bonder-wires (transformer size: $3 \times 3\,\mathrm{mm}^2$).

analyzer, as shown in Fig. 4. Fig. 5 shows the implemented transformers with 20 bonder-wires. The metal width is 200 µm, the metal length is 1450 µm, the space between adjacent metal lines is 100 µm, and the metal thickness is 18 µm. The feeding lines for the measurement setup are de-embedded. The total size of the transformer is $3 \times 3\,\mathrm{mm}^2$. The self-inductance of the primary part between port P1 (or port P2) and the virtual ground is approximately 8 nH. However, the inductance can be controlled according to the number of PCB patterns. For example, we easily implemented a transformer with 10 bonder-wires to reduce the inductance compared to a transformer with 20 bonder-wires.

Figure 6 shows the measured MAGs of the transformers. A maximum MAG of -0.8 dB was obtained at an operating frequency of 1.0 GHz for the transformer with 10 bonder-wires, and a value of -0.75 dB was obtained at 0.7 GHz for the transformer with 20 bonder-wires. The MAG was higher than -1 dB at a range from 0.5 to 1.2 GHz.

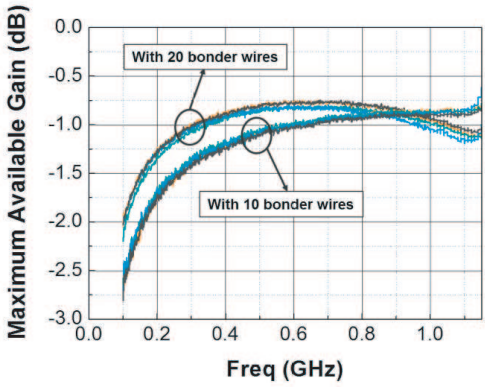


Figure 6. Measured maximum available gain of the transformer.

Table 1. Comparison of transformers.

Transformer type	Ref.	MAG [dB]	Size [mm^2]	Freq. [GHz]	Additional process	Results from
Fully-Integrated	[15]	−1.700	1.0 × 1.0	1.900	×	simulation
	[16]	−1.170	0.9 × 1.0	1.800	×	simulation
IPD	[20]	−0.810	0.7 × 0.9	1.800	O	simulation
	[21]	−0.390	1.2 × 1.4	1.900	O	simulation
PCB	[19]	−0.238	2.4 × 5.1∗	0.875	×	simulation
PCB + Bonder-wire	This work	−0.800	3.0 × 3.0	0.900	×	measurement

*The CMOS power amplifier is partially located in the transformer.

Table 1 provides a comparison of various types of transformers with size, loss, operation frequency, and requirement of an additional process. As described in Table 1, the MAG of this work is lower than that of previous works [19] and [21]. However, the IPD transformer requires an additional process and the PCB transformer of the previous work [19] has a metal thickness of 35 µm, which is two times greater than that of the proposed transformer, to reduce the parasitic resistance and enhance the coupling coefficient. Furthermore, the self-inductance of the primary part is approximately 1.9 nH, which is lower than that of the proposed transformer.

4. CONCLUSION

In this work, we proposed a transformer using PCB patterns and bonder-wires. Although the transformer has larger size than a fully-integrated transformer, it has lower loss without additional process cost. Additionally, we describe a method to construct a differential structure using the proposed unit transformer to allow application to differential RF CMOS circuits. The transformer is composed of a general FR4 PCB substrate and gold bonder wire, which is essential for the chip-on-board. From the measurement results, we verified the feasibility of the transformer, which has comparable maximum available gains to other types of off-chip transformers that require additional cost and bulky size. The proposed transformer can provide a stepping stone toward fully-integrated RF CMOS circuits. The transformer can be properly used in GHz-order CMOS circuits as the components of the input/output matching network and balun.

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