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A BROADBAND OUT-OF-PHASE POWER DIVIDER FOR HIGH POWER APPLICATIONS USING THROUGH GROUND VIA (TGV)

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Abstract—In this paper, we present a broadband out-of-phase power divider with high power-handling capability. The proposed device consists of several sections of double-sided parallel-strip lines (DSPSLs), a mid-inserted conductor plane, and two external isolation resistors, which are directly grounded for heat sinking. A through ground via (TGV), connecting the top and bottom sides of DSPSLs, is employed. The special metal via is realized to short the isolation resistors at full-frequency band when the odd-mode is excited. Meanwhile, it can be ignored as the excitation is even-mode. This property is efficiently utilized to improve the bandwidth. To examine the proposed power divider in detail, a set of closed-form equations are derived. Meanwhile, the power operation analysis illustrates that the proposed power divider is a good candidate for high power applications. The design charts show that the proposed device can support a wide frequency ratio range (1–1.7). Furthermore, broadband responses can be obtained when proper frequency ratios are adopted. For verification, an experimental power divider operating at 1.25/1.75 GHz is implemented. The measured results exhibit a bandwidth of 44.3% with better than 15 dB return loss and 18 dB port isolation is achieved.

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1. INTRODUCTION

RF subsystems are composed of many components [1–4]. Among these passive and active devices, power dividers are fundamental and important ones. Thus far, the Wilkinson power divider is the most widely used kind [5–13] since it features low insertion loss, perfect isolation, all ports matching and other advanced performances. Unfortunately, they are not suitable for balanced-circuits such as balanced mixers, multi-pliers and push-pull amplifiers due to their IN-PHASE responses. To achieve the out-of-phase features, much research has been conducted and different balanced transmission lines have been investigated [14–17]. For instance, microstrip-slot lines [14] and asymmetrical coplanar striplines (ACPSs) [15] are used to design out-of-phase power dividers. Recently, the double-sided parallel-strip line (DSPSL) becomes very popular in out-of-phase power divider designs. Both single- [16] and dual-band [17] power dividers have been presented by using DSPSLs. However, the isolation resistors of these dividers are integrated in the middle of the substrate, which makes the heat-sinking difficult. This drawback limits their high-power applications. To improve the power-handling capability, the authors have developed a novel power divider with external isolation resistors in [18]. The isolation resistors are directly grounded for heat dissipation, where they can be easily mounted on the cooling systems by adding a transmission line of the same characteristic impedance. However, the frequency ratio (m) of the power divider only covers the range of $1.62 < m < 3$. Meanwhile, the designed power divider is limited to achieve narrow bandwidth responses, which is the main restriction for potential industrial applications.

Therefore, in this paper, we propose a novel design of the power dividers to overcome the drawback of the limited band-width. The proposed power divider consists of a novel dual-band impedance matching network with two external isolation resistors. The resistors are grounded with a direct path for heat sinking. A through ground via (TGV), connecting both sides of the DSPSLs, is employed. The special via is realized to makes the isolation resistors shorted at full-frequency band when odd-mode is excited. Meanwhile, it can be ignored when the excitation is even-mode. This property is efficiently utilized to obtain broadband matching and isolation features. To analytically investigate the proposed power divider, a set of designed equations are derived base on the even- and odd-mode analysis method. For practical design process, design charts are also proposed by using these analytical equations. It is found that the proposed power divider can operate at two frequencies f_1 and mf_1 with a frequency ratio range at

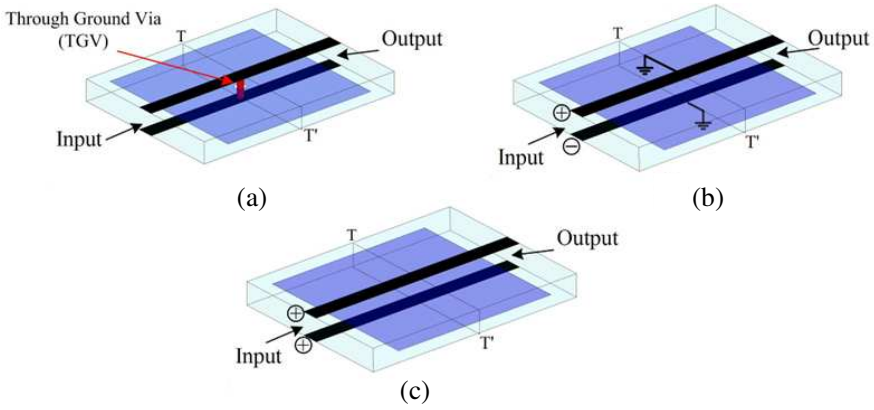


Figure 1. (a) 3-D view of the DSPSLs with a through ground via (TGV). (b) Equivalent circuit with odd-mode excitation. (c) Equivalent circuit with even-mode excitation.

$1 < m < 1.7$. By choosing the proper frequency ratio, the proposed broadband power divider can be designed. For verification, an example power divider with frequency ratio of 1.4 : 1 is implemented. The measured results show that a bandwidth of 630 MHz (44.3%) with better than 15 dB return loss and 18 dB port isolation is obtained. Since the proposed power divider simultaneously has the advanced performances including broadband matching/isolation, out-of-phase feature and high power capability, it is a perfect candidate for balanced high-power applications.

2. INVESTIGATION OF THROUGH GROUND VIA

Figure 1(a) shows the conventional DSPSL with a mid-inserted conductor plane as common ground. A metal via connects the top and bottom sides of the DSPSL at the reference face T-T' through the mid-inserted common ground. It is named as Through Ground Via (TGV). Therefore, at the reference face T-T', the voltage on the both sides of the DSPSL is equal.

For odd-mode excitation, the mid-inserted plane can be regarded as infinite ground [18, 19]. And the voltage along the DSPSL has identical amplitude but opposite phase. Thus, the voltage at the reference face T-T' must be equal to zero. The equivalent circuit is shown in Figure 1(b). This property can be used to short the isolation resistors loaded at the reference face T-T', when odd-mode is excited.

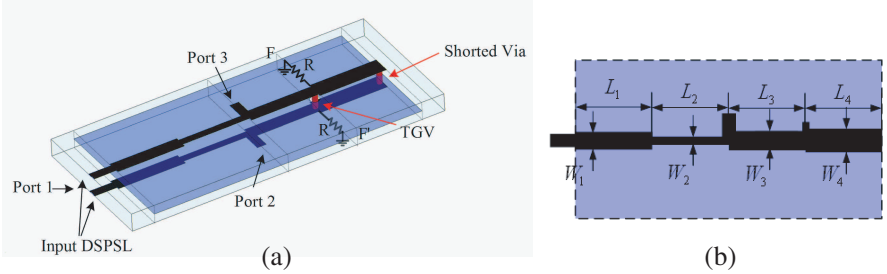


Figure 2. Layout of the proposed power divider. (a) Configuration. (b) Dimension.

For even-mode excitation, the voltage along the DSPSL has identical amplitude and phase. Thus, the TGV has no effect on the DSPSL and the equivalent circuit is shown in Figure 1(c). Emphatically, the defect of the mid-inserted plane is ignored since its dimension is very small compared the guided wavelength.

In addition, all the analysis above is frequency independent. This point can be utilized to improve the matching and isolation bandwidth in power divider designs.

3. CONFIGURATION AND ANALYSIS OF THE PROPOSED POWER DIVIDER

Figure 2(a) shows the configuration of the proposed broadband power divider. It consists of several sections of DSPSLs, two external isolation resistors, and a mid-inserted conductor plane as well as a through ground via (TGV). As discussed in [17, 19], the conductor plane segregates the DSPSLs to back-to-back microstrip lines, where it also acts as the common ground of the two output ports. Two circuits on the top and bottom layers have identical sizes, and all transmission lines have the same electrical length (θ). Figure 2(b) illustrates the dimensions of the top/bottom circuits. Since the proposed power divider is symmetrical, we can use even- and odd-mode method to extract the circuit parameters from the matching/isolation conditions. For convenience, all the impedance values in this paper are normalized with respect to input/output ports impedance ($Z_0 = 50\,\Omega$).

3.1. Odd-mode Analysis

For the odd-mode analysis, the mid-inserted plane can be regarded as the infinite ground, and the impedance of port 1 is split to be half of the

initial value [17–19]. Meanwhile, the voltages along the transmission lines on the top and bottom layers have the same magnitude and opposite phase. Since the TGV connects the DSPSLs together, the voltage of the DSPSLs at the plane F-F' has satisfied to be zero. In this case, the isolation resistors are shorted and the odd-mode equivalent circuit of the proposed power divider can be simplified as shown in Figure 3. Emphatically, all the impedance parameters (z_1, z_2, z_3), in this paper, represent the values of microstrip lines.

Mathematically, the $ABCD$ matrix of the two-port network can be calculated as [20]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta & jz_1\sin\theta \\ j\frac{1}{z_1}\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \cos\theta & jz_2\sin\theta \\ j\frac{1}{z_2}\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{jz_3\tan\theta} & 1 \end{bmatrix} \quad (1)$$

where

$$A = \cos^2\theta - \frac{z_1}{z_2}\sin^2\theta + \frac{z_2}{z_3}\cos^2\theta + \frac{z_1}{z_3}\cos^2\theta \quad (2a)$$

$$B = j(z_1 + z_2)\sin\theta\cos\theta \quad (2b)$$

$$C = j\left(\frac{1}{z_1} + \frac{1}{z_2}\right)\sin\theta\cos\theta + j\frac{z_2}{z_1 z_3}\sin\theta\cos\theta - j\frac{1}{z_3}\frac{\cos^2\theta}{\tan\theta} \quad (2c)$$

$$D = -\frac{z_2}{z_1}\sin^2\theta + \cos^2\theta \quad (2d)$$

Subsequently, the input impedance of the circuit may thus be expressed as

$$z_{in} = \frac{A + B}{C + D} \quad (3)$$

Then, the matching condition at port 1 becomes

$$z_{in} = 1/2 \quad (4)$$

By combining (2)–(4), we obtain

$$z_2 = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \quad (5a)$$

$$z_3 = \frac{2(z_1 + z_2)}{\left(2\frac{z_1}{z_2} - \frac{z_2}{z_1}\right)\tan^2\theta - 1} \quad (5b)$$

where

$$a = 4 + \frac{\tan^2\theta}{z_1^2} \quad (6a)$$

$$b = 8z_1 - \frac{2}{z_1} \quad (6b)$$

$$c = 4z_1^2 - 2\tan^2\theta - \frac{1}{\tan^2\theta} - 4 \quad (6c)$$

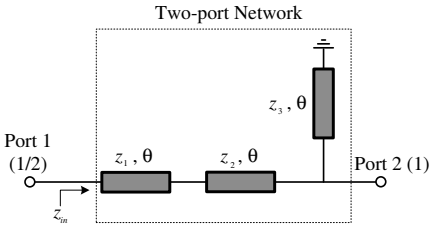


Figure 3. Equivalent circuit of the power divider for odd-mode excitation.

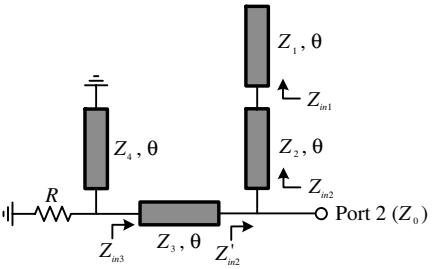


Figure 4. Equivalent circuit of the power divider for even-mode excitation.

To fulfill the dual-band impedance matching condition, the electrical length (θ) of the transmission lines at f_1 should be satisfied as [21]

$$\theta = \frac{\pi}{1+m} \tag{7}$$

where m is the frequency ratio of the dual-band operation.

Consequently, the impedances of z_2 and z_3 can be uniquely determined for some chosen z_1 once the designed frequency ratio is m given.

3.2. Even-mode Analysis

For the even-mode analysis, the two signals along the transmission lines on the top and bottom layers have the same magnitude and phase. Therefore, the TGV can be ignored since it has no effect on the DSPSL. Besides, there is also no current flowing through the input load and the input port can be regarded as an open circuit. In this case, the even-mode equivalent circuit of the proposed power divider can be simplified as shown in Figure 4.

Based on the transmission line theory, the input impedances can be expressed as

$$z_{in1} = \frac{z_1}{j\tan\theta} \tag{8a}$$

$$z_{in2} = z_2\frac{z_{in1} + jz_2\tan\theta}{z_2 + jz_{in1}\tan\theta} \tag{8b}$$

$$z'_{in2} = \frac{z_{in2}}{1+z_{in2}} \tag{8c}$$

$$z_{in3} = z_3\frac{z'_{in2} + jz_3\tan\theta}{z_3 + jz'_{in2}\tan\theta} \tag{8d}$$

The matching condition becomes

$$\left(\frac{1}{\frac{1}{r}+\frac{1}{jz_4\tan\theta}}\right)^* = z_{in3} \tag{9}$$

By separating the real and imaginary parts of Equation (9), the designed parameters of r and z_4 can be achieved as

$$r = \frac{1}{\mathrm{Re}\left(z_{in3}^{-1}\right)} \tag{10a}$$

$$z_4 = \frac{1}{\tan\theta \cdot \mathrm{Im}\left(z_{in3}^{-1}\right)} \tag{10b}$$

3.3. Analysis of Broadband Characteristics

Combining (5)–(8) and (10), we can obtain that the circuit parameters (z_2, z_3, z_4, r) are functions of the frequency ratio m once the value of z_1 is fixed. For some typical values of z_1 (z_1 = 0.75, 0.8, 0.85, 0.9), the corresponding design parameters against the frequency ratio $m = f_1/f_2$ can be calculated by using MATLAB. Numerical results are achieved as shown in Figure 5, which can be used as the design charts.

Assuming that the available impedance values are in the range of $10\,\Omega < Z_i < 150\,\Omega$, the normalized impedance values have the range of $0.2 < z_i < 3$. Therefore, a frequency ratio range covering $1 < m < 1.7$ can be obtained from Figure 5(c). This range can be complementary with that of the power divider presented in [18].

For instance, we employ Figure 5(b), as the design chart, to investigate the broadband characteristic of the proposed power divider. The circuit parameters under different frequency ratios are calculated as shown in Table 1. The transmission and reflection coefficients of the

Table 1. Normalized circuit parameters of the proposed power divider under different frequency ratios.

Frequency Ratio	$m = 1.1$	$m = 1.2$	$m = 1.4$	$m = 1.6$
z_1	0.8	0.8	0.8	0.8
z_2	1.1187	1.0866	0.9947	0.8980
z_3	0.8224	0.8345	0.8782	0.9479
z_4	0.3686	0.4251	0.7119	1.7792
r	0.7012	0.7944	1.2046	2.1459

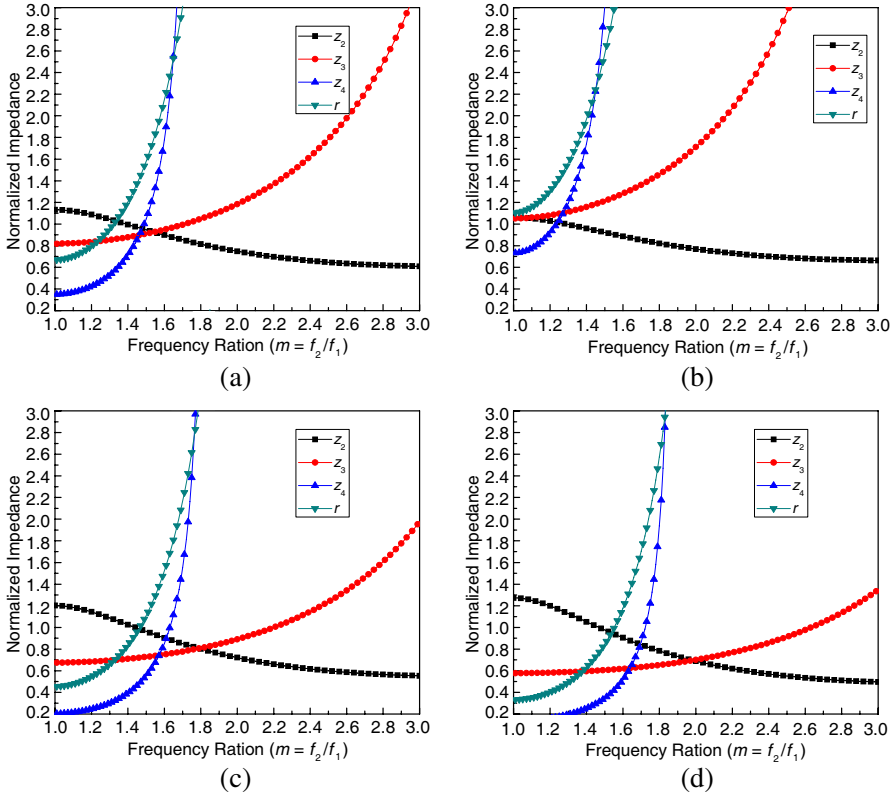


Figure 5. Normalized impedance parameters versus frequency ratio under different z_1. (a) $z_1 = 0.75$. (b) $z_1 = 0.8$. (c) $z_1 = 0.85$. (d) $z_1 = 0.9$.

proposed power divider can be calculated by [18, 21]

$$S_{11} = S_{11}^o \tag{11a}$$

$$S_{21} = S_{31} = \sqrt{\frac{S_{21}^{o2}}{2}} \tag{11b}$$

$$S_{22} = S_{33} = \frac{S_{22}^e + S_{22}^o}{2} \tag{11c}$$

$$S_{32} = \frac{S_{22}^o - S_{22}^e}{2} \tag{11d}$$

Therefore, the corresponding calculated results of the power divider are obtained as shown in Figure 6.

It is obvious that the proposed power divider can operate at

broadband response when proper frequency ratios are adopted. In Figure 6, we can find that the maximum bandwidth with 15 dB return loss/port isolation is achieved when the frequency ratio m is nearly equal to 1.4.

3.4. Analysis of Power Dissipation

The power-handling capabilities of the power dividers mainly depend on how the isolation resistors handle the generated heat. As discussed in [18, 21–24], power dividers with external isolation resistors have high power handling advantage over those with internal isolation resistors.

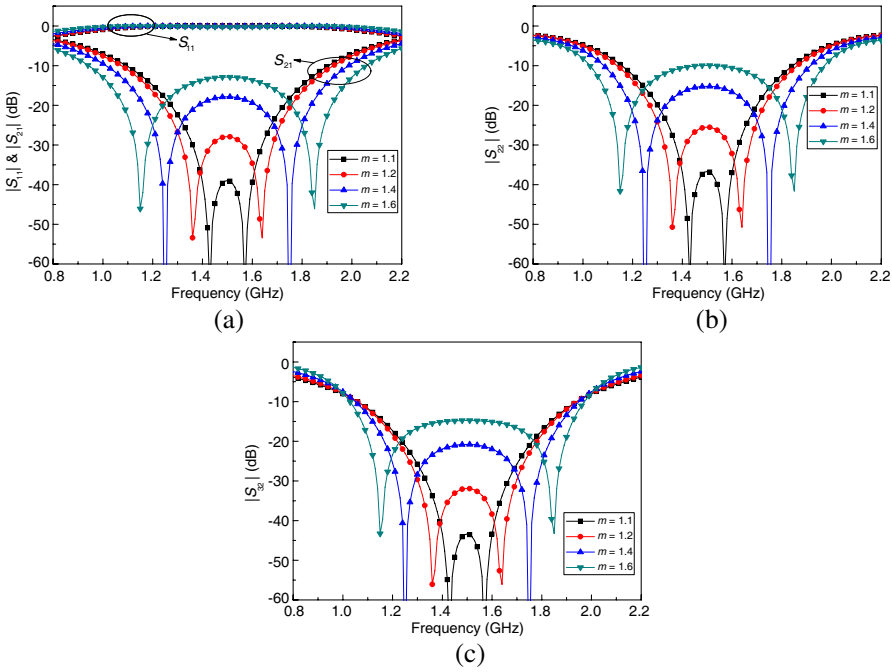


Figure 6. Calculated S-parameters of the proposed power divider under different frequency ratio m.

Table 2. Dimensions of the experimental power divider.

$W_1 = 2.405\,\text{mm}$	$W_2 = 1.732\,\text{mm}$	$W_3 = 2.097\,\text{mm}$
$W_4 = 2.838\,\text{mm}$	$L_1 = 29.8\,\text{mm}$	$L_2 = 30.225\,\text{mm}$
$L_3 = 29.975\,\text{mm}$	$L_4 = 29.6\,\text{mm}$	$R = 60.23\,\Omega$

This is because external isolation resistors can be easily mounted on the cooling systems with good thermal conductivity by adding a transmission line of the same characteristic impedance between the resistor and heat sink.

Besides the advantage of high power handling capability in operation bands, the proposed power divider presents another advantage out of the operation band. As presented in [18, 21–24], the external isolation resistors are generally shorted by transmission lines. Thus, the out-of-band signal power will be partly dissipated on the isolation resistors since the shorting condition is frequency-dependent. In this design, the isolation resistors are shorted by TGV at full-frequency band. Therefore, no power is dissipated on the isolation resistors. This property ensures the proposed power divider has a high power capacity both in and out of the operation bands.

4. SIMULATION AND MEASUREMENT

To validate the previous analysis, an experimental power divider is implemented in this section. The divider is fabricated on two sandwiched Rogers 4350 substrates with the relative dielectric constant

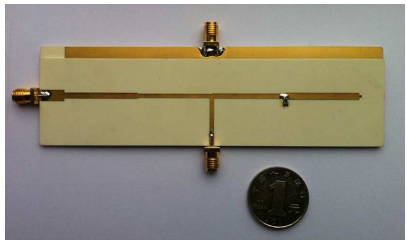
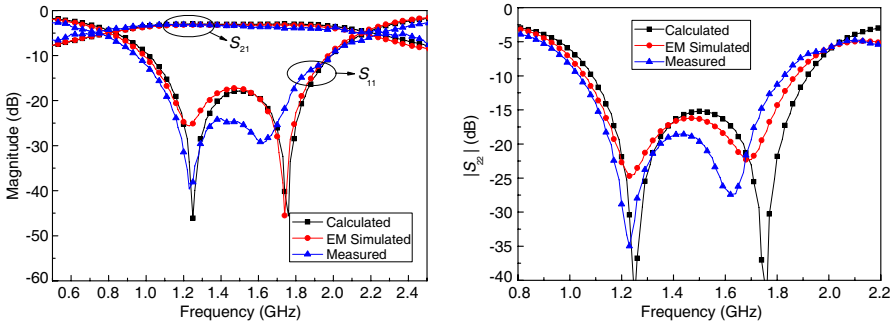


Figure 7. Photograph of the fabricated power divider.



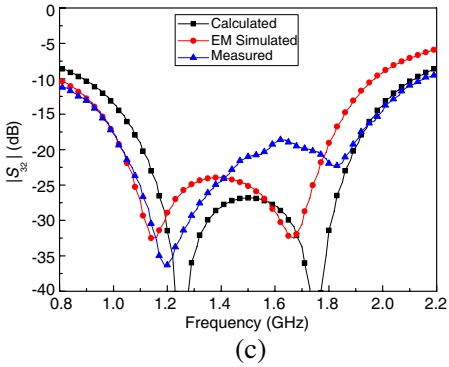


Figure 8. Calculated, EM simulated and measured S-parameters of the proposed power divider. (a) S_{11} & S_{21}. (b) S_{22}. (c) S_{32}.

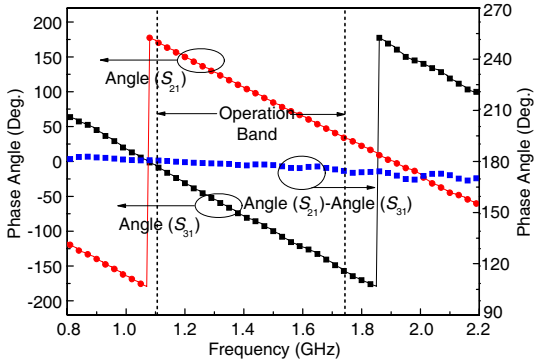


Figure 9. Measured phase response of the proposed power divider.

of 3.48, a thickness of 0.76 mm, and a loss tangent of 0.004.

Typical parameters of the designed power divider are given as follows:

$$Z_0 = 50\,\Omega, \quad f_1 = 1.25\,\text{GHz}, \quad f_2 = 1.75\,\text{GHz}, \quad m = 1.4$$

The design parameters can be obtained from Table 1 and the desired electrical length of the transmission lines is calculated to be 75° based on Equation (7). The physical dimensions of the circuit are achieved as illustrated in Table 2 by using the simulator Ansoft Designer. For the actual implementation, the component of $R = 51\,\Omega$ is adopted in this design.

The photograph of the fabricated power divider is shown in Figure 7. The simulation and measurement are accomplished by

Table 3. Comparison with previous out-of-phase power dividers.

Ref.	Power division	15-dB isolation Bandwidth	Phase Difference
[14]	equal	11.3%	Out-of-Phase
[15]	equal	9.5%	Out-of-Phase
[16]	equal	58.6%	Out-of-Phase
[17]	equal	Dual-band (34.5%/15.5%)	Out-of-Phase
[18]	equal	Dual-band (10.4%/4.2%)	Out-of-Phase
This work	equal	44.3%	Out-of-Phase
Ref.	Isolation resistance	Heat sinking	-
[14]	Internal Isolation Resistance	Not Easy	-
[15]	Internal Isolation Resistance	Not Easy	-
[16]	Internal Isolation Resistance	Not Easy	-
[17]	Internal Isolation Resistance	Not Easy	-
[18]	External Isolation Resistance	Easy	-
This work	External Isolation Resistance	Easy	-

using Ansoft simulator HFSS and Agilent 8358E network analyzer, respectively. Figures 8(a)–(c) compare the calculated, simulated and measured results. The measured return loss (S_{11}, S_{22}) and isolation (S_{32}) are below -15 dB/-18 dB from 1.11 GHz to 1.74 GHz (FBW: 44.3%). The maximum insertion loss during the corresponding band is measured to be 3.7 dB. Furthermore, the measured phase difference between the two output ports is in the range of $180^\circ \pm 6^\circ$ from 1.11 GHz to 1.74 GHz as shown in Figure 9.

The proposed power divider is compared with previous out-of-phase dividers in Table 3. It can be found that the proposed divider has a wider bandwidth. Meanwhile, the isolation resistance is shorted by TGV at full-frequency band. It also means no power is dissipated on the isolation resistors at full-frequency band. This property ensures the proposed power divider has a high power capacity both in and out of the operation bands.

5. CONCLUSION

In this paper, a novel broadband out-of-phase power divider has been presented. The proposed power divider employs the external isolation resistors, which have advantages in heat sinking and largely enhance the power-handling capability. A through ground via (TGV) is investigated. And a novel dual-band impedance matching structure is developed. Besides, analytical equations have been derived and several design charts are given. In Section 4, an experimental power divider, operating a bandwidth of 630 MHz (44.3%) with better than 15 dB return loss and 18 dB port isolation is implemented. The good agreement between simulated and measured results has been achieved, validating the proposed methodology. This power divider will be very useful for the high-power balanced systems and push-pull applications.

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