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A NEW SCHEME FOR THE DESIGN OF BALANCED FREQUENCY TRIPLER WITH SCHOTTKY DIODES

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Abstract—We propose a balanced frequency tripler scheme for millimeter-wave and submillimeter-wave application, in which double-sided suspended stripline is adopted. Two arms of Schottky diodes are mounted on the upper side of the substrate, and the other two arms of diodes are mounted on the lower side. The diodes are DC biased without bypass chip capacitor, which is essential in the common used balanced tripler scheme. Furthermore, the numbers of the diodes are doubled as there are only two arms of diodes in the common balanced tripler scheme, and this will double the power handling capability of the tripler. A W-band frequency tripler is designed according to the proposed scheme with commercial Schottky Varistors. The output power is from 2.9 to 5.7 dBm at the frequencies from 89.7 to 94.8 GHz, with the conversion efficiency from 1.95% $\sim$ 3.7%.

1. INTRODUCTION

Millimeter-wave and submillimeter-wave frequency multipliers [1–6] and mixers [7–14] based on planar Schottky diodes are widely used for atmosphere and space detection. The multipliers are usually driven by an oscillator [15–18] or a phase-locked millimeter-wave source. Up to tens of microwatts power at room temperature was produced at 2.7 THz with cascaded frequency multipliers designed with Schottky Varactors [1]. This power level is sufficient to pump the HEB receiver. Schottky varactors are usually adopted for multipliers design in VDI Inc. and Jet Propulsion Laboratory (JPL), because high output power and high efficiency could be achieved compared with the varistors. The operation frequency, output power and conversion efficiency are keep improving for the evolvement of the design method and multiplier process.

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Balanced frequency multipliers are preferred at millimeterwave and submillimeterwave frequency for simplifying idle circuits and providing higher efficiency. The balanced frequency multipliers, mostly the frequency doublers and frequency triplers, usually have two arms of the diodes [1–6]. The early multipliers usually employ only two diodes, with each diode in one arm limited by the chip process at that time. Nowadays, two or more series arrays of diodes in each arm are used to enhance the power handling capacity, and thus the output power [5]. The series arrays of diodes may be treated as a single diode so far as circuit design is concerned.

State-of-the-art performance has been achieved by balanced frequency doubler with Erickson's scheme [1, 3], in which the diodes are in anti-series connection with the end of each arm bonded to the metal channel. The reverse bias is applied to the diodes from the center line connected to the cathodes of the two arms. As for the frequency triplers, Schottky varactors and heterostructure barrier varactors (HBV) could be used. The performance of the tripler designed with Schottky diode is superior to the one designed with HBVs at millimeter-wave and submillimeter-wave frequency with higher output power and efficiency. In the commonly used balanced tripler scheme [4, 6], all diodes are in series connection, with one arm connected to the metal channel and the other arm RF grounded by a chip capacitor for the bias line as shown in Fig. 1. The on-chip

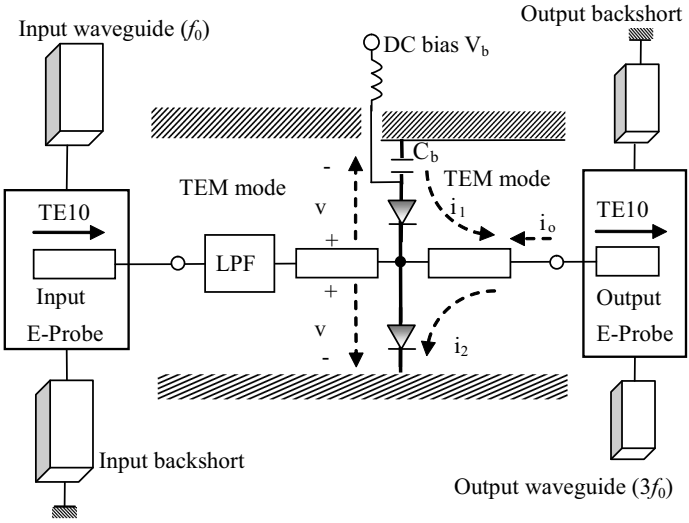

Figure 1. Block diagram of the common balanced tripler with bias circuit.

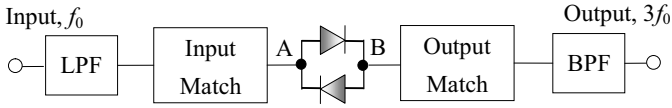

Figure 2. Block diagram of the existing balanced tripler with diodes in anti-parallel connection.

capacitor should provide RF grounding at least at the input frequency, the second harmonic and the third harmonic to avoid affecting the design. Large capacitor is required at lower frequency which would occupy the valuable real estate on the tripler chip, while at higher frequency the capacitor may lead to additional loss. However, state-of-the-art performance is achieved with this balanced tripler scheme thanks to the MMIC-like multiplier chip process and advanced design tools. Besides, external DC bias is usually applied to the diodes to improve the conversion efficiency [19].

There is also another scheme for balanced tripler design with two anti-parallel diodes [20], as shown in Fig. 2. The DC bias could not be applied to the diodes conveniently, because the diodes are in anti-parallel connection.

A new balanced tripler scheme is proposed in this work. First, the numbers of diodes in this scheme is doubled compared with the common schemes, and hence the output power. Second, the DC bias could be applied to the diodes without chip capacitor, which makes the fabrication and assembly of the tirpler much easier.

2. CIRCUITS DESCRIPTION

This work begins with the analysis of the existing design schemes for the balanced frequency tripler, and then the proposed scheme is presented.

2.1. Analysis of the Existing Balanced Tripler Schemes

The block diagram of the common used balanced tripler is illustrated in Fig. 1 [4]. An E-plane probe located in the input waveguide couples the TE10 mode signal at the fundamental frequency to the suspended stripline. The TE10 mode signal is converted into TEM mode supported by the suspended stripline. The low-pass filter (LPF) at input side of the diodes is used to prevent the produced third harmonic from leaking into the input waveguide. The third harmonic produced by the diodes is coupled to the output waveguide by another

E-plane probe. The leaked input signal at output side of the diodes is cut off by the output waveguide, and thus no output filter is needed.

The nonlinearity of Schottky diode could be expressed with power series equation as follow

$$I = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + \ldots \tag{1}$$

where V is the voltage drop from anode to cathode, and I is the current also with the direction from anode to cathode.

The voltage drops across the two diodes in Fig. 1 from the suspended stripline to the channel wall (RF ground) are the same in magnitude and phase, due to the symmetrical TEM mode supported by the suspended stripline. Then the currents flow in the two diodes could be written as

$$i_1 = a_0 - a_1 v + a_2 v^2 - a_3 v^3 + \ldots \tag{2}$$

$$i_2 = a_0 + a_1 v + a_2 v^2 + a_3 v^3 + \ldots \tag{3}$$

where v is the voltage drop from the suspended stripline to ground.

Then,

$$i_o = i_2 - i_1 = 2a_1 v + 2a_3 v^3 + \ldots \tag{4}$$

where i_o is the total output current with the direction from output waveguide to the diodes (also could be from the diodes to the output waveguide with 180 degree out of phase).

Equation (4) implies that only odd harmonics present at the output of the diodes. Among them, the fundamental frequency is cut off by the output waveguide, the higher order harmonics are small enough to be ignored. Then the output signal mainly contains the third harmonic.

This type of balanced triper needs a chip capacitor to provide RF grounding for diodes and DC block for bias line. The capacitor is usually designed on chip in the MMIC-like multiplier chip. This chip capacitor could introduce additional loss when signal passes through it, and the phase balance could also be slightly changed by this capacitor. This scheme is suit for MMIC-like process, because the chip capacitor could be integrated in the circuit precisely. However, when it comes to hybrid integrated frequency multiplier, especially at frequencies about 200 GHz and below, the commercial chip capacitor is the only option. The capacitances of these capacitors are limited to several values and the size of the chip is too large to be mounted on the multiplier circuit without jeopardizing the performance.

There is another scheme could be used to design the balanced tripler [20], as shown in Fig. 2. Anti-parallel diodes are placed in series with the transmission line. The input LPF passes the input fundamental signal, and rejects the higher order harmonics. The

output band-pass filter (BPF) only passes the third harmonic, and rejects the other harmonics. The input LPF combining with the input matching circuit will present a short circuit at f_0 at point A, and the output BPF combining with the output matching circuit will present a short circuit at $3f_0$ at point B. This manipulation makes the circuit in Fig. 2 equivalent to the circuit in Fig. 1, and then Equations (1) to (4) also apply in this circuit.

The disadvantage of this scheme is that the DC bias could not be applied to the diodes conveniently, because the diodes are in anti-parallel connection.

2.2. The Proposed Balanced Frequency Tripler Scheme

The proposed balanced tripler adopts single substrate double-sided suspended stripline (DSS), which is famous for its low loss application [21–23]. There are two basic modes supported by DSS, which are the odd mode and the even mode. The two-dimensional electric field distribution of the even mode is shown in Fig. 3(a), and only the even mode could be excited by the E-plane DSS probe when coupling energy from waveguide [24]. The simulation of the waveguide-to-DSS transition will be shown in Part 3. The proposed balanced tripler is illustrated in Fig. 3(b). The input and output put waveguide, and the input LPF are the same as in Fig. 1, and thus not shown in Fig. 3(b). The proposed balanced tripler has four arms, with two arms on the upper side of the substrate and the other two on the lower side. Each arm could consist of one diode or even more diodes in series. The series arrays of diodes may be treated as a single diode so far as circuit design is concerned.

As shown in Fig. 3(b), the two diodes on the upper side are in anti-series connection with the cathodes connected to the upper line, while the two diodes on the lower side are also in anti-series connection but with the anodes connected to the lower line. The substrate is mounted on the center plane of a metal channel to guarantee the symmetry. The red solid lines represent of upper stripline and the field distribution of it, while the blue dotted lines represent of lower stripline and the field distribution of it. The electronic field distribution is symmetrical about the center two lines as shown in Fig. 3(a), which leads to the conclusion that the excited voltages at point A and point B in Fig. 3(b) are totally the same in magnitude and phase. Then the currents flowing through the four diodes are

$$i_1 = a_0 - a_1 v + a_2 v^2 - a_3 v^3 + \ldots \tag{5}$$

$$i_2 = a_0 - a_1 v + a_2 v^2 - a_3 v^3 + \ldots \tag{6}$$

$$i_3 = a_0 + a_1 v + a_2 v^2 + a_3 v^3 + \ldots \tag{7}$$

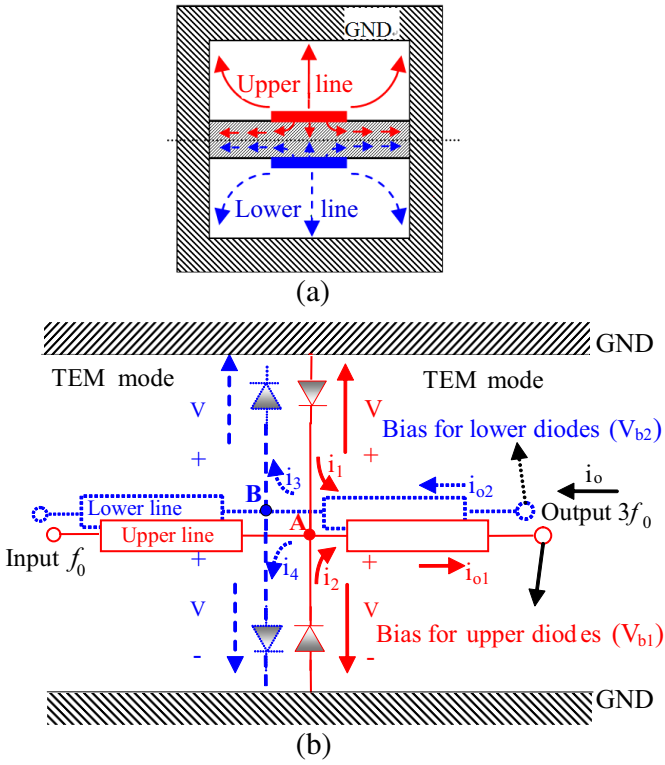

Figure 3. (a) Cross view of the electric field of DSS. (b) Block diagram of the proposed balanced tripler.

$$i_4 = a_0 + a_1 v + a_2 v^2 + a_3 v^3 + \ldots \tag{8}$$

Then the current flow on the upper line and the lower line are

$$i_{o1} = i_2 + i_1 = 2a_0 - 2a_1 v + 2a_2 v^2 - 2a_3 v^3 + \ldots \tag{9}$$

$$i_{o2} = i_3 + i_4 = 2a_0 + 2a_1 v + 2a_2 v^2 + 2a_3 v^3 + \ldots \tag{10}$$

Because the currents of the top line and the bottom line are in the opposite direction, the total output current of the tripler is

$$i_o = i_{o2} - i_{o1} = 2a_1 v + 2a_3 v^3 + \ldots \tag{11}$$

As can be seen from Equation (11), the output current only contains odd harmonics, with even harmonics suppressed by the balance configuration.

2.3. Construction of the Proposed Balanced Tripler

A three dimensional (3D) view of this balanced tripler is illustrated in Fig. 4. The tripler module is split into two blocks along the center of the

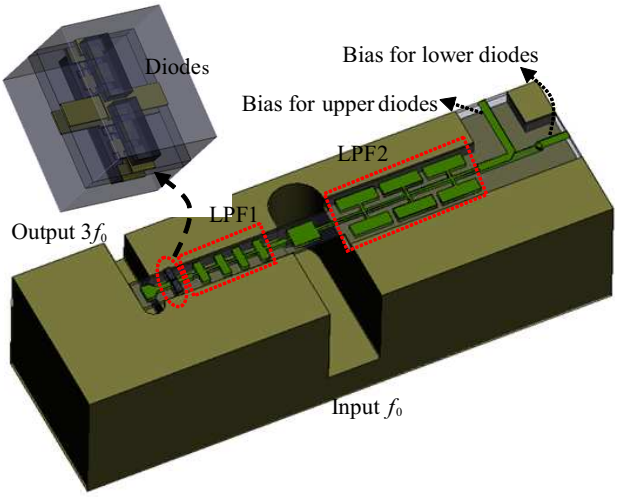

Figure 4. 3D model of the proposed balanced tripler.

E plane, namely the lower block and the upper block. The substrate is mounted on the lower block with silver epoxy. The substrate is double-sided suspended stripline with the same circuits printed on both sides, including the input E-probe, the input LPF (LPF1) for suppressing the third harmonic and impedance matching, the Schottky diodes, the output E-probe and the hammer-head LPF (LPF2) for bias line to prevent the input signal from leaking to the bias terminal [25].

The proposed balanced tripler scheme has the following potential advantages compared with the common used ones: 1) On-chip or discrete capacitor for DC bias is avoided, so the fabrication and assembly of the circuits are simplified; 2) The numbers of the diodes are doubled, and so does the output power; 3) The diodes are strictly balanced, so the multiplying efficiency is enhanced; 4) Better RF grounding is fulfilled, for all the four ends of the diode arms are connected to the metal channel, which also results in better heat dissipation.

3. SIMULATIONS

The simulations of the proposed balanced tripler are divided into several steps. First, the input waveguide-to-DSS transition with hammer-head LPF (LPF2) for bias, the output DSS-to-waveguide transition and the input matching LPF (LPF1) are simulated and optimized. Second, the optimum input and output embedding

impedances of the tripler are obtained by HFSS and ADS co-simulation. Third, the impedance matching circuits are designed according to the embedding impedances. Fourth, the whole tripler model was simulated in HFSS, and then the S parameters are exported into ADS for the performance simulation, including the output power, the conversion efficiency, and so on. Based on the simulated results, some parameters of the circuit are tuned to achieve the optimum results. A W-band balanced tripler at frequencies from 90 to 96 GHz is designed in this work to verify the feasibility of the proposed scheme.

3.1. Simulation of the Input Waveguide-to-DSS Transition with Hammer-head LPF

The DC biases are applied to the diodes through the input E-plane probe, so the input waveguide-to-DSS transition and the hammer-head LPF are simulated together as one model in HFSS as shown in Fig. 5(a). The input waveguide is standard WR-28 waveguide with dimensions $a = 7.11$ mm and $b = 3.56$ mm. The standard waveguide is then transitioned to a reduced height rectangular waveguide to achieve broadband waveguide-to-DSS transition. The DSS hammer-head LPF allows the DC bias pass through it, and prevents the input signal from leaking to the DC bias terminal. This hammer-head filter is designed to have a rejection of more than 40 dB at the input frequencies from 30 to 32 GHz.

As mentioned before, the DSS has two operation modes, which are

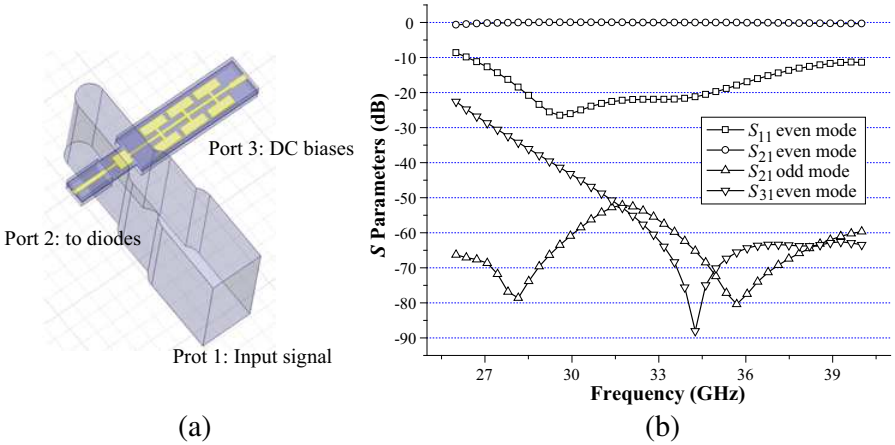

Figure 5. WG-to-DSS transition with hammer-head LPF. (a) HFSS model. (b) Simulated results.

even mode and odd mode. Only the even mode could be excited by the waveguide-to-DSS transition. The simulation of waveguide-to-DSS transition with two modes at port 2 is carried out, with the results shown in Fig. 5(b). It is found that the input waveguide TE10 mode signal could be converted into DSS even mode with very low loss, while the DSS odd mode is an evanescent mode in the waveguide-to-DSS transition and attenuated tremendously along the DSS line.

3.2. Simulation of the Input LPF

Five steps of stepped impedance [26–28] LPF is designed as shown in Fig. 6. The LPF mainly has two functions. First, it passes the input fundamental signal to the diodes, and prevents the produced third harmonic by the diodes from leaking to the input waveguide. Second, combining with a short length of transmission line right before the diodes, it will function as input matching circuit. The cut-off frequency of the LPF is about 40 GHz, and the insertion loss of the LPF at 90 GHz is about 20 dB, which is enough for the tripler design.

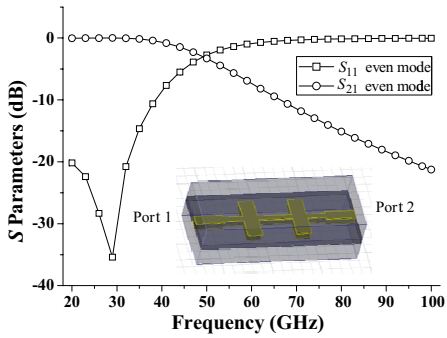

Figure 6. HFSS model and simulated results of the input LPF.

3.3. Simulation of the Diodes plus the Output DSS-to-waveguide Transition

The commercial Schottky varistor chip DBES105a, fabricated by UMS, is used in this work. Although the efficiency of tripler designed by varistors is obviously lower than the one designed by varactors, DBES105a is still adopted for low cost design, for the main purpose of this work is to verify the balanced tripler scheme.

Actually, DBES105a chip is formed by two diodes in series Then each arm of the tripler has two diodes in series. The parametric effect of the diode structure is also taken into account by including the

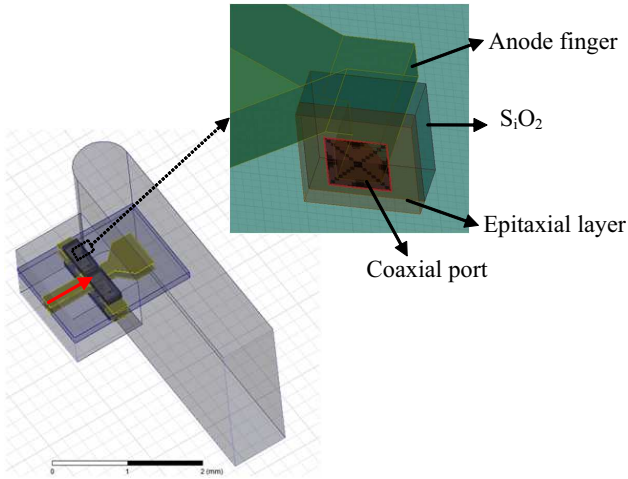

Figure 7. HFSS model of the diodes and the output DSS-to-waveguide transition.

diode in the tripler model in HFSS as shown in Fig. 7. The model of DBES105a is similar to the one described in [29]. The buffer layer is treated as perfect electric conductor (PEC). Coaxial port is placed at each Schottky contact [30], as illustrated in the dotted box in Fig. 7. The anode passed through the SiO_2 layer and the epitaxial layer, and contacts the buffer layer. The coaxial port is just located at the contact. Thus the model in Fig. 7 has ten ports, which are the output waveguide port, the input even mode DSS port, and total eight coaxial ports for eight diodes. This way the diode could be de-embedded in the HFSS model. The input DSS port is further de-embedded to the reference plane right before the diode, which is necessary for the input matching next step. The output mach is realized by tuning the width and length of the DSS line after the diode and the dimensions of the E-plane probe. The ten-port S parameters are then exported to ADS to optimize the input impedance to achieve the minimum input return loss, which means that the tripler could couple the maximum power from the input. As mentioned before, the input impedance matching is achieved by the input LPF and a short length of transmission. The width and length of the transmission line are determined by the optimized input impedance according to the ADS simulation.

3.4. Simulation of the Balanced Tripler in One Model

Once the input matching circuit and the output matching circuit have been designed, the model of the tripler, including the input waveguide-

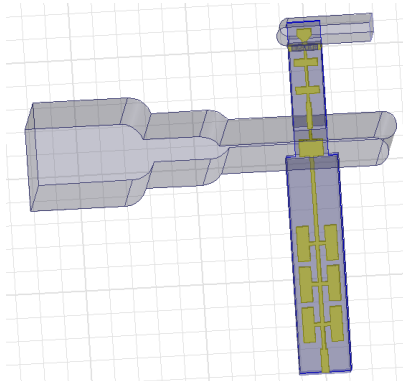

Figure 8. HFSS model of the proposed balanced tripler.

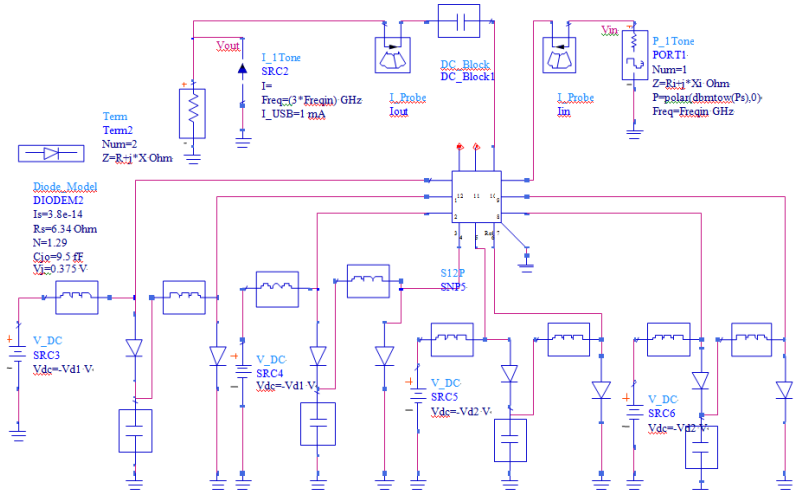

Figure 9. The schematic of the balanced tripler in ADS.

to-DSS transition with hammer-head filter, the input LPF, the total eight diodes and the output DSS-to-waveguide transition, is then built in HFSS as shown in Fig. 8.

This model contains eleven ports, which are the input waveguide port, the output waveguide port, the bias DSS port, and eight coaxial ports for eight diodes (four chips of DBES105a). The simulated eleven-port S parameter is the exported to ADS to verify the performance of the balanced tripler. The ADS simulation schematic is shown in Fig. 9.

The simulated results are illustrated in Fig. 10. The input return

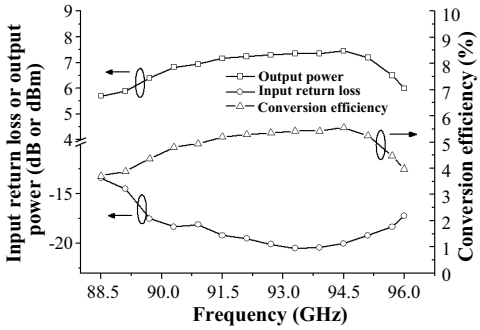

Figure 10. Simulated results of the balanced tripler.

loss corresponding to the output frequencies from 90 GHz to 96 GHz is lower than −15 dB, which means most of the input power has been coupled to the diodes. The predicted peak output power at 94.5 GHz is 7.4 dBm with 5.5% conversion efficiency when the drive power is 20 dBm.

4. ASSEMBLY AND TEST BENCH SETUP

Substrate RT/D 5880 from Rogers is adopted here for the tripler circuit. The thickness of the substrate is 0.254 mm. The substrate is electrodeposited with 17 μm copper foil, which is further clad with 2 μm gold. Copper is also used to fabricate the module, which is then plated with gold before the assembly.

The assembly begins with the diode mounting. First, two chips of DBES105a are mounted on the lower side of the substrate with silver epoxy. Second, the other two chips are mounted on the upper side of the substrate. Third, the substrate is mounted on the lower block of the module with silver epoxy, too. Last, the upper block and the lower

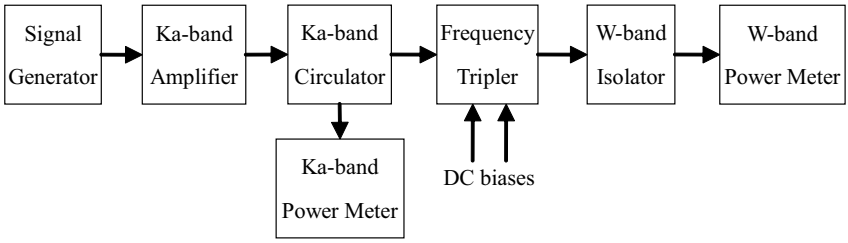

Figure 11. Test bench setup for the proposed frequency tripler.

block is jointed together with screws.

The test bench setup is illustrated in Fig. 11.

The circulator before the frequency tripler under test has two functions. First, the interaction between the Ka-band amplifier and the highly nonlinear load of the tripler can be severe. The circulator provides essential isolation between them, in case the amplifier has poor output return loss. Second, the third port of the circulator is used to test the input return loss of the frequency tripler. The network analyzer is not used here for the input return loss measurement because its output power is not high enough to drive the frequency tripler. The isolator at the output is also added to provide isolation between the tripler and the power meter.

There are two bias terminals for the frequency tripler. The DC bias for the upper diodes is positive (V_b), which sources current. While the DC bias for the lower diodes is negative ($-V_b$), which sinks current. The two biases are predicted to be in the same magnitude to keep the diodes on both sides of the substrate in balance.

5. TEST RESULTS AND DISCUSSION

The measured results are shown in Fig. 12. The measured frequency ranges from 29.9 GHz to 31.6 GHz, due to the limited frequency range of the drive amplifier. When the drive power is 20 dBm, the measured output power is from 2.9 to 5.7 dBm, and conversion efficiency from 1.95% to 3.7%, as shown in Fig. 12(a). The measured output power and conversion efficiency are lower than expected. After re-checking

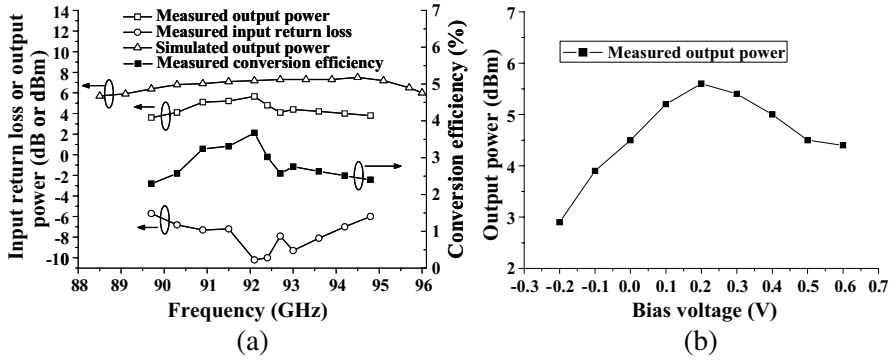

Figure 12. Measured results of the proposed frequency tripler. (a) Output power and conversion efficiency. (b) Output power vs. bias voltage.

the tripler module, the main reason should be the deformation of the soft substrate RT/D 5880 during the high temperature curing of the silver epoxy. As shown in Fig. 13, the center of the substrate along the channel is a little concaved, which could break the balance of the tripler. This also deteriorates the measured input return loss as shown in Fig. 12(a). There are also other reasons could contribute to the discrepancies between the simulated and measured results, such as the assembly error.

The output power versus bias voltage is also measured as in Fig. 12(b). The x-axis of the figure is corresponding to the bias voltage

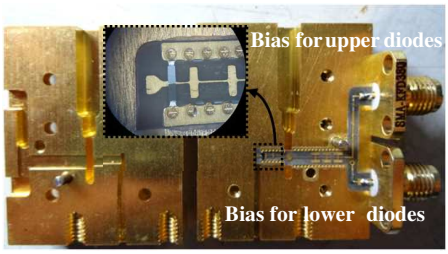

Figure 13. Photo of the proposed frequency tripler.

Table 1. Summary of the previous balanced frequency triplers and this work.

References	[29]	[2]	[31]	[6]	This work
Devices	DBES105a Varistor	DBES105a Varistor	Not known	JPL Varactor	DBES105a Varistor
Output frequency (GHz)	114 ∼ 135	75 ∼ 110	75 ∼ 110	260 ∼ 340	89.7 ∼ 94.8
Input Power (dBm)	19.8	27	20	20	20
Output Power (dBm)	−10 ∼ 5.4	5.5 ∼ 11	−1 ∼ 2.6	1.8 ∼ 8.8	2.9 ∼ 5.7
Conversion Efficiency (%)	3.5	3 (typical)	0.8 ∼ 1.8	1.5 ∼ 7.5	1.95 ∼ 3.7
Year	2010	2013	2007	2006	2013

for the upper diodes, and the bias voltage for the lower diodes is simply the negative value of it.

During the measurement, the input power is gradually increased from 20 dBm to 24 dBm, and the observed output power is also increased linearly. The peak output power is 9.5 dBm when the drive power is 24 dBm. The performance for higher input power is not covered in this measurement for the limited output power of the Ka-band amplifier.

The comparison between the performance of the frequency tripler of this work and others are listed in Table 1. The performance of the tripler designed in this work is comparable with the ones also designed with varistors, but apparently inferior to the tripler designed by varactor, considering the output frequency of the varactor tripler is about three times that of the varistor triplers.

6. CONCLUSIONS

A new scheme for balanced tripler is proposed in this work. This scheme features doubled number of diodes, and no chip capacitor is required to bias the diodes. The doubled number of diodes means more output power could be produced. Biasing the diodes without chip capacitor guarantees the nearly ideal balance of the diodes, avoids the loss introduced by the capacitor, and also makes the fabrication and assembly easier. The measured results agree with the simulated results fairly, and prove the proposed scheme valid. The deformation of the soft substrate during assembly should be the main reason why the measured output power and efficiency are lower than the simulated ones. This could be solved by using hard substrate, such as Al_2O_3 or quartz substrate.

The proposed scheme could potentially substitute the existing schemes, especially at the frequencies around 200 GHz and below.

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