

## DUAL FED DISTRIBUTED AMPLIFIER WITH CONTROLLED TERMINATION ADJUSTMENT

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**Abstract**—A new circuit and technique to extend the bandwidth of the Dual Fed Distributed Amplifier (DFDA) while preserving the improvement on efficiency performance in comparison to conventional distributed amplifiers (DAs) is presented. The theoretical analysis is described in detail, and a test vehicle is realized to demonstrate the effectiveness of the proposed method. Output power of  $\sim 29$  dBm, gain of 10 dB, covering a bandwidth from 100 to 800 MHz, with a PAE of 20–45% is experimentally demonstrated. The results are compared with measured results of the conventional DA, demonstrating a significant improvement in bandwidth and efficiency.

### 1. INTRODUCTION

Traditionally, two-way public safety radios are operated in a single band. For example, in USA, rural police is operating at VHF band, different from the one used by urban police. Hence in an emergency situation, both agencies cannot directly communicate with each other. This is therefore a strong market drive for a single radio capable to operate in wide frequency range, the so-called SDR (Software Defined Radio) frequency band [1, 2].

The Distributed Amplifier (DA) topology is an attractive candidate for SDR applications [1–3]. In conventional DAs however, the current combining efficiency at the drain line is typically poor, due to current splitting on the drain line into two branches, forming two

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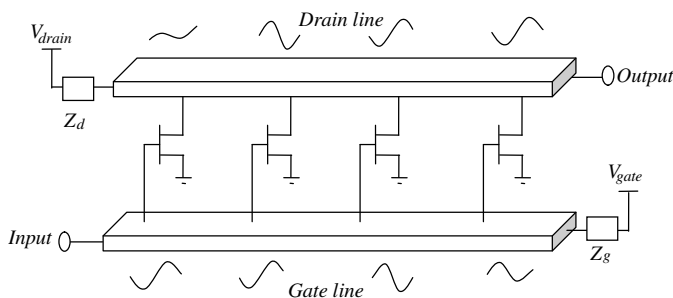
waves traveling one towards the load and the other toward the dummy terminations. The tapered drain line DA [4, 5] eliminates the drain line reverse wave adopting a suitable tapering of the drain line impedance. The dual fed distributed amplifier (DFDA) topology, proposed in [6], allows efficient power combining at the load termination. Similar technique, by adding Lange couplers or Wilkinson combiners at the input and output of the DA to improve output power, gain and power-added efficiency (PAE), was demonstrated by [7, 8]. A compact DFDA with single-ended termination was shown in [9] demonstrating a practical realization with meandered artificial transmission lines loaded with short-circuit stubs. Other works related to DFDA approach were demonstrated by [10, 11].

In this paper, a further improvement of the DFDA topology with a termination adjustment network is proposed, demonstrating a remarkable bandwidth-efficiency improvement over the conventional DA. The concept is experimentally validated for the driver amplifier for SDR application, to provide an output power of  $\sim 29$  dBm over the frequency bandwidth from 100 to 800 MHz. The simple implementation permits low cost and smaller size, suitable for a market-oriented product.

## 2. PRINCIPLE OPERATION AND EFFICIENCY ANALYSIS OF DISTRIBUTED AMPLIFIERS

The gain and bandwidth of an amplifier stage is limited by intrinsic parameters of the active device employed. It is well known that expanding the bandwidth determines a gain reduction [13]. As the gain is made close to unity, it becomes inefficient to cascade amplifier stages. On the other hand, combining the outputs from a number of active devices in parallel increases the output power without improvement of the gain-bandwidth product [12]. The basis of the distributed amplification is to superimpose constructively the output currents from a number of devices, refer to Fig. 1, while avoiding the sum of the shunt capacitances [12].

The concept of distributed amplification is based on combining the input and output capacitances of the active device with inductors in such a way that two artificial transmission lines are obtained. The input and output capacitances of each device become the capacitance per unit section for these lines that are coupled by the  $g_m$  of the active device. As a result, it is possible to obtain amplification over a wider bandwidth than a conventional amplifiers [13]. Designers have concentrated the efforts mainly on increasing the gain-bandwidth product and the gain flatness, as well as on output power capabilities.



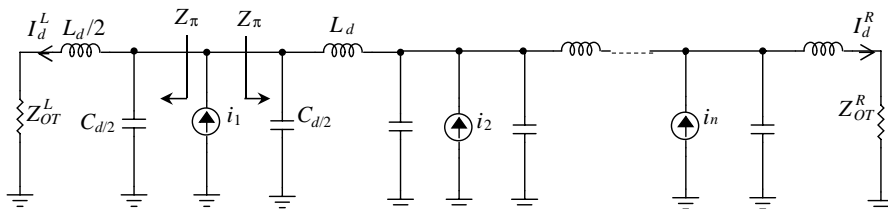
**Figure 1.** The distributed amplification concept.

In DA, the equivalent transmission lines are often analyzed as a cascade of two ports. For the amplifiers employing transmission lines, the voltage developed along the output line tends to increase as the cut-off frequency is approached if the magnitudes of the current injected by the active devices along the line remain constant [13]. This is the result of the factor of  $(1 - \omega^2/\omega_c^2)^{-1/2}$  in the mid-shunt image impedance  $Z_{O\pi}$  [13].

Conventional DAs have never demonstrated a PAE of more than 20% [7, 8]. This is primarily due to the current splitting on the drain line into two branches forming waves traveling towards the output load termination, and waves traveling towards the dummy termination. Each transistor injects a current of  $g_m v_{gs}$ , where  $g_m$  and  $v_{gs}$  are transconductance and gate-source voltage, respectively. Since the drain of each transistor is loaded by the same impedance  $Z_\pi$  in both directions, hence half of this current travels to the left and half to the right [12], as illustrated in Fig. 2.  $Z_\pi$  is given by:

$$Z_\pi = \sqrt{\frac{L_d \left(1 - \frac{f^2}{f_c^2}\right)^{-1}}{4C_d}} \tag{1}$$

where  $L_d$  and  $C_d$  are inductive and capacitive elements to form artificial transmission line along the drain line, respectively and  $f_c$  is the cut-off frequency of the transmission line.



**Figure 2.** Impedance  $Z_\pi$  seen by each transistor in both directions.

The currents flowing to the load termination,  $I_d^R$  and dummy termination,  $I_d^L$  can be deduced from the network shown in Fig. 2. Each low-pass network,  $L_d$ - $C_d$  has an image propagation factor,  $\theta_d$  along the drain line. Applying the superposition theorem to the network shown in Fig. 2, the current towards drain termination [12],  $I_d^R$  can be derived as

$$\begin{aligned} I_d^R &= \frac{1}{2} [I_1 e^{-(n-1/2)\theta_d} + I_2 e^{-(n-3/2)\theta_d} + I_3 e^{-(n-5/2)\theta_d} + \dots + I_n e^{-(n-(n+2)/2)\theta_d}] \\ &= \frac{1}{2} e^{-\frac{\theta_d}{2}} \sum_{K=1}^n I_K e^{-\theta_d(n-K)}, \end{aligned} \quad (2)$$

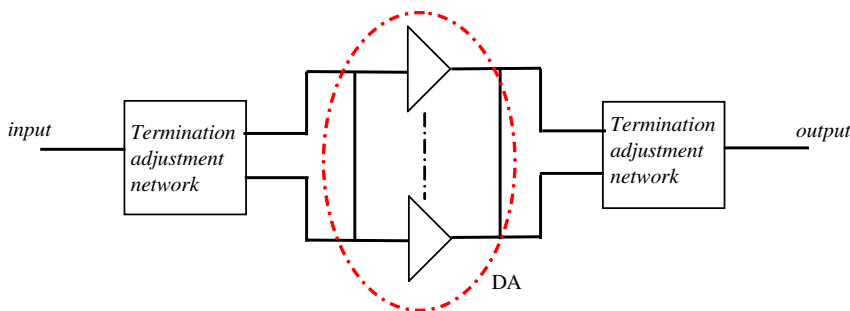
where  $n$  is number of transistor sections. The network is assumed to be lossless. Similarly, applying the superposition theorem, the current towards dummy termination  $I_d^L$  [12] is derived as

$$\begin{aligned} I_d^L &= \frac{1}{2} [I_1 e^{-(1/2)\theta_d} + I_2 e^{-\theta_d} + I_3 e^{-2\theta_d} + \dots + I_n e^{-(n-1)\theta_d}] \\ &= \frac{1}{2} e^{-\frac{\theta_d}{2}} \sum_{K=1}^n I_K e^{-\theta_d(K-1)}. \end{aligned} \quad (3)$$

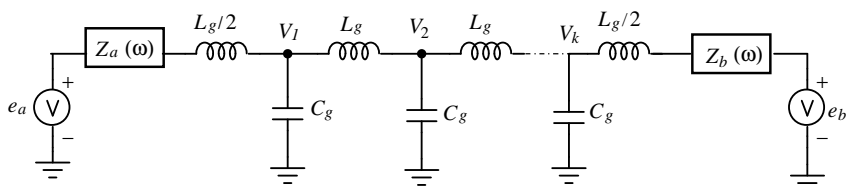
### 3. ANALYSIS OF DUAL FED DA WITH TERMINATION ADJUSTMENT

The conventional DA consists of an input port on one side of the gate line and an output port on the opposite side of the drain line. In basic DFDA, the unused gate and drain ports, known as dummy termination, will be terminated with appropriate characteristic impedance. The two ports of the gate line are simultaneously fed and both end of the drain line are assumed as output ports. In this work, the termination of the DFDA is modified as shown in Fig. 3, to obtain a remarkable bandwidth extension with an optimum impedance termination selection at both end ports of the gate line. In similar manner, by adjusting the termination impedance at the drain line, the efficiency is maximized over the entire bandwidth.

If in linear conditions super-position is applied [14], it follows that the output due to forward gain from the left to right gate input signal appears at the right hand drain port and similarly the output due to forward gain from the right to the left gate input signal appears at the left hand gain port [15]. These two output signals can be combined to give the total output power. The reverse gain must also be taken into account, and, if the phase of the splitter/combiner is appropriate, the currents due to reverse gain flow out of the same output port and add vectorially to the forward gain [16].



**Figure 3.** Schematic diagram of DFDA with termination adjustment.



**Figure 4.** Termination adjustment at both ends of the DA gate line.

In [8] it is clearly detailed that if both terminations end ports are terminated with an appropriate impedance value, a gain improvement is achieved by maintaining the same device structure.

This work is focused on the improvement of the bandwidth-efficiency response over conventional DAs. Beyer et al. analytically showed that the gate line attenuation  $\alpha_g$  is more sensitive to the frequency response than the drain line attenuation  $\alpha_d$  [12]. Following such consideration, the concept proposed in this work provides the optimum impedance at both ends of DA gate line to extend bandwidth response.

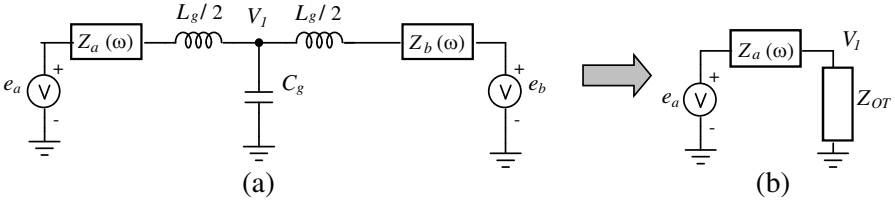
With reference to Fig. 4, the impedances  $Z_a(\omega) = R_a(\omega) + jX_a(\omega)$  and  $Z_b(\omega) = R_b(\omega) + jX_b(\omega)$  can be defined as the equivalent Thevenin impedances for the driving sources  $e_a$  and  $e_b$  respectively, at both ends of the DA gate line. The scheme in Fig. 4 can be simplified (with a single section only) as shown in Fig. 5(a).

A further simplification, neglecting  $e_b$ , is shown in Fig. 5(b). The voltage  $V_1$  can be thus expressed as:

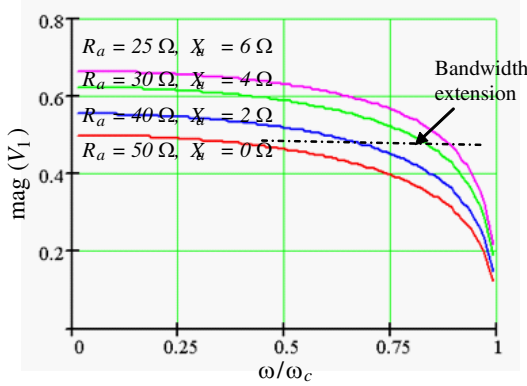
$$V_1 = \frac{e_a}{\frac{R_a(\omega) + jX_a(\omega)}{Z_{OT}(\omega/\omega_c)} + 1}, \tag{4}$$

where  $Z_{OT}(\omega/\omega_c)$  represents  $T$ -section constant- $k$  LC network, terminated with matched characteristic impedance [13].

To obtain the behavior of  $V_1$  as a function of the frequency, the expression (4) has to be further investigated. Assuming  $e_a = 1\angle 0^\circ$  V,



**Figure 5.** Simplifications of the scheme in Fig. 3 with the exclusion of  $e_b$ .



**Figure 6.** Voltage  $V_1(\omega)$  over normalized frequency ( $\omega/\omega_c$ ) with selection of  $R_a(\omega) + jX_a(\omega)$ .

an optimum  $X_a(\omega)$  can be numerically determined for various  $R_a(\omega)$  values. The  $V_1$  magnitude is plotted in Fig. 6. As it can be noticed, the magnitude can be increased over a wide frequency range by properly selecting  $R_a(\omega) + jX_a(\omega)$ . For instance, selecting  $Z_a = 30 + j4\Omega$ ,  $V_1$  around 0.5 V is achieved for wider bandwidth ( $\omega/\omega_c \sim 0.85$ ) as compared to  $Z_a = 50\Omega$ . The superposition theorem is now applied to Fig. 4(a), considering also  $e_b$  (and  $Z_b$ ); the total resulting voltage  $V_1(\omega)$  is expressed by:

$$V_1 = \frac{Z_t^L e_a}{Z_t^L + j\omega L_g/2 + Z_a(\omega)} + \frac{Z_t^L e_b}{Z_t^R + j\omega L_g/2 + Z_b(\omega)} \quad (5)$$

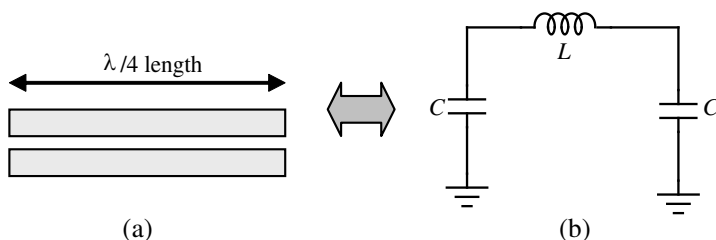
where

$$Z_t^L = \frac{j\omega L_g/2 + Z_b(\omega)}{1 - \omega^2/4\omega_c^2 + j\omega C_g Z_b(\omega)}, \quad \text{and} \quad Z_t^R = \frac{j\omega L_g/2 + Z_a(\omega)}{1 - \omega^2/4\omega_c^2 + j\omega C_g Z_a(\omega)}.$$

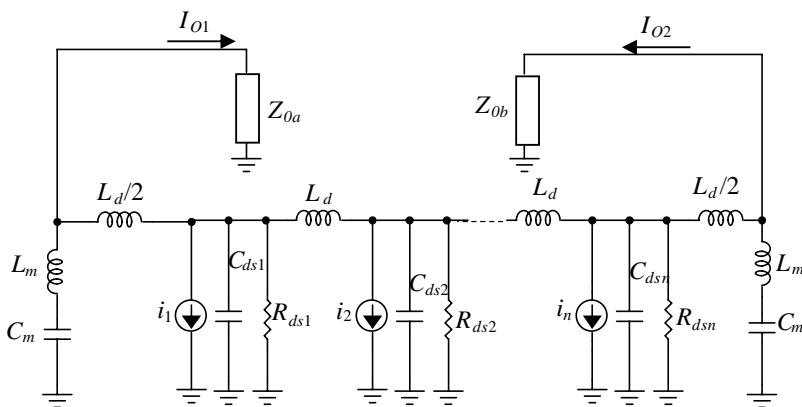
For an equal injection at both ends of the gate line,  $e_a = e_b$ , the voltage response  $V_1(\omega)$  from (5) can be widened over a wide frequency range in a similar way by terminating the gate line with an optimum  $Z_a(\omega)$  and  $Z_b(\omega)$ .

In this contribution, the termination adjustment network is realized by Wilkinson splitters. The termination adjustment impedance  $Z_a(\omega)$  and  $Z_b(\omega)$  are accomplished by tuning the resonance frequency  $f_o$  of Wilkinson splitter at gate and drain line networks. The detailed explanation of the adjustment of the termination networks will be given in the following section.

The splitter offers broad bandwidth and equal phase characteristics at each of its output ports [17]. The splitter employs  $\lambda/4$  transmission line sections at the design center frequency, which can have unrealistic dimensions at low RF frequencies, where the wavelength is large [18]. Due to size constraints, lumped-element equivalent network replacing the  $\lambda/4$  transmission line would be preferable, as shown in Fig. 7(a). This network is equivalent to the original at the center frequency  $f_o$  only. Consequently, the expected performance (insertion loss, return loss, isolation, etc.) should be similar to that exhibited by the distributed-form divider for a narrow bandwidth centered at  $f_o$ , wide enough for most applications. The “ $\pi$ ” LC equivalent networks



**Figure 7.** Lumped element  $\pi$ -section by using (a) transmission line, (b) lumped element representation.



**Figure 8.** Theoretical circuit analysis of the drain line of the modified DFDA.

exhibit a low-pass behavior (refer to Fig. 7(b)) rejecting high frequencies, while the response of the classical splitter repeats at odd multiples of the center frequency ( $3f_o$  and  $5f_o$ , mainly) [18].

A microstrip Wilkinson splitter or combiner at 100 MHz has an area of about  $60\text{ cm}^2$  on FR-4 PCB, while the presented lumped-element version occupies an area of less than  $2\text{ cm}^2$ . Lumped-element circuits with higher  $Q$  than distributed circuits have the advantage of smaller size, low cost, and wide bandwidth characteristics [16]. The values of the lumped elements are given by the following expressions:

$$C = \frac{1}{2\pi f_o Z_o}, \quad (6)$$

$$L = \frac{Z_o}{2\pi f_o}, \quad (7)$$

where  $Z_o$  and  $f_o$  are the characteristic impedance and the resonance frequency of the lumped elements, respectively as shown in Fig. 7(b).

The analysis of the output drain line of the modified DFDA shown in Fig. 8 is described in the following. The forward currents ( $I_{o1}$  and  $I_{o2}$ ) summing in phase at the corresponding output ports are considered [15]. For simplicity, the circuit is analyzed at low frequencies. By assuming that the input voltage of each gate line is  $V_i/\sqrt{2}$ , the output current towards each output port is expressed as

$$I_{oi} = \frac{nR_{ds}}{(nZ_{0o} + 2R_{ds})} g_m \frac{V_i}{\sqrt{2}}, \quad i = 1, 2, \dots, n, \quad (8)$$

where  $n$  is the number of FETs,  $R_{ds}$  is the drain-source resistance of the active devices,  $g_m$  is the transconductance and  $Z_{0o}$  is the load impedance of the output ports ( $Z_{0a}$  and  $Z_{0b}$ ). The total output power,  $P_{out}$  computed as the sum of the contributions from  $I_{o1}$  and  $I_{o2}$ , is given by

$$P_{out} = \frac{1}{2} |I_{o1}|^2 Z_{0a} + \frac{1}{2} |I_{o2}|^2 Z_{0b}, \quad (9)$$

and when  $Z_{0a} = Z_{0b} = Z_0$ ,  $P_{out}$  can be simplified as below

$$P_{out} = \frac{n^2 R_{ds}^2 Z_0^2}{(nZ_0 + 2R_{ds})^2} g_m^2 \frac{V_i^2}{2}. \quad (10)$$

The power delivered from the input source  $P_{in}$  is

$$P_{in} = \frac{1}{2} \frac{V_i^2}{Z_o}, \quad (11)$$

where  $V_i$  are the supply voltages and  $Z_o$  is gate line characteristic impedance. The overall gain  $G$  is given by

$$G = \frac{P_{out}}{P_{in}} = \frac{n^2 R_{ds}^2 Z_0^2}{(nZ_0 + 2R_{ds})^2} g_m^2. \quad (12)$$



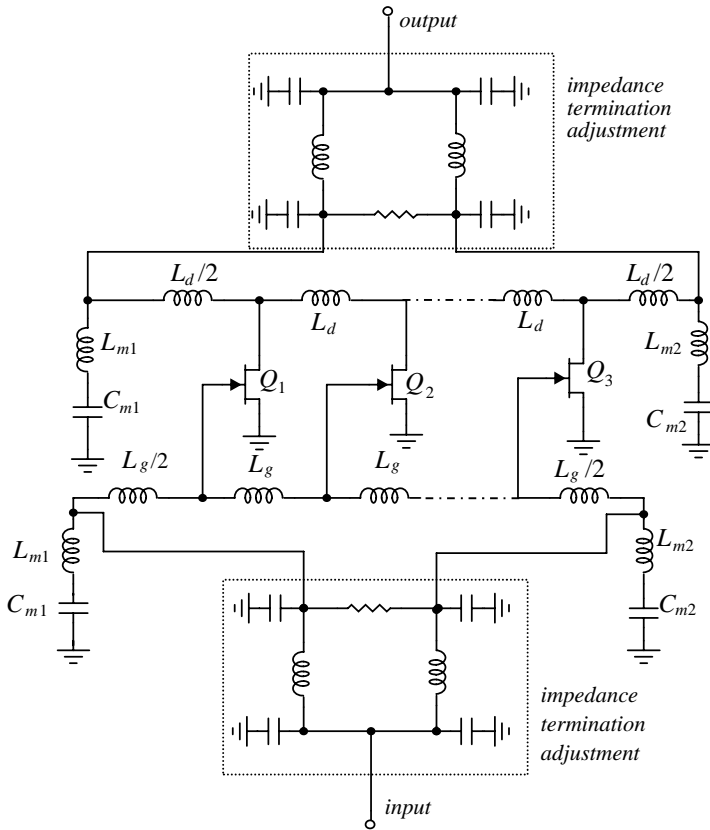
From (10), it can be derived that when increasing  $Z_0$ , a higher gain and output power can be obtained. Unfortunately, the correspondent degradation of the output return loss is a critical limitation [7]. The gain as a function of the output loads  $Z_{0a}$  and  $Z_{0b}$  for different number of FETs ( $n = 2, 3, 4$ ) and the corresponding return loss are discussed in [7]. One can conclude from [8] that the right values of  $Z_{0a}$  and  $Z_{0b}$  for the chosen  $n$ , will lead to optimum power performance without trading off output return loss. Hence,  $f_o$  of the drain line is selected to improve the output matching over the entire bandwidth.

#### 4. DESIGN AND SIMULATION ANALYSIS OF THE DUAL FED DA

The basic distributed amplifier design guidelines are applied, including the desired transistor, gate and drain transmission line synthesis, number of section, etc.. A LDMOS  $n$ -type MOSFET packaged device from Mitsubishi (RD01MUS1) is selected, for its medium power performance along with the availability of a nonlinear model. In this work, the number of stages selected for the DA is  $N_{opt} = 3$ . The resulting modified DFDA topology is shown in Fig. 9.

The inductances of gate and drain lines are determined from the value of the line image impedance and  $\omega_c$ . In order to force the currents in the drain line to interfere constructively (add in phase), the phase shift per section of the gate and drain lines must be equalized. The phase velocities synchronization between the gate and drain line is achieved by adjusting the inductance value of the gate line (the capacitively coupled technique, where discrete capacitor in series form to each gate of the transistor is not implemented) [12]. A  $m$ -derived network serves as wideband image impedance image termination and it is placed at both ends of the gate and drain lines. A  $m$ -derived half section is designed with  $m = 0.6$  for best flatness across the bandwidth [13]. For the termination adjustment network,  $L$  and  $C$  are selected according to (6) and (7), where an optimum  $f_o$  and  $Z_o$  will be identified in the simulation analysis. For convenience, the characteristic impedance of the splitter  $Z_o$  is set to  $70.7\ \Omega$ , but  $f_o$  has to be determined.

The presented analysis shows that by applying the termination adjustment with proper  $f_o$  selection at gate line, a bandwidth improvement is obtained. It notable that a small degradation of the gain is expected, due to the splitter losses. Nevertheless, the gain of the amplifier can be boosted in a similar way at the drain line or by applying a tapered drain line [3, 4]. Hence, as a guideline, tuning the  $f_o$  of the termination adjustment network in the range lower than

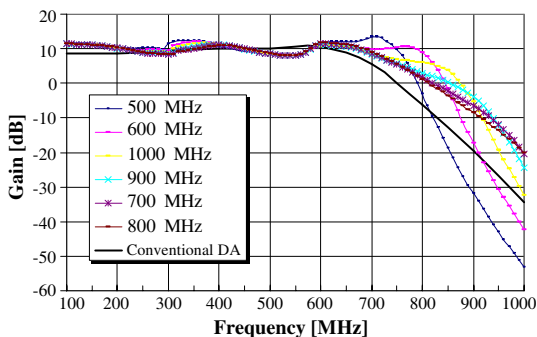


**Figure 9.** Modified DFDA with termination adjustment network ( $m$ -derived) at both gate and drain lines.

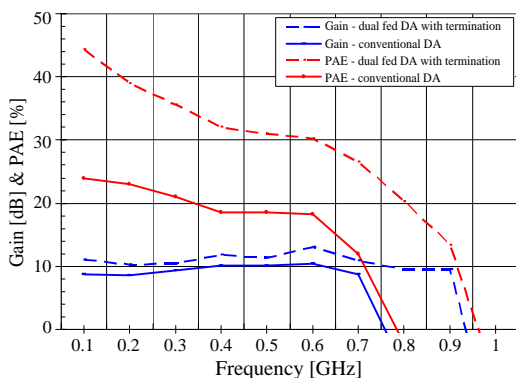
line cutoff frequency  $f_c$  and higher than the conventional DA center frequency, determines a significant bandwidth extension, making it preferable over the conventional DA strategy.

Nonlinear analysis (Harmonic Balance) of the modified DFDA making use of the non-linear active device model and passive components models is performed. The DC bias is  $V_{GS} = 2.1\text{ V}$  and  $V_{DS} = 7.8\text{ V}$ ; an input power  $P_{in} = 17\text{ dBm}$  is applied to the modified DFDA input. The analysis indicates that an optimum selection of  $f_o$  (i.e.,  $f_o \sim 600\text{ MHz}$ ) leads to a bandwidth extension of  $\sim 220\text{ MHz}$ , compared to conventional DA (black curve), as shown in Fig. 10.

The HB simulation to simulate the large signal performance (with Advanced System Design simulator making use of the non-linear active device model and passive components models) of the 3-section modified DFDA is compared to a conventional DA. Both topologies adopt the

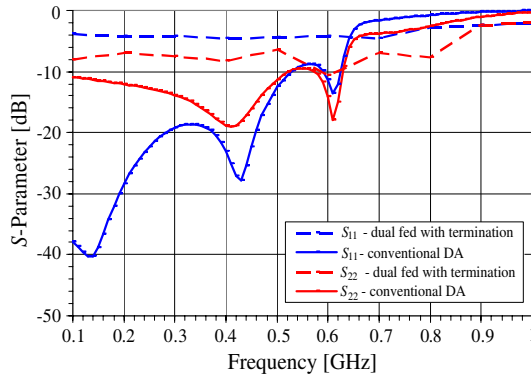


**Figure 10.** Gain vs. frequency for various cases of  $f_o$  tuning. Fine selection of  $f_o \sim 600$  MHz (pink curve) leads to bandwidth extension.



**Figure 11.** Gain and PAE comparison for modified DFDA and conventional DA having same input and output artificial transmission line, DC biasing scheme at the same condition ( $V_{GS} = 2.1$  V and  $V_{DS} = 7.8$  V) and same  $P_{in} = 17$  dBm).

same device, same input and output artificial transmission line, DC biasing scheme at the same condition ( $V_{GS} = 2.1$  V and  $V_{DS} = 7.8$  V) and same  $P_{in} = 17$  dBm is applied to both amplifiers. The  $f_o$  of the input and output adjustment termination networks is fixed at 600 MHz. The gain of the conventional DA is  $9.5 \pm 1$  dB whereas the modified DFDA shown an increase of about 2 dB across 100 to 900 MHz bandwidth (Fig. 11). The PAE for the conventional DA is lower than 20% whereas the PAE for the modified DFDA is increased of more than 30% (50% of improvement), as shown in Fig. 11. The remarkable achievement of the modified DFDA consists in the relevant



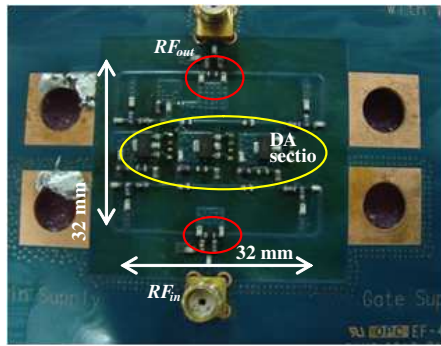
**Figure 12.**  $S$ -parameters comparison for modified DFDA and conventional DA having same input and output artificial transmission line, DC biasing scheme at the same condition ( $V_{GS} = 2.1\text{ V}$  and  $V_{DS} = 7.8\text{ V}$ ) and same  $P_{in} = 17\text{ dBm}$ ).

extension of the frequency band of 200 MHz over conventional DA. The  $S$ -parameter simulation of the modified DFDA is given in Fig. 12, and obviously the input and output return losses are degraded below 600 MHz as compared to conventional DA (but still acceptable value). Since the tuning resonance frequency of the termination adjustment is 600 MHz, the return loss exhibits significant improvement beyond 600 MHz. However, the input and output return loss is  $< -5\text{ dB}$  across bandwidth. Therefore, it is choice of the designer to identify  $f_o$  of the input and output termination networks to achieve the optimum power performance over the entire bandwidth operation.

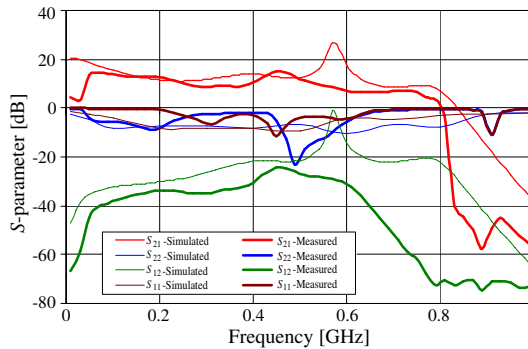
## 5. MEASUREMENT RESULTS

In order to experimentally validate the DFDA with the termination adjustment network concept, a prototype board is fabricated using FR4 3-layers PCB material, with permittivity  $\epsilon_r = 4.5$  and thickness  $h = 30\text{ mil}$ . The photograph of the resulting PCB board is given in Fig. 13. Each device is biased with 7.8 V drain supply voltage. A bias voltage of 2.1 V is applied to each gate resulting in class AB operation, with quiescent current  $I_{dq}$  of  $\sim 90\text{ mA}$  ( $10\% I_{max}$ ).

The measured results of small-signal and power performance of a 3-section modified DFDA, are shown in Fig. 14 and Fig. 15. The input return loss ( $S_{11}$ ) is below  $-10\text{ dB}$ , but the output return loss ( $S_{22}$ ) is approximately  $-6\text{ dB}$  across 100 to 800 MHz frequency range, as in Fig. 14. It is possible to provide an optimum  $f_o$  at drain line



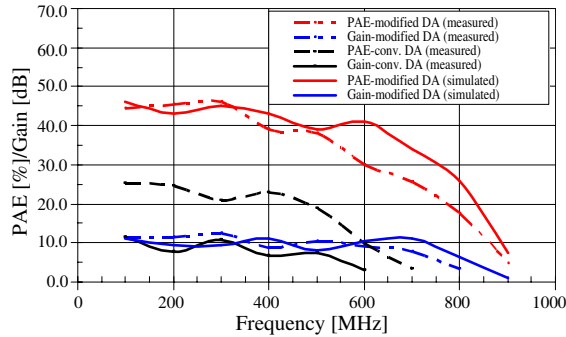
**Figure 13.** Photograph of the modified DFDA prototype board. The effective DA size area is 32 mm × 32 mm. Red color circle represents termination adjustment network (at gate and drain section).



**Figure 14.** Measured versus simulated results of small-signal  $S$ -parameters across frequency range of 100 to 900 MHz.

to improve further  $S_{22}$ . There is a minimum gain peaking observed in small signal performance although it is visible in simulated results. Simulations of gain and PAE of the both DFDA and conventional DA are including realistic technological aspects by a full wave modeling of EM simulator of PCB stack-up, via-holes, grounded heat-sink, parasitic, screw modeling, etc.. The PCB layout structure was imported from Cadence to CST environment, and then simulation is performed in ADS (HB simulator) with layout information from CST. A good agreement between simulation and measurement results is obtained for both the DFDA and the DA (for reference in Fig. 15 are reported the simulation for the DFDA).

An output power of  $\sim 28$  dBm, gain of 10 dB and PAE  $> 20\%$  are achieved throughout 100 to 800 MHz frequency range as shown in



**Figure 15.** Measured *vs.* simulated results for PAE and gain across the 100–900 MHz frequency range.

**Table 1.** Summary performance of power and PAE over the 100–800 MHz for DA realizations with low DC supply voltage.

	<i>This work</i>	[5]	[4]	[3]	[18]	[19]
PAE (%)	20–45	18–27	20–47	28–30	14–29	13–21
Power (dBm)	29.2	30	27.4	26	-	-
DC supply (V)	7.2	7.2	6.5	4.5	5	6
Device	LDMOS	LDMOS	HBT	pHEMT	pHEMT	CMOS

Fig. 15. As a comparison, a conventional 3-section DA having the same input and output line impedances, and the same DC biasing scheme is built and measured. The same PCB properties and layer structure were adopted. The DFDA provides higher efficiency performance and a bandwidth wider of about 180 MHz with respect to the conventional DA. An average PAE improvement of 15% is obtained across the bandwidth. A good agreement between simulations and measurement results is obtained.

A comparison with previous results is summarized in Table 1 where the output power and the PAE performance over the bandwidth 100–800 MHz for different DA realizations with low DC supply voltage are listed. *This work*, [4] and [5] report operating frequencies for the 100–800 MHz range, while [3] is operating in the bandwidth 10–1800 MHz with 4.5 V power supply. On the other hand, recent works from [20, 21]

demonstrated wideband amplifier for SDR applications using pHEMT and CMOS technology, providing, however, a lower output power.

*This work* demonstrates remarkably efficiency improvement over the entire bandwidth (100–800 MHz), with 7.2 V drain supply, making this approach suitable for SDR driver applications. In [22, 23] is shown the narrow frequency UHF band that demonstrated high efficiency employing switched gain stage and class E approaches, respectively with 7.2 V. Other recent works related to high performance power amplifier are reported in [24, 25] with GaAs HBT and CMOS technology, respectively. In the other hands, power amplifier design with parallel-coupled transformer matching is demonstrated in [26, 27].

## 6. CONCLUSION

A novel topology of Dual Feed Distributed Amplifier with terminations adjusted for optimum power performance with low DC supply voltage is presented. The termination adjustment provides a relevant improvement in comparison to the conventional DA topology and demonstrates the effectiveness of the topology. An output power of  $\sim 29$  dBm, 10 dB gain in the whole bandwidth for SDR (100–800 MHz), with a PAE of 20–45%, obtained by low DC supply voltage is experimentally demonstrated. This is an effective low cost and low area consumption design which is suitable for SDR applications.

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