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# SIGNAL INTEGRITY AND ELECTROMAGNETIC BROADBAND PACKAGING MODEL EXTRACTION OF FULL DIFFERENTIAL BANDPASS FILTER ON IPD WITH BGA PACKAGING

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**Abstract**—Since the system-level package was proposed, the electronics industry has increasingly attached importance to both directly relevant and related issues, and the scope of system-level package usage has increased. Creating more complex system-level package structures, thereby leading to the design of overall electrical effects, requires more electromagnetic simulation resources, and therefore a great deal of time in the design process. The main purpose of this paper is to analyze the effects of system-level packaging, and to establish systems-in-package in accordance with electrical specifications. Using a segmented approach, this paper also builds an overall model for designers to predict electrical characteristics, thus shortening the product development schedule. In this paper, the transmission effects of a substrate are analyzed by changing the length of the substrate transmission line, with or without a thermal ground ball and ground ring. Previously established package IP are cascaded to establish the model of the package substrate, which verifies the feasibility of the package IP. We then analyze the characteristics of the interference between chips and package using an integrated passive device, and propose a complete package equivalent circuit model.

## 1. INTRODUCTION

As shown in Fig. 1 [1–13], Moore's Law proposed that the number of transistors on an integrated circuit would double every 24 months (in 1975 this was changed to 18 months), enabling more chip functions

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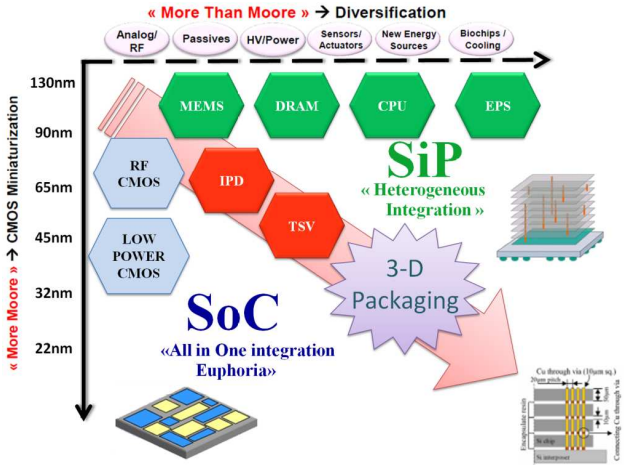



**Figure 1.** Developmental trends regarding Moore's law and the evolution of package structure.

within the same area. Since Moore's Law increases chip integration, the System on Chip (SoC) structure has also flourished. In the past few decades, Moore's Law has been quite consistent with real circumstances, including economic developments in the electronics industry. In conformity with the law, semiconductor dimensions have shrunk to 22 nm in recent years. However, we may be approaching the lower size limits for semiconductors. Because package size is easier to reduce than chip size, important trends have been occurring in package development. It has been difficult to further reduce the size of single-chip packages, so if chips can be packaged individually, the size of a system can be reduced. Currently, to achieve more functions in the same area, the concepts of 3D stacked packages, side-by-side packages, and even system in package (SiP) have been proposed. Designers are therefore setting multiple chips in a single package, making a given system easy to replace and improve. The advantages of SiP can reduce the cost of debugging.

Although SiP technology can reduce both size and cost, two important issues must be considered. The first is package signal degradation [14–17]. High-frequency and high-speed technology make it impossible to ignore this factor. Signals passing through the package components — such as the wire bond, transmission line or routing, plated through-hole (PTH) via, and ball — can be distorted because of the skin effect of the conductor, crosstalk/coupling between adjacent components, impedance mismatch at the interface of line and via or

line and ball, the resonant cavity in the power/ground plane and the great radiated emission with bad power/ground design. Therefore, a package designer can propose many structures to suppress these issues arising from bad package design, including simultaneous switching noise (SSN), IR drop, and signal attenuation. Some solutions include a power/ground ring, thermal ground ball, or embedded electromagnetic band-gap (EBG).

The second issue is design time. Generally, package designs require an electromagnetic (EM) simulator to predict electrical performance. Analyzing the EM effects of a package or SiP requires that both chip and package be placed into the EM simulator. However, in reality the structural complexity of a SiP demands too many computer resources and a great deal of time for such analysis, increasing the development and debugging costs. Hence, this is not a good method for developing a new product.

One feasible alternative is to conduct separate chip and package analysis and then combine the results using circuit simulation software. When chip and package are separated, EM simulation is faster because the structure is relatively simple. Although circuit simulation is quicker than EM simulation, the latter is still necessary, so to further reduce the EM simulation time, the idea of the package IP has been proposed.

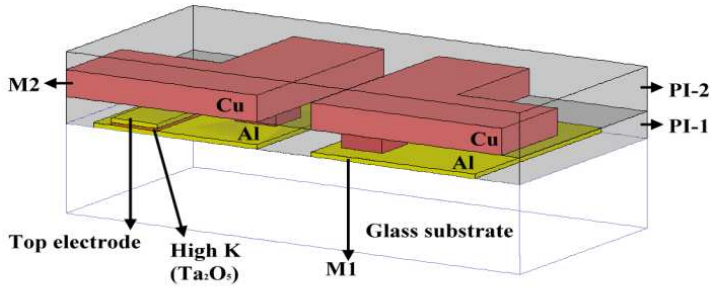
A package IP is used to establish an equivalent model for the effects and structures of a variety of packages [18–20]. Those structures include wire bond, plated through-hole, transmission line, finger, etc. [21]. The package IP is used to predict the signal path effect from package input to output using a circuit simulator, so no EM simulation is required in the design process. With chip data obtained via simulation or measurement, and with the use of a package IP, the design time can be minimized. Nonetheless, interference between the chip and substrate is still an issue, and determining the effect of interference is very important when using a package IP.

In this paper, several different packages are designed to analyze the electrical effects of each package type, and a package substrate model is extracted using a combination of previously developed package IPs. In addition, an integrated passive device (IPD) component is used to analyze the mutual interference between the chip and package substrate, and a complete package model is proposed.

## 2. CHIP DESIGN

A filter has an explicitly resonating nature for analyzing the signal integrity of a package, so the component with IPD technology used in this paper is a filter. The design theorem of this filter,

proposed in [22] in GIPD process, has the central frequency 2.9 GHz and [23] in PCB process, has the central frequency 5.2 GHz, has yielded very good performance using just a small area, which is appropriate for SiP technology. In this study, the filter, has the central frequency 2.1 GHz, is redesigned to verify the design theorem in ASE (Advanced Semiconductor Engineering) IPD process and investigate signal integrity issue of package; the filter structure is shown in Fig. 2.




| Metal 1 (Al) | Metal 2 (Cu) | Top electrode (Al) | High k dielectric |
|---|---|---|---|
| 1 um | 10 um | 1 um | 0.27 um |
| Glass Thickness | | Polyimide 1 (PI-1) | Polyimide 2 (PI-2) |
| 700 um | | 3.7 um | 9.5 um |

**High K ($Ta_2O_5$) dielectric :**
**-dielectric constant : 25**
**-loss tangent : 0.001**
**BCB :**
**-dielectric constant : 3.2**

**Figure 2.** Cross-sectional structure and material parameters of the IPD.

The circuit design includes three metal layers. Metal 2 is thick copper for the transformer and inductors, to achieve high $Q$, while the top electrode and metal 1 are aluminum. A high dielectric constant (high $K$) layer of $Ta_2O_5$ between the top electrode and metal 1 allows metal-insulator-metal (MIM) capacitors to be part of the circuit design. A polyimide layer or the BCB dielectric provides cover and isolation.

The transformer-based full differential bandpass filter implemented on ASE IPD technology is shown in Fig. 3. It also consists of two parallel resonant circuits (Resonator 1 and Resonator 2). By symmetrically interweaving an octagonal coil on metal 2, the mutual inductance $M$ of a transformer was realized. The underpass of a transformer was implemented on metal 1, as was the ground ring. A pair of dual MIM capacitors, located at the end of the resonators, used the top electrode and metal 1. Fig. 4 shows the overall structure and measurement details.

Figures 5(a) and (b) present comparisons of the probe measurement and EM simulation with Ansoft HFSS simulator of the

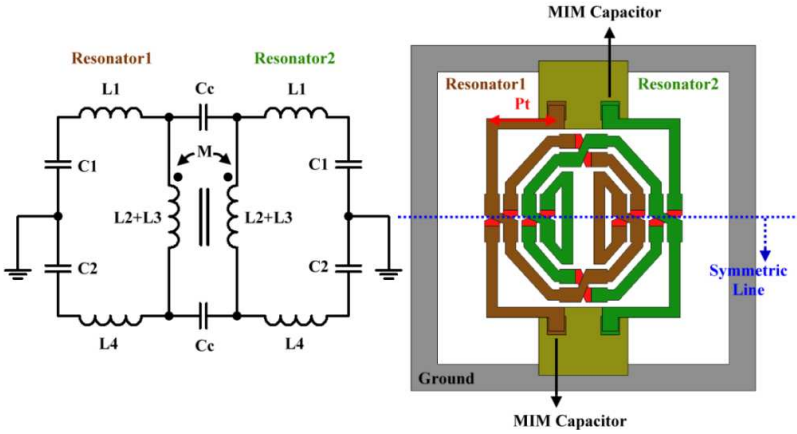
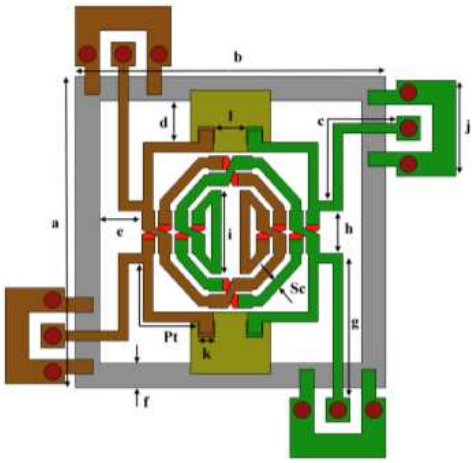


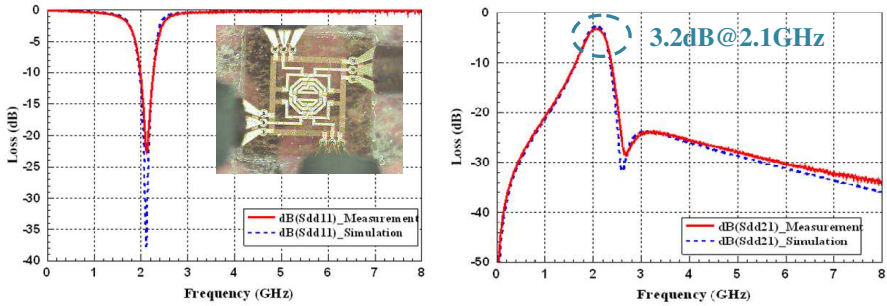

**Figure 3.** Circuit model and physical layout of the bandpass filter using the IPD.




| | Length (mm) | | Length (mm) |
|---|---|---|---|
| *Pt* | 0.47 | *f* | 0.1 |
| *Sc* | 0.03 | *g* | 0.6 |
| *a* | 1.3 | *h* | 0.18 |
| *b* | 1.3 | *i* | 0.35 |
| *c* | 0.59 | *j* | 0.4 |
| *d* | 0.175 | *k* | 0.07 |
| *e* | 0.177 | *l* | 0.13 |

**Figure 4.** Physical layout of the full differential bandpass filter on the IPD.

proposed full differential bandpass filter. The measured passband frequency is 2.1 GHz. The minimum insertion loss ($S_{21}^{dd}$) and return loss ($S_{11}^{dd}$) are 3.2 dB and 22 dB, respectively. The full differential bandpass filter implemented on IPD technology occupied an area of 1.3 mm × 1.3 mm, and the transmission zero occurred at 2.7 GHz.

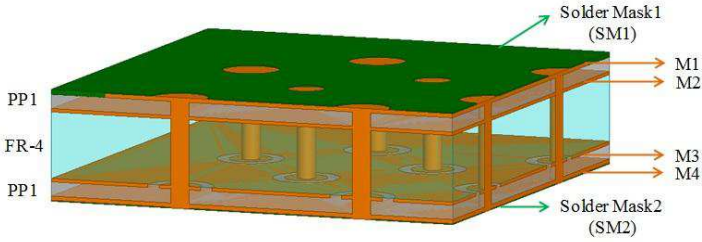



(a) Return loss (dB) (b) Insertion loss (dB)

**Figure 5.** Measured and simulated differential-mode responses on the IPD.

## 3. PACKAGE DESIGN

Generally, the package can protect the chip from outside interference, including thermal changes, physical stress, and electromagnetic waves. However, signal from the chip can be distorted when passing through the package. Investigating the routing effect on the package and reducing the attenuation can ensure the signal transmits perfectly. Fig. 6 shows the packaging cross-sectional structure with laminate FR-




| Layer | Thickness | Layer | Thickness |
|---|---|---|---|
| SM1 | 10 | M3 | 35 |
| M1 | 43 | PP2 | 150 |
| PP1 | 150 | M4 | 43 |
| M2 | 35 | SM2 | 10 |
| FR-4 | 700 | Unit | um |

***FR-4***
Dielectric constant : 4.4
Loss tangent : 0.02

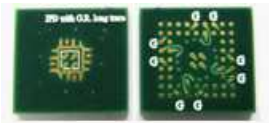
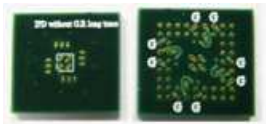
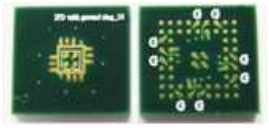
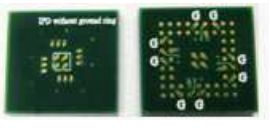
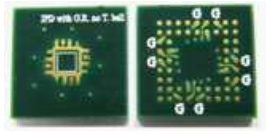
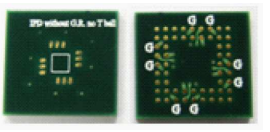
***PP***
Dielectric constant : 2.25
Loss tangent : 0.001

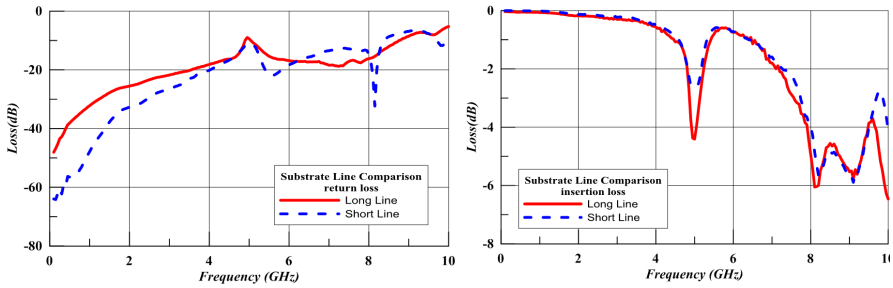
**Figure 6.** Cross-sectional structure and material parameters of the package design.

4 substrate. The signal from the chip on the top layer passes through the wire bond, transmission line, and plating through-hole to the ball land on the bottom layer.

In order to investigate the electrical effect and signal quality of different packaging structures, six packaging designs were created, as shown in Table 1. These designs can be divided into two types, routing and ground. The designs include different ground ring formations with square shape — width is 0.2 mm and length is 2.5 mm, different transmission line lengths — width is 0.2 mm and length is 2 mm and 5 mm, and various thermal ground ball designs. As every engineer knows, varying the line length and the ground system should yield differences in the signal. To study the electrical effect of the chip-package, the package layout first needs to be measured. Fig. 7 presents measured comparisons between the long and short lines. Long line and short line have the close results in insertion loss, but the comparison of return loss shows great difference before 2 GHz. It represents that the long line can lead to large radiation emission at low frequency in package design. Fig. 8 shows the results with and without ground ring. The purpose of ground ring layout is to improve the electrical

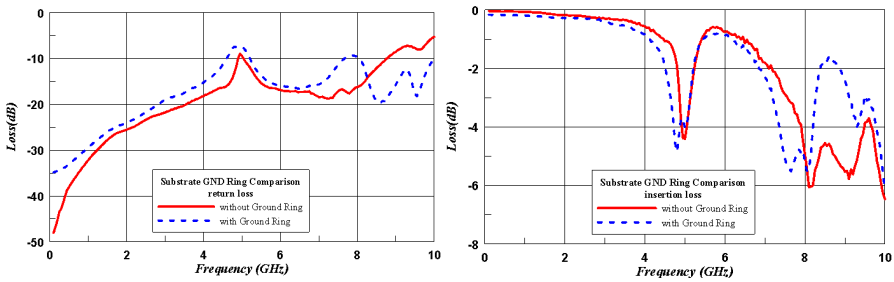
**Table 1.** Six package designs for investigating electrical effects.

| | **With ground ring** | **Without ground ring** |
|---|---|---|
| **Long line** |  |  |
| | LT_wGR_wTB | LT_woGR_wTB |
| **Short line** |  |  |
| | ST_wGR_wTB | ST_woGR_wTB |
| **Without thermal ground ball** |  |  |
| | ST_wGR_woTB | ST_woGR_woTB |




Return loss (dB) Insertion loss (dB)

**Figure 7.** Measurement comparisons for different transmission line lengths.




Return loss (dB) Insertion loss (dB)

**Figure 8.** Measurement comparisons with and without ground ring design.

effect by shortening the wire length or the return path. However, the measurement results would not included the wire effects, the improvement performance is still not obvious. As for the thermal ground ball, which is located below the die pad, its original purpose is to radiate heat. But it can also promote electrical characteristics when chips are packaged on the substrate, because it can decrease the ground inductance by shortening the signal return path to suppress the SSN or the ground bounce, using different quantities of thermal ground ball. This will be discussed in the next section.

## 4. CHIP AND PACKAGE CO-SIMULATION AND DESIGN OPTIMIZATION

As shown above, the electrical characteristics decrease after the chip is packaged to protect the circuit. Therefore, package design is an

important issue given the extensive use of high-frequency and high-speed signals. The electromagnetic effect of the package was introduced in the previous section. By packaging the IPD chip, the overall performance of chip and package can be measured. Fig. 9 shows the performance before packaging as a red line and after packaging as a blue line. At a lower frequency of about 2.5 GHz, the package does not affect the chip performance because the package is not enough small to interfere the chip. Above 2.5 GHz, the package can generate parasitic effects on the electrical performance. These parasitics include resistance with skin effect, capacitance with substrate and inductance with package routing and via.

In addition to studying the $S$-parameter of the package, we also compared the common-mode rejection ratio (CMRR) with differential signals. Fig. 10 compares the CMRR values. We found that if the chip is fully packaged, the CMRR will decrease by 10 dB. In other words, the chip balance is damaged by the package component. If

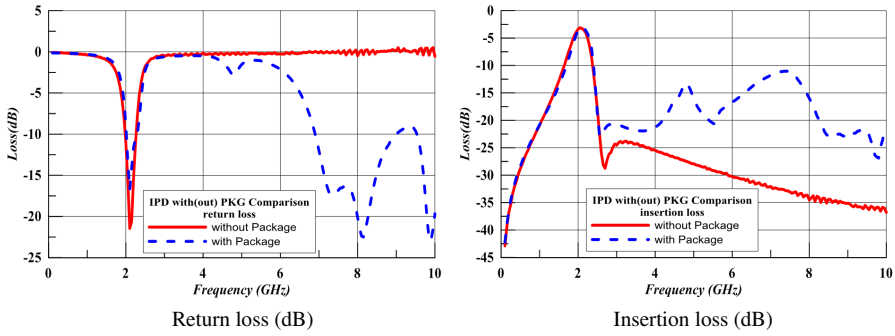



**Figure 9.** Co-simulation comparison with different transmission line lengths.

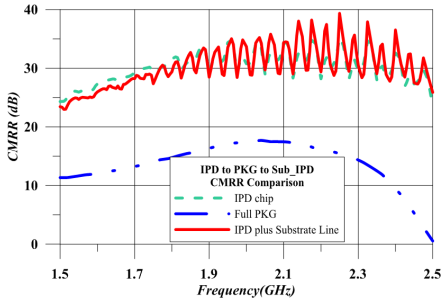
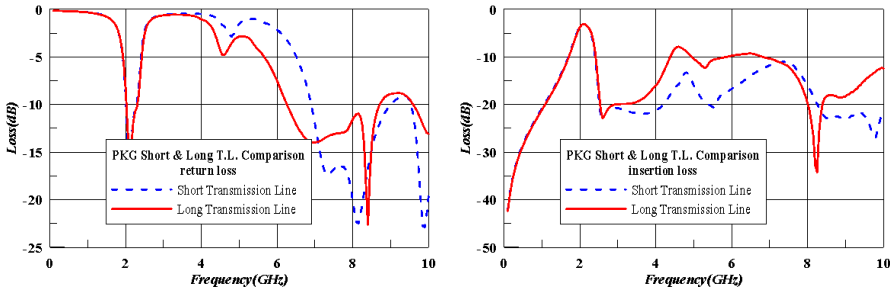



**Figure 10.** Common-mode rejection ratio (CMRR) after packaging.

the package is a real application for a new product with differential signals, it would generate enormous common-mode noise and radiate electromagnetic wave to interfere the system. It can be concluded from the measurement results in Fig. 9 and Fig. 10 that the package indeed influences the signal quality. Since technology development trends will continue to favor high-speed and high-frequency signals, package design will also gradually develop toward system integration such as system in package (SiP) and package on package (PoP). Therefore, the package design will dominate the optimization of signal integrity in the future.

Packaging can affect the electrical performance of a signal from a chip. Therefore, package choice and design are very important issues for signal integrity. Fig. 11 shows the measurement results of different routing length on the package substrate. The short line (blue) is better than the long line (red) at higher frequency about 3 GHz, due to loss caused by the skin effect and high-frequency L-C resonances.

With respect to the ground design of the package, Fig. 12 presents the measurement results with ground ring (ST_wGR_wT) and without ground ring (ST_woGR_wT). Evidently, the package with the ground ring design exhibits better performance because the ground system or signal return path is much better. This means the ground ring structure can improve the signal integrity. Fig. 13 shows the measurement data with and without a thermal ground ball. The results indicate that the thermal ground ball structure does not affect the electrical performance in this case. This is because there was no data signal, clock signal or printed circuit board, the next stage load of package, in this study, so thermal ground balls could have no significant impact on reducing ground inductance. Our future work will include package-PCB interconnection study to realize the thermal ground balls effect on suppressing ground bounce or simultaneous switching noise (SSN).




Return loss (dB) Insertion loss (dB)

**Figure 11.** Measurement comparison with different transmission line lengths.

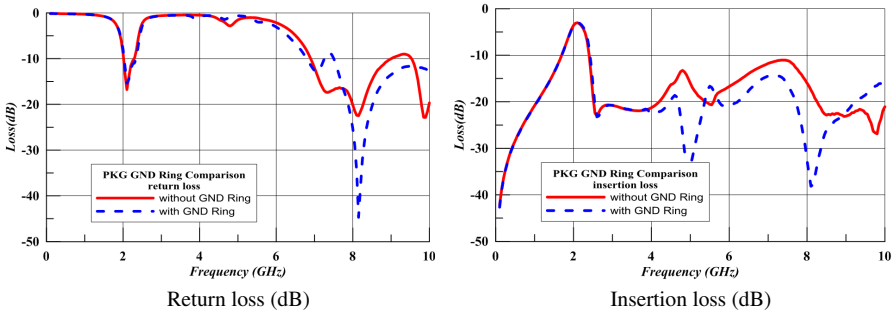



**Figure 12.** Measurement comparison of different ground ring designs.

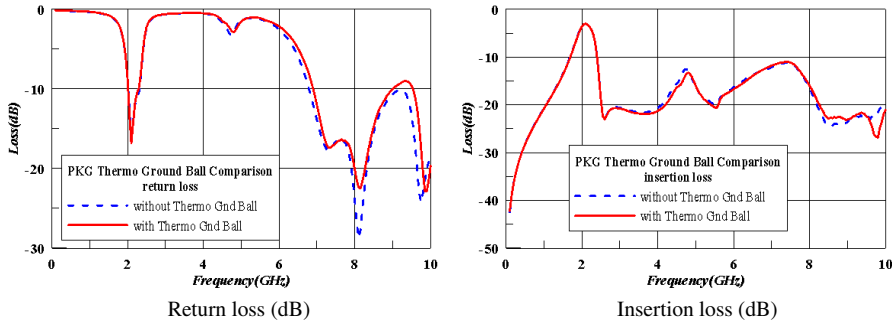



**Figure 13.** Measurement comparison with and without a thermal ground ball.

In summary, many key factors influence the electrical performance or signal integrity of high-frequency and high-speed signals. The package substrate effect could be decreased by some of these factors, including impedance control, resonant cavity in the power/ground plane, radiated emission by crosstalk, or coupling and skin effects. The simple solution for increasing electrical performance is shortening the routing length and spacing, and improving the ground design.

## 5. PACKAGE IP DEVELOPMENT AND VALIDATION

In order to investigate physical performance, the electrical modeling needs to be extracted. By completing the following procedure, the ideal lump components, including inductance, capacitance, and resistance, can be known. From the formula (1)–(3) [24] and Fig. 14, the time delay, characteristic impedance and effective width of transmission line can be obtained by using physical factor and dielectric factor. Then,

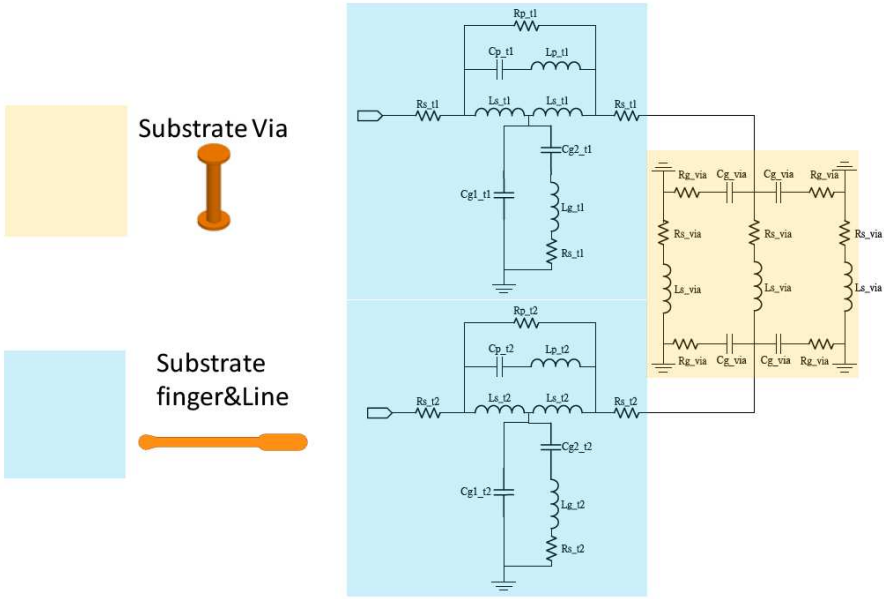



**Figure 14.** Package substrate component model.

the transformation from electrical effect to lump model can be analyzed by Equations (4)–(7) [25, 26]. On the other hand, the via, an inserted component on package or PCB, can provide signal a path from top layer to bottom layer. Therefore, modeling of via must be created and extracted to accomplish the data base of package modeling. The synthesized theorem is shown in (8)–(9) [27].

$$t_{pd} = 1.017\sqrt{0.457\varepsilon_r + 0.67}\left(\frac{ns}{ft}\right) \tag{1}$$

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \tag{2}$$

$$w_{eff} = 0.8w + t \tag{3}$$

$$L_0 = Z_0^2 C_0 \left(\frac{pH}{ft}\right) \tag{4}$$

$$C_0 = 1000 \times \frac{t_{pD}}{Z_0}\left(\frac{pF}{ft}\right) \tag{5}$$

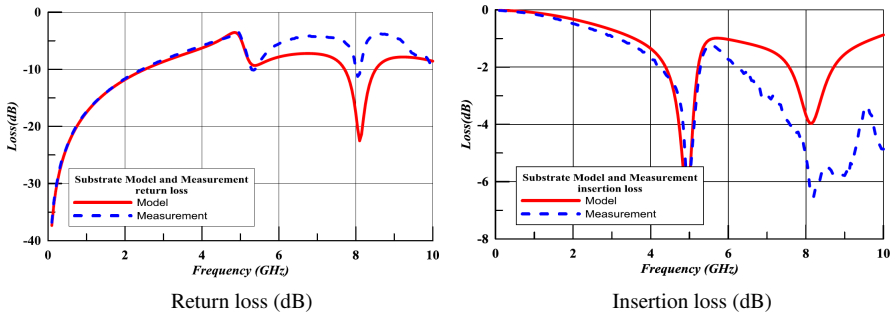
$$C = C_0 \times l \tag{6}$$

$$L = L_0 \times l \tag{7}$$

$$L = 5.08h\left[\ln\left(\frac{4h}{D}\right)+1\right] \tag{8}$$

$$C = \frac{1.41\varepsilon_r T D_1}{D_2 - D_1} \tag{9}$$

From the value of the components, a solution can be realized if we want to suppress ground inductance or dielectric capacitance, and so on. The more important application is to save product development time, as EM simulation urgently needs to be replaced. This section therefore proposes a broadband model, or package IP. First, the package substrate needs to be segmented into routing on the top layer, PTH via, and routing on the bottom layer. Then, measuring the segmented component and combining all the data completes the co-simulation results. Based on these results, the models using lump components, including resistance, inductance, and capacitance, were extracted and validated. Fig. 14 shows the lump model of the routing of length 2 mm and substrate via of length 1.2 mm and diameter 0.3 mm, while Fig. 15 compares the model and measurement results. The broadband results show that the model is in good agreement with the measurements and the bandwidth is up to 10 GHz.




Return loss (dB) Insertion loss (dB)

**Figure 15.** Comparison results of package substrate model and measurement.

In this study, we not only determined the electrical performance of the package but also extracted the chip-package effect. Fig. 16 shows an overall model by lump component. This model extracts the performance from the filter by chip, wire bond, transmission line, and PTH via. Moreover, in this structure, the chip and package do not have the same ground, so the ground effect compensation has been extracted using L-C series. The comparison results in Fig. 17 indicate that the model is in agreement with the measurements and the bandwidth is up to 10 GHz. In other words, this model can replace the chip-package structure.

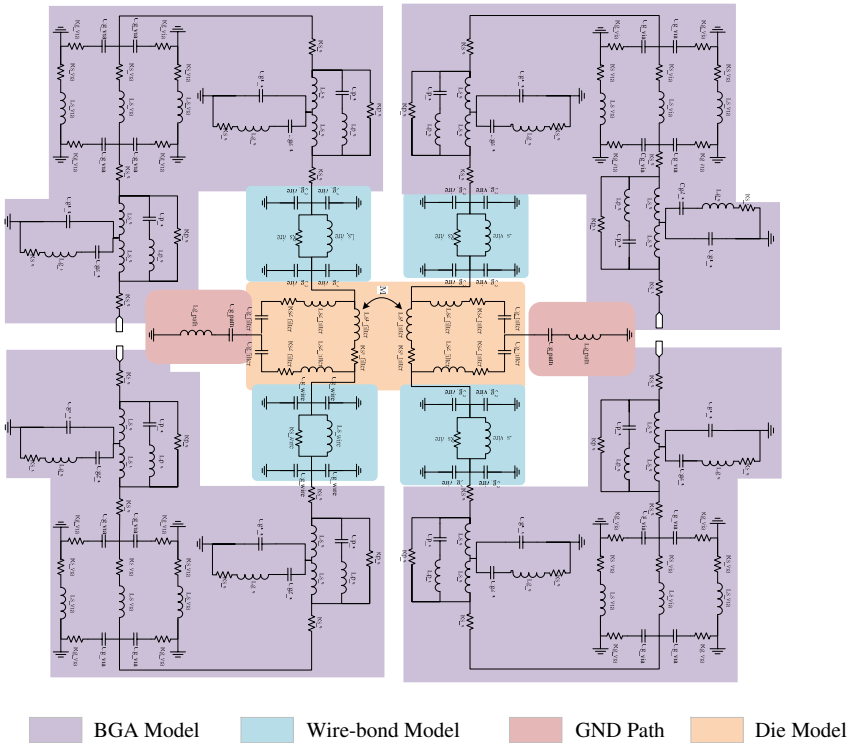
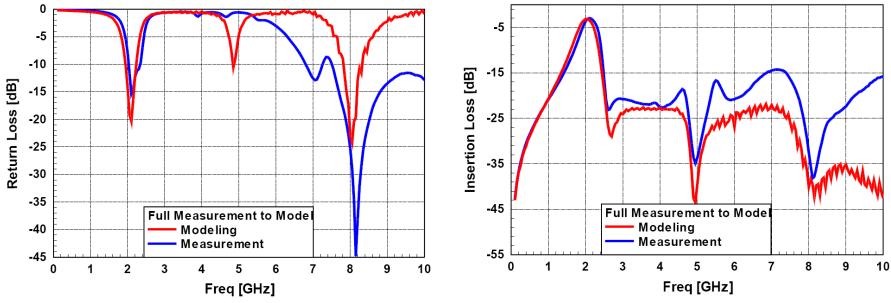



**Figure 16.** Co-simulation comparison of different thermal ground ball designs.




Return loss (dB) Insertion loss (dB)

**Figure 17.** Co-simulation comparison of different thermal ground ball design.

## 6. CONCLUSION

This paper has presented a study of the electrical performance of package substrates and equivalent models by lump component,

to extract information about packaging quality with high-frequency and high-speed signals. We utilized a filter with IPD technology composed of a double resonator and packaged in BGA substrate. In order to study the signal integrity of the package substrate, six different substrates were designed and measured. These structures included different line lengths, ground ring designs, and thermal ground ball designs. Next, the measured data of the chip and package were subjected to co-simulation in a circuit simulator. The results indicate that the short line and ground ring designs have better signal transmission effects. In addition, the thermal ground ball made no difference to the electrical performance, because it can cause a SSN effect with an active chip in the package. Finally, the physical model from chip to package, explained by lump component, also was extracted to understand the physical performance, including routing, via, and grounding effect. This overall model has the potential to save design time by eliminating the need for EM simulation.

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