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HIGH-SPEED, SIMPLIFIED DESIGN OF AN IMAGE RECEIVER FOR WIRELESS CAPSULE ENDOSCOPY

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Abstract—Just over a decade ago, wireless capsule endoscopy (WCE) was introduced as a novel alternative to conventional wire or probe endoscopy to examine disorders of the human gastrointestinal (GI) tract. Yet, the persistent inability of transmitting high-quality images due to limited data rate of the telemetry system continues to be an issue of major concern. Thus, high-data-rate telemetry systems are essential due to the widespread use of the WCE technique. In this paper, we present such a telemetry system that includes a highly-simplified receiver for the use in WCE. Unlike the conventional architecture of a radio frequency (RF) receiver, the architecture of the new receiver allows the direct conversion of analog RF signals to digital signals, eliminating the need for any frequency conversion in the analog domain. Our receiver system consists of sub-blocks, a low-noise amplifier (LNA), a logarithmic amplifier (LA), a power detector (PD), and a comparator. The common-source cascode LNA was designed with its frequency spectrum centralized at 450 MHz, which was determined by electromagnetic (EM) simulation of the path loss in the GI tract of the human body. To ensure that the higher data rate, i.e., 100 Mbps, could be attained, the LNA was designed for a system bandwidth of 100 MHz, i.e., 400–500 MHz. The LNA and the three cascading blocks in combination have total gain of 80 dB to

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compensate for the losses in the weak signals that are received. The LNA and the LA, including the PD and the comparator, require 17-mA and 337-μA currents, respectively, from a 1.5-V, DC source.

1. INTRODUCTION

Endoscopy is a technique that allows doctors to see the human digestive tract and diagnose the potential causes of the patient's discomfort. In recent years, this technique has been simplified and enhanced by the development of an ingestible, wireless capsule, leading to assessments of the GI tract being conducted by means of wireless capsule endoscopy (WCE) [1]. This technology is non-invasive and allows painless endoscopy, significant improvements over the complexities associated with the conventional wire endoscopy that was used earlier. In addition, WCE has the ability to see the entire length of the GI tract, whereas conventional wire endoscopy allowed the physician to view only the upper portion of the small intestine.

However, the limitation of WCE that deters its more extensive use is the poor quality of the images it provides [2, 3]. Recently, high-speed, low-power telemetry systems have been developed that are capable of providing high-quality images at greater frame rates, and these new systems show great promise for extending the applicability of WCE. Thus, much of the ongoing research is focused on the development of telemetry systems that require less power and provide higher rates of data for high-resolution images. The first clinical capsule system, developed by Given Imaging, uses a telemetry chip produced by Zarlink Semiconductor, Inc. (Canada) that supports a data speed up to 2.7-Mb/s, which is enough for transmitting and receiving 320×320-pixel images at the rate of two frames per second. The power consumption is only 5.2 mW [4]. Subsequently, many RF telemetry systems that offer reduced power consumption and improved data rates have been developed for WCE.

Currently, the super-heterodyne architecture is the common choice for the RF transceiver due to its superior sensitivity, stable frequency, and selectivity. For WCE application, a super-heterodyne transmitter and a receiver were implemented on a single chip in [5]. But this system has maximum data rate of only 1 Mbps. A near field frequency shift keying (FSK) transmitter has been proposed in [6] which consume only 2 mW DC power but its transmission capacity is only up to 2 Mbps. The impulse radio ultra-wide band (IR-UWB) technology [7–9] is good candidate for providing both a high data rate and a low power requirement. A UWB-OOK system was developed in [8], and it provided a data rate up to 10-Mbps and was capable

of transmitting and receiving images with resolutions of 640 × 480 pixels at the rate of 2.5 frames/s. However, the use of the UWB technique in WCE is problematic because its high frequency carrier is attenuated significantly by the biological tissue that makes up the walls of the small intestine [10, 11]. Most recently, considering the RF signal's attenuation by the body tissue, Kim et al. developed a high-speed, highly-efficient capsule endoscopy system that consists of a gain-separated, super-heterodyne receiver, and it achieved a data rate 20 Mbps [12]. Adding to this, a field-programmable gate array (FPGA) based high speed receiver with the receiving rate 20 Mbps is proposed in [13]. The 20-Mbps channel can transmit images with resolutions of 640 × 480 at a rate of eight frames per second without compression. Clearly, the present telemetry systems for WCE are incapable of transmitting and receiving high quality images at the rate of 30 frames per second.

Thus, after introducing our high-speed transmitter system in our previous article [14], we now propose a high-speed, simplified-receiver system for WCE. The architecture of the proposed receiver system allows the direct conversion of analog RF signals to direct digital signals. The entire receiver circuit was designed using 0.18-μm Complementary metal-oxide-semiconductor (CMOS) technology. The simulated results of the proposed receiver showed that it was capable of receiving high-quality images.

2. EM FIELD SIMULATION FOR PATH LOSS

The human body is a complex composite of many different tissue layers that have different electrical properties (permittivity and conductivity) and that change with frequency [15]. In WCE, the selection of the frequency of the system has a significant influence on the performance of the system, because path loss in the GI tract of the human body depends on the frequency [16]. In order to determine the trade-off between the frequency of WCE's telemetry system and the path loss in the GI tract, [10] analyzed the path loss. The heterogeneous, digital, body model described in [17] was used to analyze the path loss. The simulation setup for determining path loss is shown in Figure 1 [10]. Rather than using the entire body model, the simulation used a slice of body model from the selected locations to form a virtual waveguide that measured 10 cm × 10 cm × D cm, where 'D' is the distance between the two waveguide ports. The EM signal was passed through this virtual waveguide. Two waveguide ports, i.e., port 1 (positive) and port 2 (negative) were used as a source and a receiving port, respectively. Port 1 was placed inside the body, and

port 2 was placed outside of the body. Port 2 must be touching the patient's skin to produce more accurate results. The simulated path loss is summarized in Figure 2 [14]. Clearly, the path loss saliently varies with frequency and anatomic region of GI track. The average (irrespective of anatomic regions) path loss shows that path loss was significantly low under the frequency 500 MHz. Thus, we considered bandwidth between 400 MHz and 500 MHz, i.e., about 450 MHz, to be the most suitable selection for a telemetry system to be used in WCE.

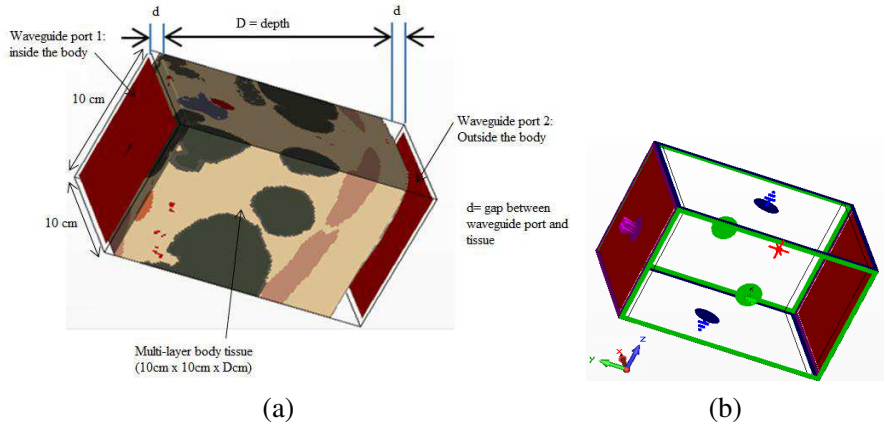

Figure 1. (a) Simulation setup for investigating path loss in the GI tract; (b) boundary condition [10].

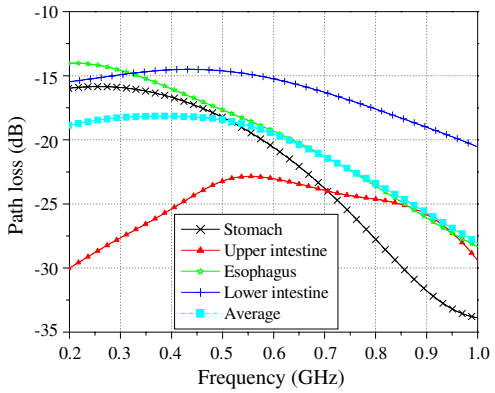

Figure 2. Variation of path loss in the human body [14].

Table 1. Link budget of the proposed receiver system.

Frequency of the System @ 450MHz	Power budget	
Output power, transmitter	−4 dBm	−74 dBm
Gain, transmitting antenna	−10 dB	
Path loss	−40 dBm	
Gain, receiving antenna	−5 dB	
Link margin	−15 dB	
Noise, receiver	5 dB	
SNR (at BER $\leq 10^{-6}$)	14 dB	
Thermal noise	−94 dBm	

3. DESIGN OF THE RECEIVER

3.1. Link Budget Calculation

According to the path loss analysis in the GI tract, the optimum frequency for WCE to minimize the attenuation of the RF signal was 450 MHz [10]. The high-speed image transmitter was introduced in our previous article [14], and it has a transmitting signal bandwidth of 100 MHz at the on-off keying (OOK) modulated data rate of 100 Mbps. The transmitter had a power output of −4 dBm. In the link budget calculation, the gains of the transmitting and receiving antennas were considered to be −10 and −5 dB, respectively. Table 1 shows that the total loss in the body was −40 dB (from the path loss simulation). Although the heterogeneous digital body model was used in the path-loss analysis to achieve better accuracy, nonetheless the investigated path loss still was not absolutely accurate because it varies with the condition of the patient's health. This led us to set the link margin at 15 dB. Therefore, the expected receiving power was −74 dBm when the transmitting power was considered.

Based on the above considerations, the strength of the received signal was considered to be above −80 dBm. The power budget of the receiver was selected for the maximum data rate of 100 Mbps with a bit error rate (BER) of less than 10^{-6}. The BER of the OOK system was given by [18, 19] as follows:

$$\mathrm{BER} = \frac{1}{2}\, e^{-\mathrm{SNR}/2} \tag{1}$$

Here, the system must have a minimum SNR of 14 dB to make the BER less than 10^{-6}.

3.2. Architecture of the Receiver

In WCE, the receiver must compensate for the large attenuation of the RF signal that occurred in the GI tract. Considering the simplicity of the system, a scheme for converting RF analog signals to digital signals [20] was used in this design. Figure 3 shows the architecture of the proposed receiver, which consists of LNA, LA, PD, and a comparator. In this receiver system, the incoming RF analog signals are converted directly to baseband digital signals, meaning that this scheme does not require an IF stage, local oscillator, mixer, and some other complex filtering parts. This receiver takes less area and uses less power than conventional RF receiver systems. To compensate for the large attenuation of the received signal, the total gain was divided into two sections, i.e., LNA and LA.

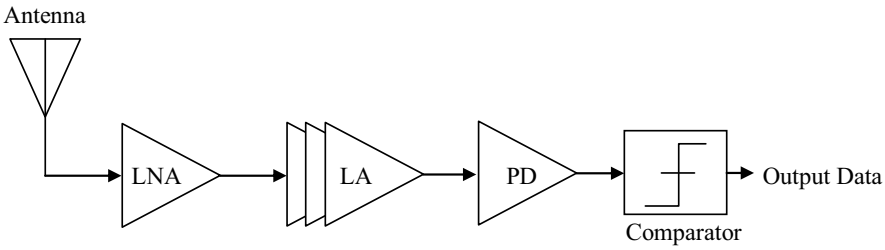

Figure 3. Block diagram of the proposed receiver system.

First, the received weak signal is amplified by the LNA, and then the remaining gain is provided by the multi-stage LA. After the power detector, the power level is compared with the reference power to determine whether the received signal level is zero bit or one bit of baseband signal.

3.3. LNA Design

The low-noise amplifier (LNA) is the initial gain stage of a typical receiver, and it is one of the most important blocks. Weak RF signals coming from the antenna are amplified by the LNA as much as possible, while minimizing the amount of noise that is introduced to the signal. Generally, the LNA is characterized by the vital parameters of voltage gain, noise figure (NF), bandwidth, input-output isolation, linearity, and power consumption. In any particular application, the selection of the topology of the LNA is a complex trade-off of these parameters. The common source and the cascode are the two most commonly used topologies of the LNA. Although the cascode configuration lacks

linearity due to the stacking of load and driving transistors in series, it is still preferred over the common source configuration for most applications because it has a high voltage gain, low noise, and input-output isolation. This analysis led us to use the cascode topology to design the LNA block. Figure 4 shows the complete circuit of the proposed LNA.

In designing the LNA, it is useful initially to know the optimum width of the driving transistor. According to the relation given in [21], the optimum length in the 0.18 µm CMOS process can be expressed as:

$$W_{opt} = \frac{1}{170 f C_{ox}} \text{ [µm]}, \tag{2}$$

where f is the frequency of the system in GHz, and C_{ox} is the gate oxide capacitance per unit area, which is $8.517\,\text{Fm}^{-2}$ in the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 µm process. At a frequency of 450 MHz, the optimum width has a value of 1535 µm. In order to satisfy the small die area this large size transistor cannot be used when the maximum width of the CMOS process is 100 µm. Thus, the technique of calculating the optimum width of the driving transistor does not satisfy the design consideration at low frequency. Therefore, two MOS transistors, MN_1 and MN_2, with a maximum

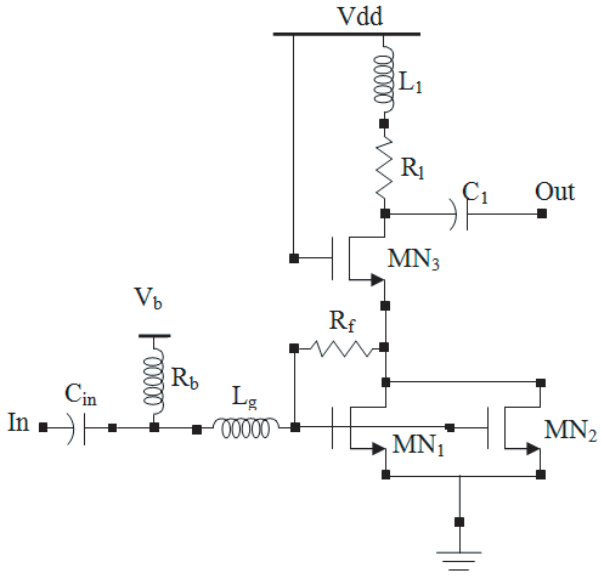

Figure 4. Circuit diagram of LNA.

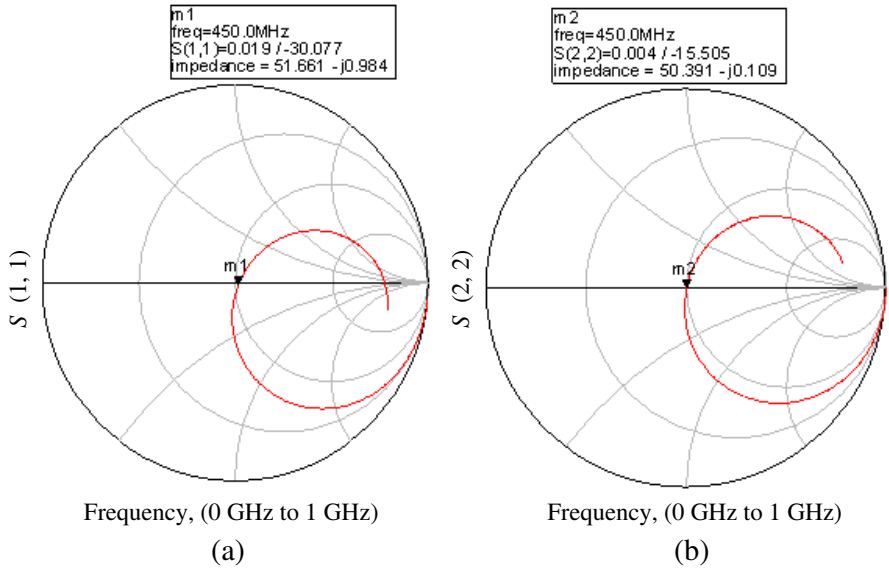

Figure 5. (a) Smith chart of input matching; (b) smith chart of output matching.

width of 100 µm are used in parallel to trade-off among noise, gain, and power consumption. The cascading transistor MN_3 was used to improve the reverse isolation and to increase the gain. After the cascading and driving transistors were modelled, the next task was to design the input-output matching network. The input matching network requires that the input impedance of the LNA at the desired frequency be the most common value, i.e., 50 Ω, for matching with the antenna. The input impedance of this LNA is given by:

$$Z_{in} = \frac{1}{sC_{in}} + \left(sL_b || \left(sL_g + \frac{1}{sC_{gs}} \right) \right) + \frac{g_m}{C_{gs}}, \tag{3}$$

where $C_{gs} = C_{gs,\,\mathrm{MN}_1} || C_{gs,\,\mathrm{MN}_2}$, and g_m is the combined transconductance of transistors MN_1 and MN_2. Usually, the design of the wide-band input or output matching network is more complex than the design of the narrow-band matching network because the latter can be done using simple, passive elements [22]. It is common practice to use an additional parallel resonance circuit to enhance the bandwidth of the matching network. In this design, a parallel feedback resistor R_f is used instead of a resonance circuit because the low frequency of the latter requires a higher value of passive elements, which increases the size of the chip. The inductive shunt-peaking technique is used

for output matching, where the load is tuned to 450 MHz by adjusting the value of L_1 and C_1, and the bandwidth is enhanced to more than 100 MHz by the small resistor R_l.

Table 2. Optimum component size (parameter value) of LNA.

Parameter	Value
MN_1, MN_2, MN_3	100/0.18 µm
L_1	35 nH
R_l	16 ohm
C_1	3.5 pF
R_f	2000 ohm
L_g	4 nH
L_b	35 nH
C_{in}	3 pF

The optimum values of the active and passive elements of the LNA are shown in Table 2. Figure 5 shows that the input and output of the LNA matched very closely to 50 Ω at 450 MHz.

3.4. Logarithmic Amplifier Design

In most of the cases, the RF receiver must handle a large, dynamic range of input signals. Thus, it is common practice to use an automatic gain control (AGC) circuit to achieve a sufficiently dynamic range. The logarithmic amplifier (LA) is an effective alternative to the AGC circuit; the logarithmic amplifier refers to an amplifier for which "the gain must be linear until a certain level of the input signal is reached, after which the gain must be unity" [23]. The most important advantages of the LA are that it can assist in separating unwanted signals from the desired signal and that can be operated with low DC power [24].

The problem of phase equalization in an LA can be solved by using a cascoding amplifier that consists of dual gain stages. If it is required, cascading N identical LA blocks (with each of the LA blocks having a dual-gain stage) to achieve the desire dynamic range, the output voltage of the nth block can be expressed by the relation given in [24].

$$V_o = \left\{ n + \frac{1}{A_v} + \log_{(A_v+1)} \left[\frac{A_v V_{in}}{V_L} \right] \right\} V_L, \tag{4}$$

where A_v is the small signal gain of LA amplifier, V_L is the limiting voltage, and V_{in} is the input voltage.

The output signal from the LNA is passed to the LA as shown in Figure 6. The dual-gain stage is used in each LA block, and three LA blocks are cascaded to achieve a sufficient dynamic range. The three LA blocks that are used are identical, as is the transistor size (MP_1 to MP_8 and MN_4 to MN_{15}) in each gain stage. The amplified signal is rectified using two shunt capacitors, C_2 and C_3. The rectified output at capacitor C_2 indicates the voltage level of the received signal, and this voltage is compared with the reference voltage in the comparator circuit to determine the digital logic level of the received signal. The sizes of the transistors and other components are listed in Table 3.

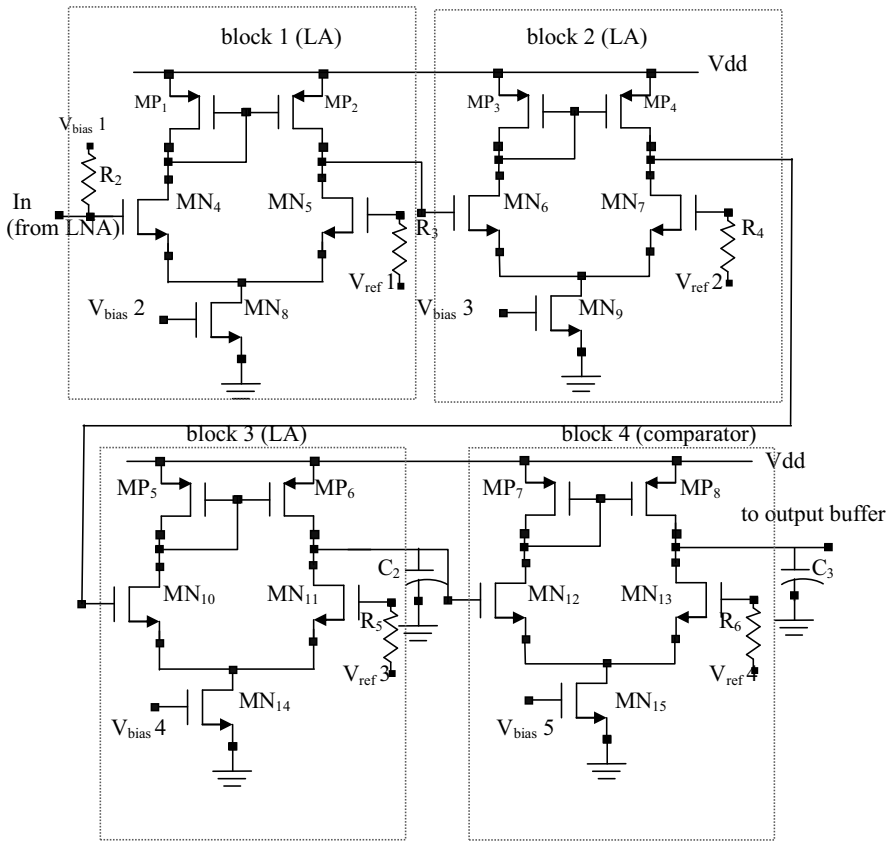

Figure 6. Logarithmic amplifier, power detector, and comparator.

Table 3. Sizes of the components in the circuit shown in Figure 6.

Parameter	Value
R_2, R_3, R_4, R_5, R_6	500 Ω
C_2, C_3	1 pF
$V_{ref}1$ to $V_{ref}4$	0.6 V
$V_{bias}1$	0.6 V
$V_{bias}2$ to $V_{bias}3$	1.5 V
MP_1	2.5/0.18 µm
MP_2, MP_3	1.5/0.18 µm
MP_4, MP_5	2/0.18 µm
MP_6	4/0.18 µm
MP_7, MP_8	1/0.18 µm
MN_4	15/0.18 µm
MN_5	9/0.18 µm
MN_6	12/0.18 µm
MN_7	14/0.18 µm
MN_{10}	5/0.18 µm
MN_{11}	10/0.18 µm
MN_{12}, MN_{13}	2/0.18 µm
MN_8, MN_9, MN_{14}, MN_{15}	1/0.18 µm

4. RESULTS AND DISCUSSION

4.1. LNA Simulation Results

The simulated results of inductive, degeneration, cascode, feedback LNA are presented and discussed in this section. The LNA was simulated with a DC power supply of 1.5 V, and the entire LNA circuit drew 17 mA of current from the DC source. Figure 7 shows the input and output reflection losses of the LNA, S_{11}, and S_{22}, respectively. The inductive source degeneration technique is good for narrow-band matching. A 2000-ohm parallel shunt resistor, R_f, and a 15-ohm resistor, R_l, were connected in series with the load inductor, and they were chosen to have 100-MHz input and output matching bandwidths at the −10 dB level. Both the input and output matching had reflection losses less than −30 dB, which ensured that the higher power was transferred from the antenna to LNA and from LNA to the

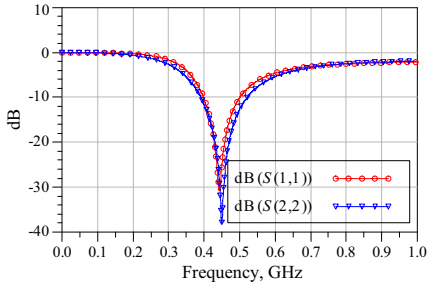

Figure 7. Simulated reflection loss of input matching (S_{11}) and output matching (S_{22}).

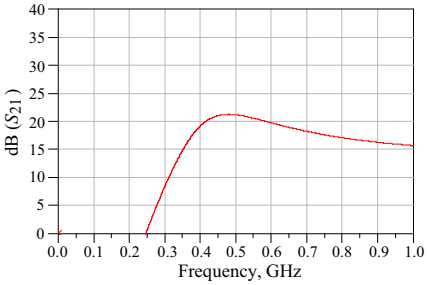

Figure 8. Simulated forward gain of the LNA.

post amplifier section, respectively. The LNA had a forward gain that was greater than 21 dB (Figure 8). Over the operating bandwidth of 400 to 500 MHz, the gain varied from a maximum value of 21.2 dB to a minimum value of 19.2 dB. The flatness of the gain within 2 dB indicated the stability of the amplification in the operating frequency band. The forward and reverse gains are compared in Figure 9. There is a 65-dB difference between forward and reverse gain, which created very strong reverse isolation. The simulated NF is shown in Figure 10. The LNA achieved the minimum NF of 0.55 dB at a frequency of 450 MHz. The maximum NF in the operating band was 1.1 dB at a frequency of 400 MHz. The NF between 1.2 dB and 0.55 dB proved that the LNA was able to reduce the noise. In the simulation, the input power of the LNA ranged from −80 to 0 dBm, and the linearity of the data in this range indicated that the LNA amplified the input signal linearly until the input power was ≤ -30 dBm (Figure 11). Overall, the results showed that the LNA had acceptable performance characteristics for this specific application.

4.2. Logarithmic Amplifier

In order to compensate for the high attenuation loss in the received signal, the signal was amplified by the LNA and then passed through the LA. To reach the desired gain, three blocks (with each block having a dual-gain stage) of the LA were used in a cascade structure. The transistors used in each gain stage were sized to achieve a gain of 21 dB by each block, producing a total gain of 63 dB. Figure 12 represents the gain characteristics of the LA's first, second, and third blocks by 'LAout1', 'LAout2', and 'LAout3', respectively. From Figure 12, it is clear that the output of LA block 3, i.e., 'LAout3', is $>$ 0 dBm

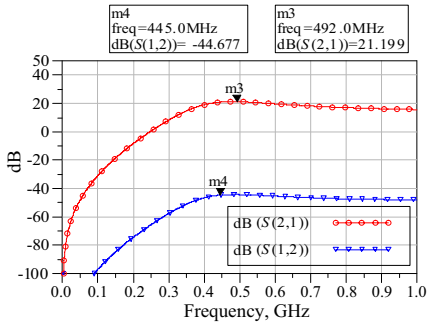

Figure 9. Input-output isolation of the LNA in terms of forward and backward gain.

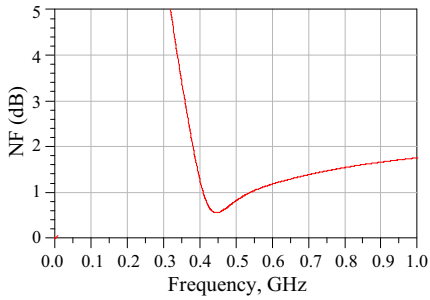

Figure 10. Noise figure of the LNA.

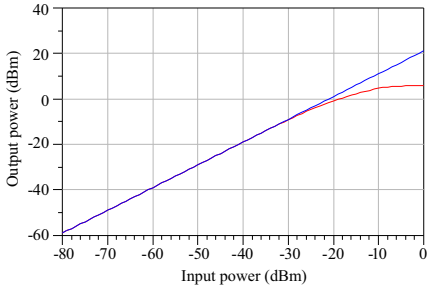

Figure 11. One-dB compression point (IP1) of the LNA.

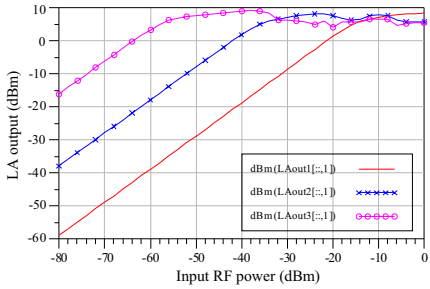

Figure 12. Gain characteristics of the logarithmic amplifier (LA) at the outputs of the different stages.

during the range of input signal from around −63 dBm to 0 dBm, which indicated that the three cascaded blocks of the LA accumulated a total dynamic range of 63 dB. In the receiving path, the LNA and LA in combination provided a resultant gain of about 80 dB, which made the comparator circuit able to detect the '1' bit from a weak signal up to −80 dBm.

4.2.1. Detector and Comparator

The amplified signal was rectified by capacitors C_2 and C_3, and the DC levels were compared to determine whether the received signal was bit '1' or '0'. Figure 13 shows the first-stage signal rectified by capacitor C_2, which is the input feed to the comparator. The input RF power

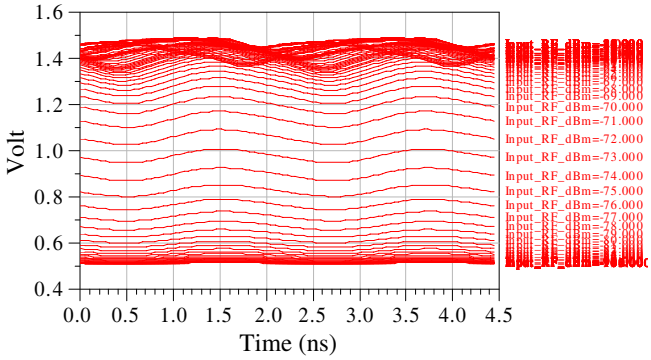

Figure 13. Level of the DC voltage of the rectified signal from LA3 corresponding to input signals ranging from −100 to 0 dBm.

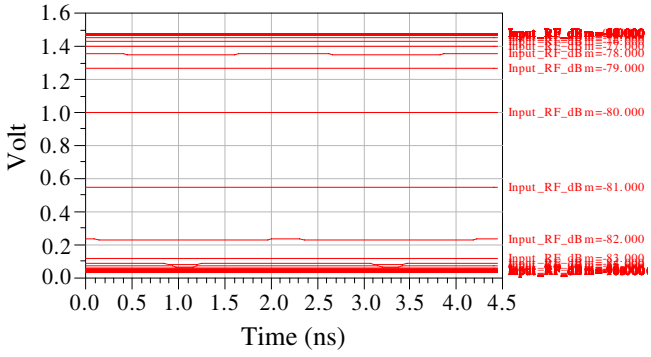

Figure 14. Comparator output over the dynamic range of the input signal.

covered the range from −100 to 0 dBm, which resulted in the rectified DC voltage varying from around 0.5 V to1.5 V. The corresponding rectified DC level for −80 dBm input RF power was fixed at around 0.6 V.

In the comparator circuit, the 0.6-V DC level was considered as the reference voltage; above this level, the rectified output was shifted to DC $\sim$ 1.5 V (bit '1'), and, below this level, the rectified output was shifted to DC $\sim$ 0 V (bit '0'). The output capacitor C_3 sharpened the DC level. The rectified output of comparator is shown in Figure 14, and the final input-output characteristics of the receiver are shown in Figure 15.

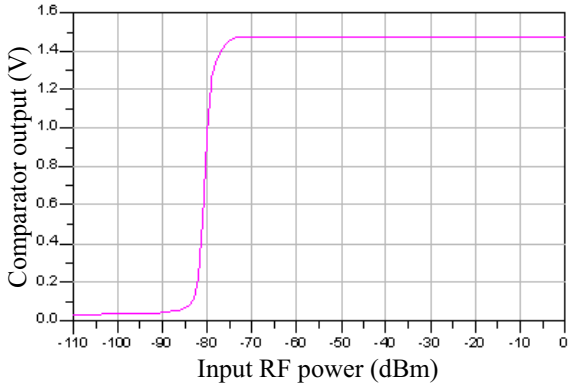

Figure 15. Received input power vs receiver's output voltage.

5. CONCLUSIONS

A high-speed, highly-simplified, direct analog RF-to-digital conversion receiver for WCE is presented in this paper. Unlike the architecture of a conventional receiver, the entire receiving path was implemented with basic blocks that included the LNA, a logarithmic amplifier, a power-level detector,and a comparator. This simplified architecture eliminated the requirement for a local oscillator and mixer. The receiver circuit diagram was designed and simulated with the TSMC 0.18-µm CMOS process in Advanced Design System (ADS). Taking into consideration the trade-off between path loss and antenna design complexity, the receiver circuit was designed at a frequency of 450 MHz and a bandwidth of 100 MHz. The LNA and the cascoded three blocks of LA provided a total gain of 80 dB, which enabled the receiver system to sense incoming, weak RF signals as low as −80 dBm, and it can support a data rate of 100 Mbps. The entire system consumed only 26 mW of power from a 1.5-DC supply. The proposed receiver is highly suited for receiving the data associated with the high-resolution image requirements in WCE applications.

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