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A 23-GHz BANDWIDTH AUTOMATIC GAIN CONTROL AMPLIFIER WITH WIDE DYNAMIC RANGE FOR HIGH SPEED COMMUNICATION

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Abstract—In this paper, a wide bandwidth and wide dynamic range AGC amplifier is presented. A push-pull variable gain amplifier (VGA) structure is proposed for wide dynamic rang. Moreover, the bandwidth enhancement technique is used in the post amplifier design to ensure the wide bandwidth and gain of whole circuit. The experimental results demonstrate that the proposed AGC amplifier fabricated in 0.13 µm SiGe BiCMOS process, achieves a 23-GHz bandwidth and 36-dB dynamic rang whereas the power and area consumption are 57.6 mW and 1.9 mm^2, respectively.

1. INTRODUCTION

The rapid growth in data communication and multimedia applications has been driving research on millimeter-wave frequency band high speed communication, such as 60-GHz radio system and over 100-GHz millimeter wave communication system [1–7]. In order to provide high

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enough data rate with smaller equipment size and lower price, the demand for high speed integrated circuits (ICs) operating at tens of Gbps remains unremitting. Traditionally, these high speed circuits are mainly designed in III-V compound semiconductor technologies [5–7]. The III-V compound semiconductor is assumed a good candidate for high frequency operation. However, due to its incompatibility with commonly used low-cost CMOS intermediate frequency or base-band circuit and high fabrication cost, the III-V compound semiconductor is not the best choice for integrated system-on-chip (SoC) circuit design. Among the technologies for high-speed circuits, the SiGe HBT, in fact, becomes a favorable candidate due to its compatibility with CMOS base-band circuits and of course, its good high frequency performance.

At the receiving end, the signal can vary over a wide range. In order to sustain the operation of the subsequent baseband circuits, weak signal has to be amplified and an overly-large signal must be depressed. To fulfill the requirement, an AGC amplifier is necessary in high speed communication systems , due to its advantage of noise and jitter compared to a limiting amplifier (LA) [8–13]. Wide bandwidth and dynamic range are the most important considerations in AGC amplifier design of high speed receiver. Recently, a 10 Gbps AGC amplifier that offers a 35-dB dynamic range is demonstrated in 0.18 μm CMOS technology [14]. However, the bandwidth of the circuit is still insufficient for modern high speed communication. A 40 Gbps AGC amplifier has also been fabricated in 90-nm CMOS technology [15] but its performance is still inadequate in some applications. To achieve an AGC with wide dynamic range, the requirement of wide bandwidth and high gain is thus a tall order for modern wireless and optical high speed communications.

This paper presents a new VGA structure to achieve a wide dynamic range with higher gain. Using the proposed VGA core, the AGC amplifier is able to realize wider dynamic range with higher gain and lower power consumption. In addition, the bandwidth enhancement and multi-stage peak detection techniques are both employed to extend the bandwidth. The circuit, occupying an area of 1.9 mm^2, is fabricated in 0.13 μm SiGe BiCMOS technology.

2. AGC AMPLIFIER ARCHITECTURE

2.1. Push-pull Variable Gain Amplifier

The architecture of the AGC amplifier is shown in Fig. 1. In AGC amplifier design, the VGA plays a very important role. Almost all popularly used VGAs for high speed data transmission developed from the differential pair and control their gain through varying the tail

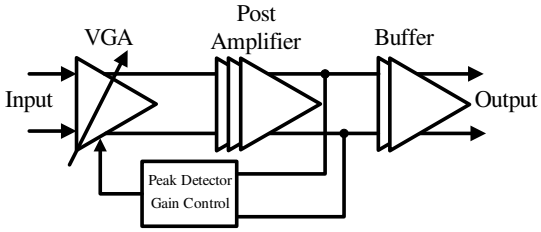

Figure 1. Architecture of the AGC amplifier.

current source. This approach raises some concerns, such as the narrow gain control range and limitation of dynamic range of whole AGC circuit. In order to solve these issues, a new control scheme variable gain amplifier is proposed in this work and the architecture of the proposed VGA is provided in Fig. 2.

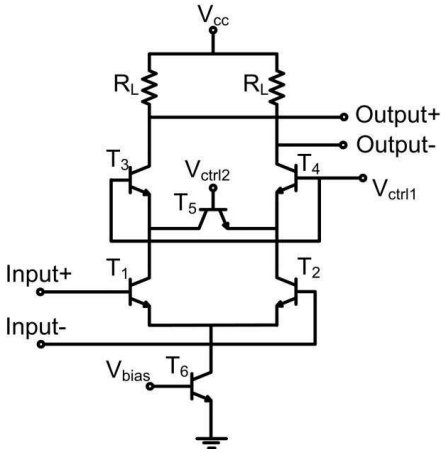

Figure 2. Architecture of proposed push-pull VGA.

From Fig. 2, it can be seen that the input signal is applied to the transistor pair T_1 and T_2, and the gain control signal is connected to transistors T_3, T_4 and T_5. The Compared with the conventional Gilbert Cell-based VGA, an additional transistor T_5 is used to control the gain of the circuit. In previous designs, the common emitter pair is often used to control the gain. However, the dynamic range of the amplifier will be impacted when the bias of common emitter pair is altered. In this work, when the input signal is applied to the input ports, the bias of the common emitter pair (T_1 and T_2) is maintained

to ensure a constant current source, and the gain is controlled by the additional transistor, T_5 and the common base pair, T_3 and T_4. When V_{ctrl1} is set to low level, the transistor T_3 and T_4 will operate at cut-off region. If V_{ctrl1} is set to high level, the transistor of T_3 and T_4 will operate at forward-active region. On the other hand, when V_{ctrl2} is set to low level, the transistor T_5 also operates at cut-off region, while it will operates at forward-active region when V_{ctrl2} is set to high level. In proposed circuit, the dynamic range of VGA is mostly dependent on the common emitter pair which is kept a constant bias source, so the dynamic range cannot be degraded when the gain of the whole VGA is varying. In addition, the adjustment time of the whole circuit is saved due to the push-pull structure. As a trade-off among power gain, dynamic range and linearity, T_1 and T_2 are chosen as 084_4 transistor, meanwhile T_3, T_4 and T_5 are chosen as 048_4 transistor. In addition, the load resistor R_L is set to 150 ohm.

In order to elucidate the working principle of our proposed VGA, the simplified half-circuit of proposed VGA core is illustrated in Fig. 3. It can be seen that the input signal is applied to transistor T_1, and the output current is divided through transistors T_2 and T_3. Hence, the output current which goes through transistor T_2 can be calculated as follow:

$$I_{o2} = g_{m1} V_{IN} \frac{1}{1 + g_{m3}/g_{m2}} \tag{1}$$

where g_{m1}, g_{m2} and g_{m3} are the transconductances of transistors T_1,

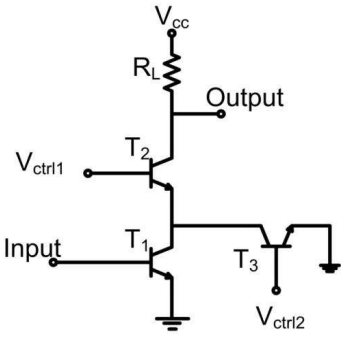

Figure 3. Simplified half-circuit of proposed VGA core.

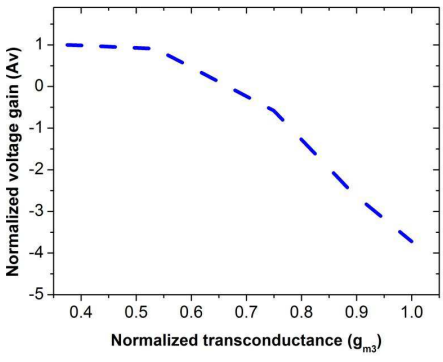

Figure 4. Voltage gain of simplified half-circuit of proposed VGA versus g_{m3}.

T_2 and T_3. The voltage gain of the VGA can be expressed as:

$$A_V = \left|\frac{V_{out}}{V_{in}}\right| = \frac{g_{m1}R_L}{1 + g_{m3}/g_{m2}} \tag{2}$$

where R_L is the output load resistor. From the above equations, it is clear that the increase of transconductance, g_{m1} and g_{m2} will lead to an enhancement of the gain of the whole circuit. On the other hand, if g_{m3} is raised, the gain of whole circuit will drop. The transconductances of the transistors are controlled by both V_{ctrl1} and V_{ctrl2}. If V_{ctrl1} is made larger, transconductance g_{m2} will increase and V_{ctrl2} will decrease accordingly to lower transconductance g_{m3}. So the gain of whole VGA increases quickly while g_{m1} is maintained at a constant value. The voltage gain of simplified half-circuit of proposed VGA versus g_{m3} is shown in Fig. 4. In VGA design, the dynamic range of the whole amplifier depends mostly on transistor T_1. In proposed design, g_{m1} is kept at a constant and both g_{m2} and g_{m3} are used to control the gain of whole amplifier. So by using this new push-pull VGA structure, the circuit gain can quickly be varied with wider gain control range and no degradation of the dynamic range.

2.2. Broadband Post Amplifier

In order to obtain sufficient gain, the VGA core is assisted by a three-stage post amplifier. Since the bandwidth of the entire circuit is expected to be very wide to provide enough high data rate, the bandwidth of post amplifier must fulfill the requirement of gain and bandwidth. In conventional amplifier design, the bandwidth is mainly determined by the RC time constants of every node. To enhance the bandwidth of the post amplifiers, the series inductor technique is added between stages.

The schematic diagram of our proposed post amplifier and also the small-signal equivalent circuit of the amplifier with series inductor are shown in Fig. 5 and Fig. 6. The L is deployed inductor, C_1 and C_2 are the equivalent capacitance by previous stage and next stage, R_1 and R_2 are the equivalent resistance by previous stage and next stage. The transfer function of the proposed amplifier is calculated in Equation (3). It is noted that the inductor and parasitic capacitances construct a third-order LC-ladder which could extend the bandwidth of whole amplifier. The 3-dB bandwidth of the proposed amplifier could be obviously extended as compare to conventional amplifier structure by adding the series inductor between stages [16], especially for the multistage cascaded structure. As a trade-off of bandwidth, power gain and stability, T_1 and T_2 are chosen as 084_4 transistor, meanwhile

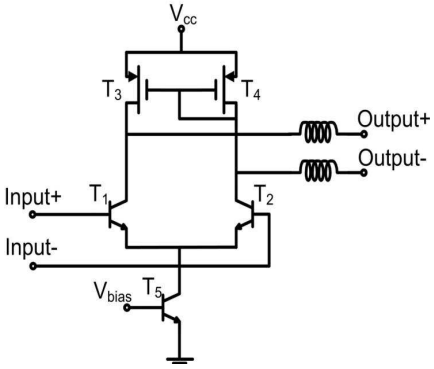

Figure 5. One stage of post amplifier.

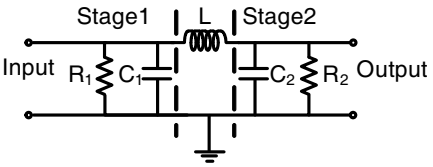

Figure 6. Equivalent inter-stage small signal modal of post amplifier.

the inductor is set to 0.25 nH and 0.45 nH for different stages.

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}R_1R_2}{R_1 + R_2 + s\left[R_1R_2(C_1 + C_2) + L\right] + s^2R_1R_2L\left[\frac{C_2}{R_1} + \frac{C_1}{R_2}\right] + s^3R_1R_2C_1C_2L} \tag{3}$$

2.3. Peak Detector and Control Voltage Generation

In AGC amplifier design, another important circuit is the peak detector, which will be used for generating the control voltage and then control the gain of whole circuit [17]. The detector of our proposed AGC amplifier is realized through a two-stage peaking detector circuit and the schematic is as shown in Fig. 7. T_1, T_2, T_8 and T_9 are chosen as 084_4 transistor, meanwhile T_{15} is chosen as 048_4 transistor. In addition, R is set to 200 ohm and C_1, C_2 are set to 15 pF, respectively.

The input signal V_{in} is applied to transistor T_1, and when V_{in} exceeds the peak voltage V_{peak}, transistor T_1 is switched on. The current that follows is copied by the current mirror, T_5 and T_6, to charge the holding capacitor C_1. On the other hand, when the input signal V_{in} is below V_{peak}, transistor T_1 is switched off and the capacitor C_1 holds the peak voltage. In our VGA design, the push-pull control voltage is used for extending the controlling range and increasing the adjusting speed. Hence, two control voltages must be generated by the detector design. Based on the above requirements, transistor T_{15} is added alongside the output holding capacitor. At the output of transistor T_{15}, the phase-opposite control voltages V_{pd1} and V_{pd2} to the

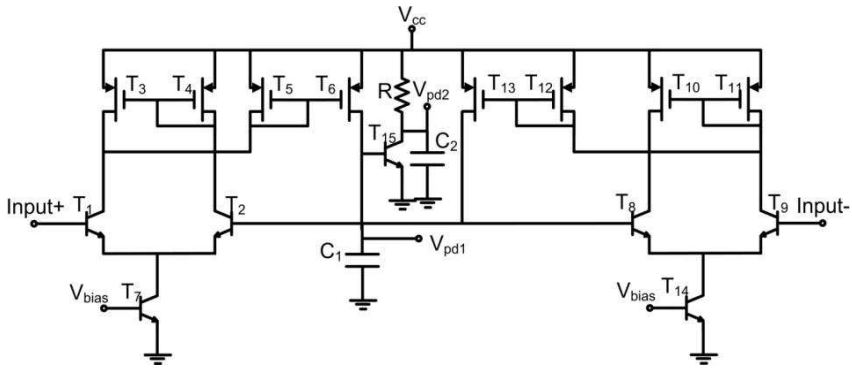

Figure 7. Architecture of peaking detector and control voltages V_{pd1} and V_{pd2} generation circuit.

peak voltage V_{peak} is generated. The push-pull control voltage can be derived as follows:

$$V_{ctrl1} = k\left(\frac{V_{ref}}{V_{pd1}}\right) \tag{4}$$

$$V_{ctrl2} = k\left(\frac{V_{ref}}{V_{pd2}}\right) \tag{5}$$

$$V_{pd2} = V_{ref} - V_{pd1} \tag{6}$$

where k is a constant coefficient and V_{ref} a reference voltage, which is related to the output power and independent of the input voltage. In addition, to obtain a constant settling time, a log amplifier is used for generating the control voltage [11]. Because of the BiCMOS process employed, the log amplifier can easily be constructed using BJT transistors.

Finally, in order to drive the output with a 50-Ω load, a two-stage output buffer is employed. The output buffer is realized using the differential configuration with active load, and the bandwidth enhancement technique is also employed to extend the bandwidth.

3. RESULTS AND DISCUSSION

The whole AGC amplifier is designed and fabricated in 0.13 µm SiGe HBT BiCMOS technology with an f_T of 200-GHz and f_{MAX} of 250-GHz. The fabricated chip microphotography is given in Fig. 8. The size of the whole switch modulator, which includes the test pads, is 830 µm × 2300 µm.

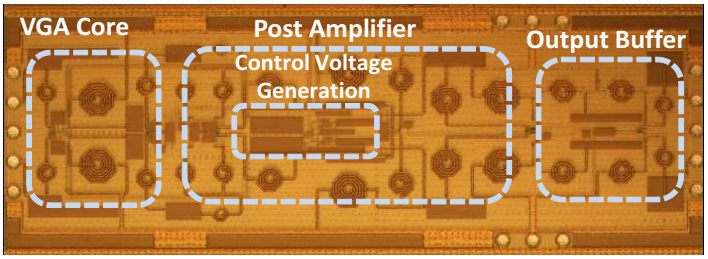

Figure 8. Microphotography of AGC amplifier.

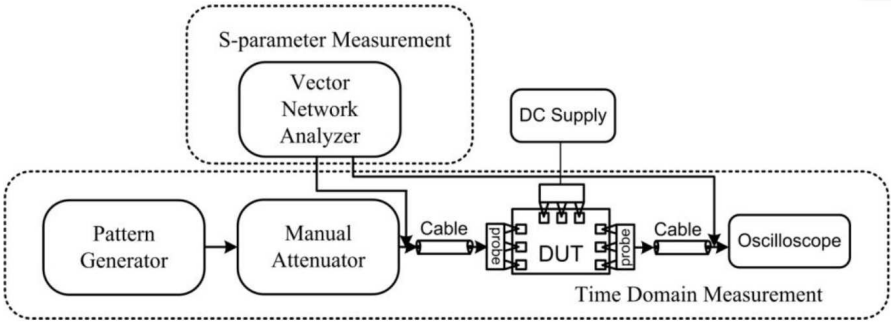

Figure 9. Measurement setup.

The experimental setup shown in Fig. 9 is used to measure the S-parameter and time-domain response of whole AGC amplifier. The equipment for on-chip measurement consists of signal generator, tunable attenuator, oscilloscope and vector network analyzer. The input signal of time domain measurement comes from the pattern generator and a continuous tunable attenuator connected by coaxial cable and ground-signal-ground (GSG) probe. The power level of input signal can be controlled by the attenuator and calibrated through a power meter. As a drawback, the attenuator will introduces some distortions and noises, which impact the input signal of device-under-test (DUT). The measurement equipments are calibrated by using line-reflect-reflect-match (LRRM) calibration with a ceramic standard substrate to compensate the impacts of connection components and probes and then make the reference plane to the probe tip.

The simulated and measured gain versus frequency characteristics under different input power level is presented in Fig. 10. From the figure, it can be seen that the 3-dB bandwidth of the proposed AGC amplifier is about 23-GHz, which can be used for over 30 Gb/s

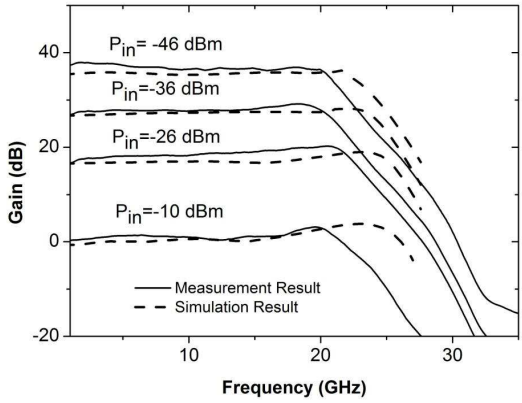

Figure 10. Measured and simulated gain versus frequency under different input power levels.

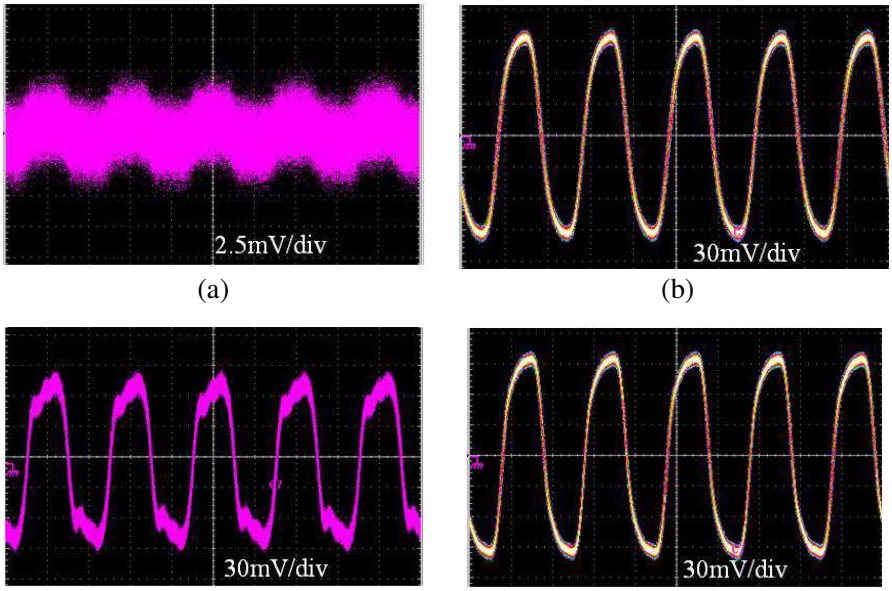

Figure 11. The input and output signal of AGC amplifier under different input power level with 10 Gbps data rate, (a) input signal at −46 dBm, (b) output signal at −46 dBm, (c) input signal at −10 dBm, (d) output signal at −10 dBm.

signal transmission. The differences between measurement results and simulation results at high frequency due to the capacitive parasitic effect of the layout and test pad. The gain of whole AGC amplifier is automatically adjusted to achieve a constant output voltage of 200 mVpp while the input power level is swept from −46 dBm to −10 dBm. The maximum gain of the AGC amplifier is 36-dB. In addition, all the gain curves derived for different input signals are also noted to be very smooth. The fluctuation in the bandwidth is smaller than 1 dB and this is very important for high speed signal transmission. The measured dynamic range of the whole AGC amplifier is about 36 dB. The entire circuit draws 32 mA current from the 1.8 V supply voltage.

The time domain response is measured up to 10 Gbps, which is limited by the measurement equipment. The input and output signal diagram of AGC amplifier at different input power level with 10 Gbps data rate is shown in Fig. 11. The input swing is swept from 3.2 mVpp to 200 mVpp. Accordingly, the power level is swept from −46 dBm to −10 dBm at 50 Ω. The different power level input signal is generated by the pattern generator and attenuator. It is noted that due to the unexpected impacts of attenuator, the input signal is not very good. However, after the processing of proposed AGC amplifier, the output signals achieve same size and very clear curve. Fig. 12 shows the measured output eye pattern for 10 Gbps input. The signal generator is used to generate the input pulse of 2^{31}-1 pseudorandom bitstream. The measurement is performed in single end mode and the other input/output ends are terminated by a 50-Ω resistor. From the figure, a well-opened eye pattern is obtained. The peak-to-peak jitter is lower than 7 ps. The VGA is observed to yield

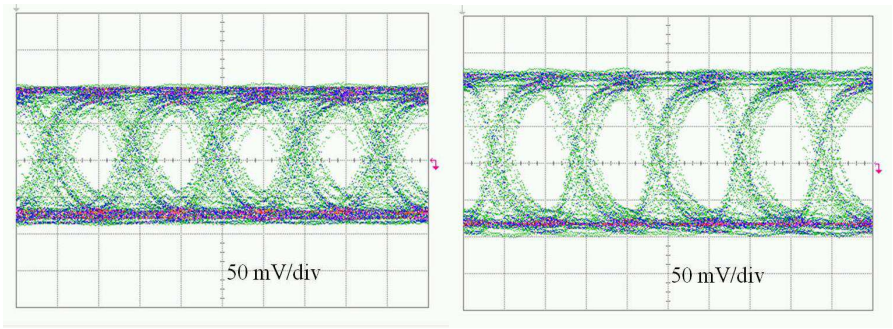

Figure 12. Single-ended eye-diagram of AGC output under different input power level with 10 Gbps data rate, (a) −46 dBm, (b) −10 dBm.

Table 1. High-speed AGC amplifiers performance comparison.

Process	**Dynamic Range (dB)**	**Bandwidth (GHz)**	**Gain (dB)**	**P_{DC} (mW)**	**Peak-to-Peak Jitter (ps)**	**Area (mm^2)**	**Ref.**
Inp-InGaAs DHBT	43	50	17	627	-	-	[12]
0.13 µm SiGe	40	7.5	30	72	40	1	[13]
0.18 µm CMOS	35	10	21*	54	25	1.3	[14]
90 nm CMOS	19	22	28*	75	-	0.56	[15]
0.13 µm SiGe	**36**	**23**	**36**	**57.6**	**7**	**1.9**	**This work**

* Estimates from figures in the corresponding papers.

superior output waveforms when the input signal amplitude varies from 3.2 mVpp to 200 mVpp. From the simulation result, the settling time of proposed AGC amplifier is smaller than 0.2 µs, while most of previous reported works are larger than 1 µs. Finally, the main performance of the proposed AGC amplifier is summarized in Table 1 and compared with recently published high-speed AGC amplifiers.

4. CONCLUSIONS

An AGC amplifier for high speed communication system is designed. In order to achieve wider dynamic range, a new variable gain amplifier is proposed, and two opposite varying control voltages are deployed to obtain wider control range and the higher adjustment speed, which is desired in high speed communication. A post amplifier is needed to assure that the whole ACG circuit can acquire sufficient gain. The bandwidth enhancement technique is employed in the post amplifier design for wider bandwidth in the complete AGC amplifier. In order to generate the push-pull control voltage, the two peak voltages are generated using a peak detector circuit. Compared with recently published AGC amplifiers, a superior result has been demonstrated by the proposed AGC amplifier. This paves the way for tens of gigabits per second data rate communication.

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