Progress In Electromagnetics Research, Vol. 142, 701–719, 2013

EFFECTS OF THE INDUCTIVE PORT OF BLUMLEIN TRANSMISSION LINE ON THE REFLECTION AND TRANSMISSION CHARACTERISTICS OF ELECTROMAGNETIC WAVES

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Abstract—The Blumlein transmission line (BTL) has broad applications in pulse modulation, microwave technology and pulsed power technology. In this paper, a new theoretical method for variable reflection and transmission of electromagnetic waves at the inductive port of transmission line is put forward, in order to analyze the wave reflection characteristics of BTL at the inductive port formed by a saturated magnetic switch. At the inductive port, the variable reflection and transmission mechanisms of the voltage waves traveling through the BTL are analyzed in detail, and the inductive effects on the square voltage pulse of load formed by the BTL are also studied. Simulation and experimental results both demonstrated the proposed new theoretical method which shows great value on high-power microwave technology, high-power pulse forming, pulse shaping and modulation.

1. INTRODUCTION

Transmission line (TL) is an important device for guiding and propagating electromagnetic waves in a special band, and it has been widely used in communications [1, 2], pulse modulation and signal measurement [3–6], microwave technology [7–10] and pulsed power technology [11–15]. Every TL has its own characteristic impedance, and the impedance of a dispersive TL changes in line with the work frequency [15, 16]. A practical TL has a finite length so that the propagating electromagnetic wave reflects and transmits at the terminal ports of the TL [16–18]. The wave reflection and transmission

Received 8 August 2013, Accepted 28 September 2013, Scheduled 11 October 2013

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coefficients at the port of a common non-dispersive TL are only determined by the port impedances [13, 14]. However, the dispersive propagating theory of traveling waves reveals that those coefficients aforementioned are determined by the port impedances, dielectric characteristics and work frequency [16]. The common concerned wave reflection cases of the TL include 3 types such as wave reflection at the joint port of TL-TL [13], or at the joint port of TL-resistor [11], or at the joint ports of TL-resistor-TL [14].

In many applications, a switch is required to connect with the TL port [11–16], in order to control the propagating courses of the electromagnetic waves. The common-used switches include the trigger switch, semiconductor switch, spark gap switch [13, 14] and magnetic switch [11, 16]. When the switch is open, the TL port of the switch is also open with an infinitely large impedance. When the switch is closed, the switch port with an impedance of 0 is shorted out. The wave propagation in the common concerned cases aforementioned can be sufficiently analyzed only by the port impedances [13, 14]. However, the closed-switch port of TL is a non-ideal short-circuit port in practice due to the parasitic inductance of switch. Though the parasitic inductance of switch is small, it shows strong effects on the wave reflection characteristics at the closed-switch port (or the inductive port). As the inductive port is quite different form the common concerned TL port and resistive port, the traditional traveling wave propagation theory can not analyze and explain the wave reflection and transmission problems at the inductive port of TL [13, 14].

In this paper, a new theoretical method for variable reflection and transmission of electromagnetic waves at the inductive port of BTL is put forward, in the purpose of analyzing the wave reflection characteristics of a high-power BTL connected with a saturated magnetic switch. The effects of the inductive port on the traveling wave reflection, wave transmission and load voltage pulse formed by the BTL are studied in detail. The proposed method shows great value on high-power microwave technology and pulsed power technology.

2. REFLECTION THEORY OF TRAVELING WAVES AT THE INDUCTIVE PORT OF BTL

In the fields of microwave and pulsed power technology, pulse transformer is usually employed to charge the high power BTL; if a matched pulse switch acts in concert to the BTL, the BTL can generate and propagate high power electromagnetic waves in a special band. Under the mechanisms of traveling wave reflection, transmission and the vectorial superimposition of waves, a quasi-square voltage (current)

pulse can be formed on the load at the terminal port of the BTL. As a result, the BTL is an important technology for high-power square pulse generation, pulse shaping and modulation [15, 16].

Figure 1(a) shows the typical pulse modulation schematic based on a BTL and a saturable pulse transformer (SPT) [19, 20]. The BTL usually consists of two single transmission lines such as the inner line and the outer line with electrical lengths as τ_{in} and τ_{out} ($\tau_{in} = \tau_{out}$), and characteristic impedances as Z_{in} and Z_{out}, respectively. Firstly, the SPT is employed to charge the inner line and outer line simultaneously at Port B. In order to obtain a uniform charging effect on the BTL, a ground inductor L_{gnd} is connected in series on Port C of the inner line. L_{gnd} is in parallel with the load R_L. When the magnetic core of SPT saturates, the charging course of the BTL is over. The secondary windings of SPT, which is connected in series with Port B of the outer line, play as a saturated magnetic switch with the saturated inductance as $L_{ss}(t)$, and a passage between the charged outer line and the ground is established. High-frequency traveling current flows between the inner line and outer line which simultaneously generates electromagnetic waves traveling in the BTL. After the SPT saturates, the working frequency of the circuit shown in Fig. 1(a) is high enough, and the L_{gnd} branch approximately equates to an open circuit. As a result, the schematic shown in Fig. 1(a) equates to the one shown in Fig. 1(b). The traveling waves in the outer line reflect and transmit when they propagate to Port B; the reflection waves from Port B will transmit again after they propagate to Port D. Finally, a quasi-square voltage pulse on the load R_L is formed by the superimposed transmitting waves from Port D and Port C, and the formed pulse width is $2\tau_{out}$.

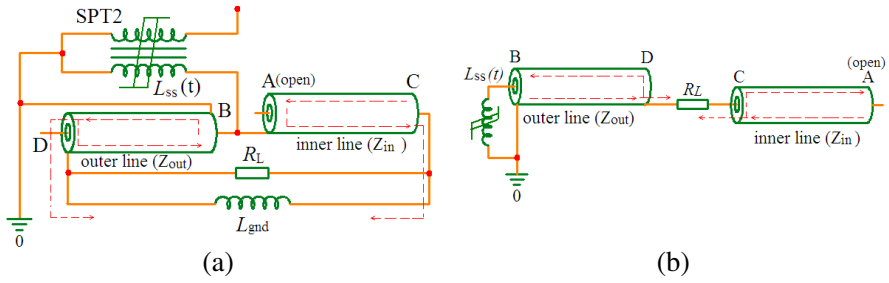

Figure 1. High-power square pulse modulation circuit based on the BTL; (a) The general pulse modulation schematic; (b) The equivalent schematic for wave propagation and pulse modulation after the SPT saturates.

If $L_{ss}(t)$ is lower than dozens of nH, Port B can be viewed as a short-circuit Port, and the outside impedance of Port B is about 0. Under the case that $L_{ss}(t) \approx 0$, important issues such as the traveling wave course in Fig. 1(b), load wave superimposing and load pulse formation characteristics can be analyzed by the traditional propagation theory of TL based on port impedances [13, 14]. However, $L_{ss}(t)$ can not be neglected in most of the applications, and the saturated inductance at Port B of the BTL shows strong effect on the traveling wave reflection, transmission and load voltage pulse formation. The traditional propagation theory of transmission line is not able to analyze the basic physical problems aforementioned, and new theory and method are urgently required.

Reference [16] shows that the reflection and transmission of traveling electromagnetic waves equate to the reflection and transmission of the flowing current waves or hypothetic voltage waves. The reflection and transmission coefficients of the inductive Port B are analyzed in detail as follows. Define the reflection coefficients of voltage waves at Port A, Port B, Port C and Port D as ξ_A, ξ_B, ξ_C and ξ_D, respectively; define the voltage transmission coefficients of Port B, Port C and Port D as α_B, α_C and α_D in order; the reflection and transmission coefficients of the current wave at Port B as ξ_{Bi} and α_{Bi}, respectively. The coefficients of the BTL mentioned above should be calculated by the electromagnetic dispersion propagation theory put forward in [16]:

$$\begin{cases} \xi_A = 1 \\ \alpha_A = 1 + \xi_A = 2 \end{cases}, \quad \begin{cases} \xi_C = \dfrac{R_L + Z_{out} - Z_{in}}{R_L + Z_{out} + Z_{in}} \\ \alpha_C(t) = 1 + \xi_C \end{cases}, \quad \begin{cases} \xi_D = \dfrac{R_L + Z_{in} - Z_{out}}{R_L + Z_{in} + Z_{out}} \\ \alpha_D(t) = 1 + \xi_D \end{cases}. \quad (1)$$

During the charging course of the BTL with charging voltage as $U_{CB}(t)$, a balance state of the traveling waves in the inner line and outer line of the BTL is achieved, and the voltage amplitude of the hypothetic voltage wave in a single direction in the inner or outer line is $U_{CB}(t)/2$. Define the formed pulse duration of the BTL as τ_{PFL} ($\tau_{PFL} = 2\tau_{out}$). When $t = t_s$, SPT saturates. During the stage that $t_s \le t \le t_s + \tau_{PFL}$, the amplitude of the incident voltage wave at Port B of the outer line is $U_{Br}(t) = U_{CB}(t_s)/2$; define the transmission current wave on the saturated inductor L_{ss} as $i_s(t)$, and the circuit equations of Port B and $L_{ss}(t)$ branch are established as

$$\begin{cases} U_{Br}(t)\alpha_{Bu}(t) = L_{ss}(t)di_s(t)/dt \\ i_s(t) = [U_{Br}(t)/Z_{out}]\alpha_{Bi}(t) \end{cases},$$
$$\begin{cases} \alpha_{Bu}(t) = 1 + \xi_{Bu}(t) \\ \alpha_{Bi}(t) = 1 + \xi_{Bi}(t) \end{cases}, \quad (t_s \le t \le t_s + \tau_{PFL}). \quad (2)$$

In the outer line, the reflection voltage wave and reflection current wave from Port B have the amplitude relation as $U_{CB}(t_s)\xi_{Bu}(t)/2 = U_{CB}(t_s)\xi_{Bi}(t)(-Z_{out})/(2Z_{out})$. As a result, $\xi_{Bi}(t) = -\xi_{Bu}(t)$. Through considering the initial condition $\xi_{Bu}(t_s) = 1$, the equations in (2) can be solved as

$$\begin{cases} \xi_{Bu}(t) = 2\exp\left[-\dfrac{Z_{out}}{L_{ss}(t)}(t-t_s)\right] - 1 \\ \alpha_{Bu}(t) = 1 + \xi_{Bu}(t) \end{cases}, \quad \begin{cases} \xi_{Bi}(t) = -\xi_{Bu}(t) \\ \alpha_{Bi}(t) = 1 - \xi_{Bu}(t) \end{cases},$$
$$(t_s \le t \le t_s + \tau_{PFL}). \quad (3)$$

In the case such as a transmission line to a resistor or another transmission line, the port reflection and transmission coefficients are constant as shown in (1). However, in the case that a transmission line to a saturated inductor, the port reflection and transmission coefficients shown in (3) are variable with time.

Since the time $t = t_s + \tau_{PFL}/2$, the reflection voltage wave from Port B when $t = t_s$ with amplitude of $U_{Bf}(t) = U_{Br}(t)\xi_{Bu}(t)$ reaches Port D, and the previous voltage balance state on the load is broken off. Load voltage pulse forming course starts, and both the transmitting waves from Port D and C form the load voltage pulse at Port C. Furthermore, the transmitting voltage wave of Port C and R_L branch superimposes with the reflection wave of Port D, which forms the incident voltage wave for Port B during the stage $t_s + \tau_{PFL} \le t \le t_s + 2\tau_{PFL}$:

$$U_{Br}(t) = \frac{U_{CB}(t_s)}{2}\left\{\left\{2\exp\left[-\frac{Z_{out}}{L_{ss}(t)}(t-t_s-\tau_{PFL})\right]-1\right\}\xi_D + \alpha_C\frac{Z_{out}}{R_L+Z_{out}}\right\},$$
$$(t_s + \tau_{PFL} \le t \le t_s + 2\tau_{PFL}). \quad (4)$$

As $U_{Br}(t)$ varies with time, the circuit equations in (2) at Port B require new solutions at this stage. Define a transition function F(t) as

$$F(t) = U_{Br}(t)\exp\left[\frac{Z_{out}}{L_{ss}(t)}(t-t_s-\tau_{PFL})\right] - U_{CB}(t_s)\left\{\frac{2\xi_D Z_{out}}{L_{ss}(t)}(t-t_s-\tau_{PFL}) + \left(\frac{\alpha_C Z_{out}}{R_L+Z_{out}} - \xi_D\right)\exp\left[\frac{Z_{out}}{L_{ss}(t)}(t-t_s-\tau_{PFL})\right],$$
$$(t_s + \tau_{PFL} \le t \le t_s + 2\tau_{PFL}). \quad (5)$$

The amplitude $U_{Br}(t)$ of the incident voltage wave at Port B, voltage reflection coefficient $\xi_{Bu}(t)$ and the amplitude $U_{Af}(t)$ of the

reflection voltage wave at Port A are extrapolated as

$$\begin{cases} U_{Br}(t)=\begin{cases} U_{CB}(t_s)/2, & t_s \le t \le t_s+\tau_{PFL} \\ \dfrac{U_{CB}(t_s)}{2}\left\{\left[2\exp\left(-\dfrac{Z_{out}}{L_s(t)}(t-t_s-\tau_{PFL})\right)-1\right]\xi_D \right. \\ \left. +\dfrac{\alpha_C Z_{out}}{R_L+Z_{out}}\right\}, & t_s+\tau_{PFL} \le t \le t_s+2\tau_{PFL} \end{cases} \\ \xi_{Bu}(t)=\begin{cases} 2\exp\left(-\dfrac{Z_{out}}{L_{ss}(t)}(t-t_s)\right)-1, & t_s \le t \le t_s+\tau_{PFL} \\ \dfrac{\left\{F(t)+U_{CB}(t_s)\left[\left(\xi_D+\alpha_C\dfrac{Z_{out}}{R_L+Z_{out}}\right)\right.\right.}{U_{Br}(t)} \\ \left.\left.\exp\left(-\dfrac{Z_{out}\tau_{PFL}}{L_{ss}(t)}\right)-2\xi_D\right]\right\} \\ \exp\left(-\dfrac{Z_{out}}{L_{ss}(t)}(t-t_s-\tau_{PFL})\right), & t_s+\tau_{PFL} \le t \le t_s+2\tau_{PFL} \end{cases} \\ U_{Af}(t)=\begin{cases} U_{CB}(t_s)/2, & t_s \le t \le t_s+\tau_{PFL} \\ \dfrac{U_{CB}(t_s)}{2}\left\{\left[2\exp\left(-\dfrac{Z_{out}}{L_{ss}(t)}(t-t_s-\tau_{PFL})\right)-1\right]\right. \\ \left.\dfrac{\alpha_D Z_{in}}{R_L+Z_{in}+\xi_C}\right\}, & t_s+\tau_{PFL} \le t \le t_s+2\tau_{PFL} \end{cases} \end{cases} \tag{6}$$

Of course, the aforementioned parameters in the stage that $t \ge (t_s + 2\tau_{PFL})$ can also be obtained by solving the Equation (2) again based on the iteration method. Finally, the voltage pulse $U_{RL}(t)$ and current pulse $i_{RL}(t)$ formed on the load R_L at Port C can be extrapolated as

$$\begin{cases} U_{RL}(t)=\begin{cases} 0, & (t_s \le t \le t_s+\tau_{PFL}/2) \\ U_{Br}(t-\tau_{PFL}/2)\xi_{Bu}(t-\tau_{PFL}/2) & \\ -U_{Af}(t-\tau_{PFL}/2), & (t \ge t_s+\tau_{PFL}/2) \end{cases} \\ i_{RL}(t) = U_{RL}(t)/R_L \end{cases} . \tag{7}$$

(7) presents the quasi-square voltage pulse (including the pulse tail oscillation) formed by the BTL through the saturated inductor $L_{ss}(t)$ in the stage that $t \ge t_s$. During the stage $(t_s + \tau_{PFL}/2) \le t \le (t_s + 3\tau_{PFL}/2)$, the main pulse on the load R_L is forming; if $R_L = Z_{in} + Z_{out}$ and $Z_{in} = Z_{out}$,

$$U_{RL}(t) = U_{CB}(t_s)\left\{\exp\left[-\frac{Z_{out}}{L_{ss}(t)}(t-t_s)\right]-1\right\}. \tag{8}$$

The polarity of the main pulse on load is reverse to the polarity of the BTL charging pulse $U_{CB}(t)$, and the characteristic time scale of the formed main pulse is as $t_{L/R} = L_{ss}(t)/Z_{out}$. Reference [21] gave two definitions on the rise time t_r of the main pulse: one, the interval between $U_{RL}(t) = 10\%U_{CB}(t_s)$ and $U_{RL}(t) = 90\%U_{CB}(t_s)$; the other, the interval between $U_{RL}(t) = 0$ and $U_{RL}(t) = 100\%U_{CB}(t_s)$. In view of that, t_r can be extrapolated as

$$t_r = \begin{cases} \begin{cases} 2.2L_{ss}(t)/Z_{out}, & (10\%U_{CB}(t_s) \sim 90\%U_{CB}(t_s)) \\ 5L_{ss}(t)/Z_{out}, & (0 \sim 100\%U_{CB}(t_s)) \end{cases}, \\ \qquad\qquad\qquad\qquad (5L_{ss}(t)/Z_{out} \le \tau_{PFL}) \\ \tau_{PFL}, \qquad\qquad\qquad\qquad (5L_{ss}(t)/Z_{out} > \tau_{PFL}) \end{cases}. \tag{9}$$

Obviously, t_r is determined by the impedance Z_{out} and the saturated inductance $L_{ss}(t)$ of the SPT. To a ideal switch of the BTL, $L_{ss}(t) \approx 0$ and the wave reflection at Port B is ideal short-circuit reflection ($\xi_{Bu}(t) = -1$). In this case, the formed load voltage pulse $U_{RL}(t)$ is a standard square pulse with $t_r = 0$, which corresponds to the ideal analytical model employed in [13, 14]. However, $L_{ss}(t)$ can not be 0 in practice, which causes the exponential waveform of $U_{RL}(t)$. If $L_{ss}(t)$ is so high that $t_{L/R} \gg \tau_{PFL}$, Port B can be viewed as a broad-sense open-circuit port and $\xi_{Bu}(t) \approx +1$ during the stage of main pulse forming on load. That's also the reason that Port B equates to an open-circuit port during the charging course of the BTL.

During the stage $t_s \le t \le (t_s + \tau_{PFL}/2)$, the energy efficiency η from the BTL to the main pulse formed on load is as

$$\eta = \frac{\int_{t_s+\tau_{PFL}}^{t_s+\frac{3\tau_{PFL}}{2}} U_{RL}(t)^2 dt}{R_L C_B (U_{CB}(t_s))^2/2}. \tag{10}$$

In (10), C_B is the parallel combination of the capacitances of the inner and outer line of the BTL. At Port B in Fig. 1(b), the current $i_s(t)$ flowing through $L_{ss}(t)$ and the withstand voltage $U_{CB}(t)$ of $L_{ss}(t)$ are extrapolated as

$$\begin{cases} i_s(t) = U_{Br}(t)[1 - \xi_{Bu}(t)]/Z_{out} \\ U_{CB}(t) = U_{Br}(t)[1 + \xi_{Bu}(t)] \end{cases}, \quad (t \ge t_s). \tag{11}$$

In other words, $i_s(t)$ and $U_{CB}(t)$ are the transmitting current wave and transmitting voltage wave at Port B, respectively.

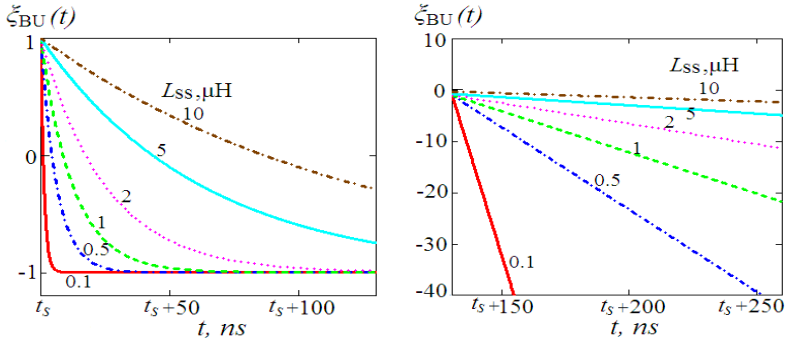

Figure 2. Theoretical calculation waveforms of $\xi_{Bu}(t)$ at inductive Port B during the stage $t_s \leq t \leq (t_s+2\tau_{PFL})$; (a) The waveform of $\xi_{Bu}(t)$ vs. t when $t_s \leq t \leq (t_s+\tau_{PFL})$; (b) The waveform of $\xi_{Bu}(t)$ vs. t when $(t_s+\tau_{PFL}) \leq t \leq (t_s+2\tau_{PFL})$.

3. WAVE REFLECTION CHARACTERISTICS AT INDUCTIVE PORT AND THE EFFECTS ON THE LOAD PULSE FORMING

3.1. Wave Propagation Characteristics at the Inductive Port

At the inductive port of the transmission line, the wave reflection and transmission coefficients are not constants again, but vary with time. Under the conditions such as $R_L = Z_{in} + Z_{out} = 160\,\Omega$, $Z_{in} = Z_{out} = 80\,\Omega$ and $\tau_{PFL} = 2\tau_{out} = 2\tau_{in} = 130\,\text{ns}$, the reflection coefficient $\xi_{Bu}(t)$ of the voltage wave at Port B during the stage $t_s \leq t \leq (t_s + 2\tau_{PFL})$ is presented in Fig. 2.

Figure 2(a) shows the effects of t and L_{ss} on $\xi_{Bu}(t)$, during the stage $t_s \leq t \leq (t_s + \tau_{PFL})$. When $t = t_s$, the SPT shown in Fig. 1(a) starts to saturate, $\xi_{Bu}(t) = 1$ and Port B still equates to an open circuit at this time. However, as t increases, $\xi_{Bu}(t)$ decreases from $+1$ to -1 in the exponential law, and the decreasing rate is completely determined by L_{ss}. According to the curves of $\xi_{Bu}(t)$ versus t as L_{ss} increases from $0.1\,\mu\text{H}$ to $10\,\mu\text{H}$, $\xi_{Bu}(t)$ can reach -1 if time is long enough. If L_{ss} is small, $\xi_{Bu}(t)$ decreases quickly. If L_{ss} is large while τ_{PFL} is short enough, $\xi_{Bu}(t)$ can not reach -1 during the stage $t_s \leq t \leq (t_s+\tau_{PFL})$, which is an important difference in contrast to the traditional theory on ideal switch ($\xi_{Bu}(t) \equiv -1$). When L_{ss} is large enough, $\xi_{Bu}(t)$ decreases so slowly that $\xi_{Bu}(t)$ almost remain unchanged during the stage $t_s \leq t \leq (t_s + \tau_{PFL})$. Therefore, the transmission line port

connected with large L_{ss} equates to an open circuit, $\xi_{Bu}(t) \approx +1$ and the voltage wave at this port has a total reflection.

During the stage $(t_s + \tau_{PFL}) \leq t \leq (t_s + 2\tau_{PFL})$, the effects of t and L_{ss} on $\xi_{Bu}(t)$ are shown in Fig. 2(b), in which $\xi_{Bu}(t)$ is normalized by the variable $U_{Br}(t)$ shown in (6). $\xi_{Bu}(t)$ decreases again as t increases, and larger L_{ss} corresponds to a smaller decreasing rate of $\xi_{Bu}(t)$. During this stage, $\xi_{Bu}(t)$ mainly affects on the main pulse tail and the first sub-pulse on load. In view of the conditions such as $\xi_{Bi}(t) = -\xi_{Bu}(t)$, $\alpha_{Bi}(t) = 1 + \xi_{Bi}(t)$ and $\alpha_{Bu}(t) = 1 + \xi_{Bu}(t)$, $\xi_{Bi}(t)$ and $\alpha_{Bi}(t)$ both have reversed changes in contrast to the changing law of $\xi_{Bu}(t)$, while $\alpha_{Bu}(t)$ shares the same changing law of $\xi_{Bu}(t)$.

Define the charge voltage of the BTL as $U_{CB}(t_s)$ when $t = t_s$. If $U_{CB}(t)$ and $i_s(t)$ shown in (11) are normalized by $U_{CB}(t_s)$, the normalized voltage $U_{CB0}(t)$ and current $i_{s0}(t)$ on $L_{ss}(t)$ at Port B are obtained as shown in Figs. 3(a) and 3(b), under the conditions of $R_L = Z_{in} + Z_{out} = 160\,\Omega$, $Z_{in} = Z_{out} = 80\,\Omega$ and $L_{ss}(t) = 500\,\text{nH}$. During the stage $t > t_s$, $U_{CB0}(t)$ decreases to 0 in the same exponential law as $\xi_{Bu}(t)$ at Port B, when t increases; actually, the voltage wave transmitting coefficient $\alpha_{Bu}(t) = 2U_{CB0}(t)$, at Port B. $i_s(t)$ is a quasi-square pulse with pulse width of τ_{PFL}. The pulse front edge of $i_s(t)$ also conforms the same exponential law as $\xi_{Bu}(t)$ shows, and the amplitude of $i_s(t)$ is twice as that of the load current pulse $i_{RL}(t)$.

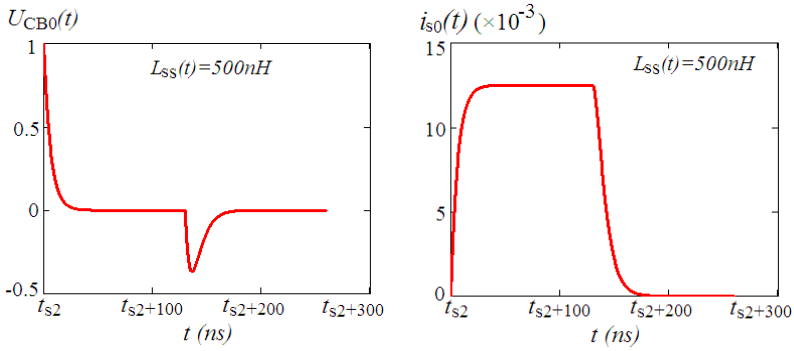

Figure 3. Theoretical calculation waveforms of the normalized voltage $U_{CB0}(t)$ and current $i_{s0}(t)$ on $L_{ss}(t)$ when $t \geq t_s$; (a) The waveform that $U_{CB0}(t)$ vs. t; (b) The waveform that $i_{s0}(t)$ vs. t.

3.2. Effects of Wave Reflection at Inductive Port on the Load Pulse Forming

Firstly, the impedance matching case of the BTL is analyzed ($Z_{in} = Z_{out}$, $R_L = Z_{in} + Z_{out}$). Set the BTL parameters as follows: $Z_{out} = 80\,\Omega$, and $\tau_{PFL} = 2\tau_{out} = 2\tau_{in} = 130\,\text{ns}$. The formed load voltage pulse $U_{RL}(t)$ shown in (7) is normalized by $U_{CB}(t_s)$ as $U_{RL0}(t) = U_{RL}(t)/U_{CB}(t_s)$. Fig. 4(a) shows the effect of saturated inductance $L_{ss}(t)$ on $U_{RL0}(t)$ at Port B. The main pulse of $U_{RL0}(t)$ starts to be formed since $t = t_s + \tau_{PFL}/2$. When $L_{ss}(t) = 0.1\,\mu\text{H}$, $0.5\,\mu\text{H}$, $1\,\mu\text{H}$, $2\,\mu\text{H}$, $5\,\mu\text{H}$ and $10\,\mu\text{H}$, the pulse rise time t_r of the main pulse of $U_{RL0}(t)$ increases from 6.25 ns to 31 ns, 62.5 ns, 125 ns, 130 ns and 130 ns, respectively. If $5L_{ss}(t)/Z_{out} > \tau_{PFL}$, no flat top of the main pulse can be formed because $t_r \geq \tau_{PFL}$. In Fig. 4(a), if $L_{ss}(t)$ is large enough and $t_r \geq \tau_{PFL}$, the amplitude of the main pulse of $U_{RL0}(t)$ is less than 1 and the energy stored in the main pulse dissipates along the time axis, which corresponds to a bad pulse modulation by the BTL and $L_{ss}(t)$. In view of the effects of wave reflection at the inductive Port B, the back edge time of the main pulse of $U_{RL0}(t)$ also increases in line with the increasing of $L_{ss}(t)$. As the impedance of the BTL is completely matched, no first sub-pulse and tail oscillation of $U_{RL0}(t)$ appear in Fig. 4(a).

Secondly, the case that $R_L = Z_{in} + Z_{out}$ and $Z_{in} \neq Z_{out}$ is analyzed, while $\tau_{PFL} = 2\tau_{out} = 2\tau_{in} = 130\,\text{ns}$. Obviously, there are two sub-cases such as $Z_{in} < Z_{out}$ and $Z_{in} > Z_{out}$. Fig. 4(b) shows the waveform of $U_{RL0}(t)$ when $Z_{in} < Z_{out}$. The main pulse of $U_{RL0}(t)$ shares similar changing laws to which shown in Fig. 4(a), and the main pulse amplitude still remains unchanged. As $Z_{in} < Z_{out}$, the sub-pulses and oscillation after the main pulse appear, and the first sub-pulse has the same polarity as which of the main pulse. If the port inductance $L_{ss}(t)$ is large, the main pulse amplitude decreases obviously, and the main pulse and the first sub-pulse are in superposition. When $Z_{in} > Z_{out}$, the waveform of $U_{RL0}(t)$ is shown in Fig. 4(c). The main pulse amplitude still remains unchanged, but the polarity of the first sub-pulse is reverse to which of the main pulse. Large port inductance $L_{ss}(t)$ can also cause amplitude decrement and bad waveform of the main pulse. In Fig. 4(d), the first sub-pulse disappear if $Z_{in} = Z_{out}$. Therefore, whether $R_L = Z_{in} + Z_{out}$ or not, sub-pulses and pulse tail oscillation appear after the main pulse if $Z_{in} \neq Z_{out}$. However, whether $R_L = Z_{in} + Z_{out}$ or not, the first sub-pulse after the main pulse can be eliminated if $Z_{in} = Z_{out}$.

According to (6) and (7), the amplitudes of the first sub-pulse and

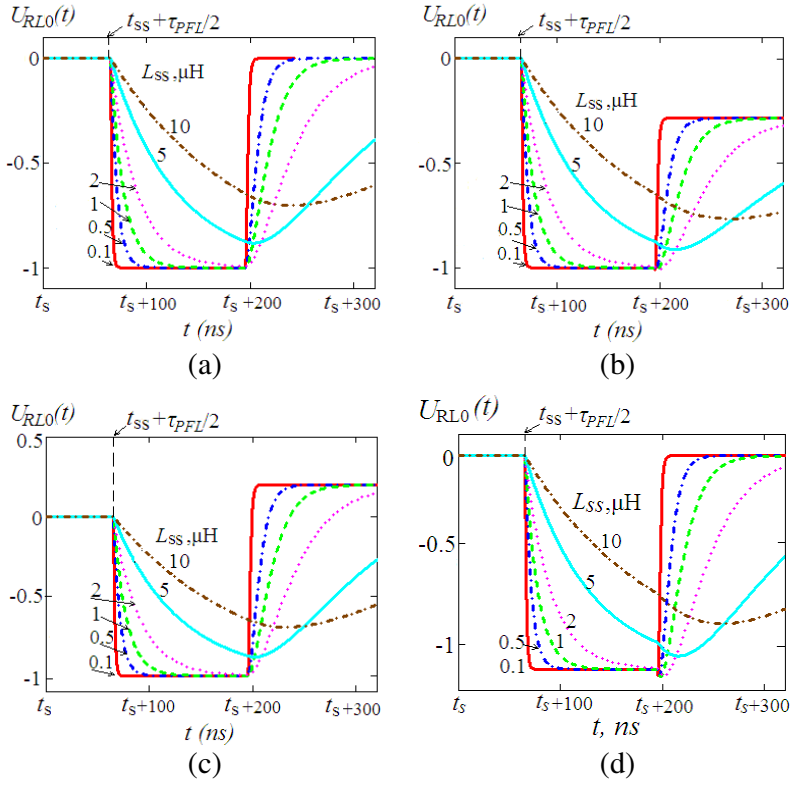

Figure 4. Effects of Wave reflection at inductive Port B on the waveforms of $U_{RL0}(t)$ during the stage $t_s \leq t \leq t_s+2\tau_{PFL}$; (a) Effects of L_{ss} on $U_{RL0}(t)$ when $Z_{in} = Z_{out}$ and $R_L = Z_{in} + Z_{out}$; (b) Effects of L_{ss} on $U_{RL0}(t)$ when $R_L = Z_{in}+Z_{out} = 200\,\Omega$ and $Z_{in} = 80\,\Omega < Z_{out} = 120\,\Omega$; (c) Eeffects of L_{ss} on $U_{RL0}(t)$ when $R_L = Z_{in} + Z_{out} = 200\,\Omega$ and $Z_{in} = 120\,\Omega > Z_{out} = 80\,\Omega$; (d) Effects of L_{ss} on $U_{RL0}(t)$ when $Z_{in} = Z_{out} = 80\,\Omega$ and $R_L = 200\,\Omega > Z_{in} + Z_{out}$.

the main pulse of $U_{RL}(t)$ have the ratio k as

$$k = \frac{1}{2}\left[\alpha_C \frac{Z_{out}}{R_L + Z_{out}} - \alpha_D \frac{Z_{in}}{R_L + Z_{in}} + \xi_C - \xi_D\right]. \tag{12}$$

Obviously, if the impedances of the BTL are matched completely ($Z_{in} = Z_{out}$ and $R_L = Z_{in} + Z_{out}$), $k \equiv 0$ and the wave energy is completely delivered to the load R_L in the formed main pulse of $U_{RL}(t)$. Therefore, only if $Z_{in} = Z_{out}$ is satisfied, $k \equiv 0$ and no sub-pulses and pulse tail oscillation appear after the main pulse, which shows an

important rule for pulse modulation technology of the BTL. Another important conclusion is that decreasing $L_{ss}(t)$ and increasing Z_{out} are two effective methods to obtain quasi-square voltage pulse with short rise time and fall time.

4. SIMULATION AND EXPERIMENTS

4.1. Pspice Simulations

According to the analysis of Fig. 3(a) aforementioned, $\alpha_{Bu}(t) = 2U_{CB0}(t)$ at Port B. The transmission coefficient $\alpha_{Bu}(t)$ of the voltage wave at Port B can be obtained through simulating the transmitting voltage wave $U_{CB}(t)$ or $U_{CB0}(t)$. Pspice codes were employed to do this job for demonstration. The Pspice schematic was the same as shown in Fig. 1(b), and the circuit parameters were set as $Z_{in} = Z_{out} = 80\,\Omega$, $R_L = Z_{in} + Z_{out} = 160\,\Omega$ and $\tau_{PFL} = 2\tau_{out} = 2\tau_{in} = 130\,\text{ns}$. Fig. 5(a) shows the simulation result of $U_{CB0}(t)$ while t_s=750 ns, the obtained $U_{CB0}(t)$ basically shared the same changing law as Fig. 3(a) (theoretical result) shows. As the saturated inductance $L_{ss}(t)$ increases at Port B, the front edge of $U_{CB0}(t)$ shown in Fig. 5(a) was delayed and electromagnetic waves were strongly transmitted from the BTL to the outside at Port B. When $L_{ss} = 0.5\,\mu\text{H}$, the $U_{CB0}(t)$ obtained from Pspice simulation and theoretical calculation is shown in Fig. 5(b). Obviously, the two of curves $U_{CB0}(t)$ versus t are in a good

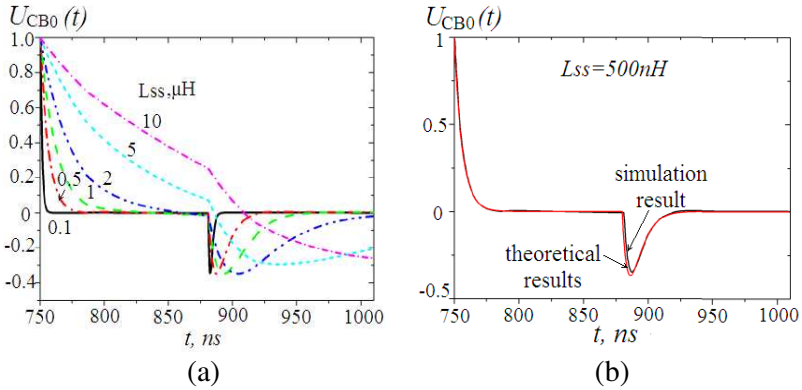

Figure 5. Pspice simulation results of $U_{CB0}(t)$ at the inductive Port B; (a) Effects of L_{ss} on $U_{CB0}(t)$ during the stage $t_s \le t \le (t_s + 2\tau_{PFL})$; (b) Comparison of the simulation and theoretical calculation results of $U_{CB0}(t)$ when $L_{ss} = 500\,\text{nH}$.

superposition, which demonstrates that analysis of $U_{CB}(t)$ shown is correct. As a result, the proposed new theoretical method for variable reflection and transmission of electromagnetic waves at the inductive port of transmission line was demonstrated to be correct.

Pspice simulation is also used to demonstrate the formed normalized voltage pulse $U_{RL0}(t)$ on the load R_L shown in Fig. 1(a). Under the complete matching conditions such as $Z_{in} = Z_{out} = 80\,\Omega$, $R_L = Z_{in} + Z_{out} = 160\,\Omega$ and $\tau_{PFL} = 2\tau_{out} = 2\tau_{in} = 130\,\text{ns}$, the simulation results of $U_{RL0}(t)$ are shown in Fig. 6(a). As the pre-pulse effect of $U_{RL0}(t)$ exists during BTL charging ($t < t_s = 750\,\text{ns}$), $U_{RL0}(t_s)$ is lower than 0. The main pulse of $U_{RL0}(t)$ has a pulse droop, due to the nonuniform charging of the BTL in a very short course. After a τ_{out} delay since $t_s = 750\,\text{ns}$, the front edge of $U_{RL0}(t)$ begin to form. Through comparing the theoretical calculation results shown in Fig. 4(a) under the same conditions, the effect of L_{ss} on the front and back edge of the main pulse of $U_{RL0}(t)$ is similar to which shown in Fig. 4(a). The $U_{RL0}(t)$ pulses obtained from simulation basically correspond to the waveforms obtained from theoretical calculation.

Under the partial matching conditions such as $Z_{in} = 120\,\Omega$, $Z_{out} = 80\,\Omega$, $R_L = Z_{in} + Z_{out} = 200\,\Omega$, $L_{ss} = 500\,\text{nH}$ and $\tau_{PFL} = 2\tau_{out} = 2\tau_{in} = 130\,\text{ns}$, the pulse waveform of $U_{RL0}(t)$ is simulated

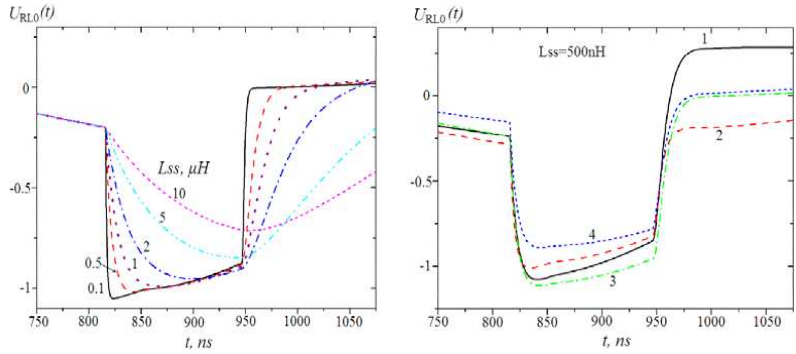

Figure 6. Pspice simulation results of $U_{RL0}(t)$ on the load R_L; (a) Effects of L_{ss} on $U_{RL0}(t)$ during the stage $t_s \le t \le (t_s + 5\tau_{PFL}/2)$; (b) Simulation waveforms of $U_{RL0}(t)$ under different impedance conditions when $L_{ss} = 500\,\text{nH}$ (curve 1: $Z_{in} = 120\,\Omega$, $Z_{out} = 80\,\Omega$, $R_L = 200\,\Omega$; curve 2: $Z_{in} = 80\,\Omega$, $Z_{out} = 120\,\Omega$, $R_L = 200\,\Omega$; curve 3: $Z_{in} = Z_{out} = 80\,\Omega$, $R_L = 200\,\Omega$; curve 4: $Z_{in} = Z_{out} = 80\,\Omega$, $R_L = 120\,\Omega$).

as Curve 1 shown in Fig. 6(b). The amplitude of the main pulse is -1, but the first sub-pulse with reverse polarity has the amplitude of $+0.26$. The theoretical calculation result in Fig. 4(c) shows that the first sub-pulse has the amplitude of $+0.24$ under the same conditions. The theoretical calculation and simulation results correspond with each other.

Under the partial matching conditions such as $Z_{in} = 80\,\Omega$, $Z_{out} = 120\,\Omega$ and $R_L = Z_{in} + Z_{out} = 200\,\Omega$, the pulse waveform of $U_{RL0}(t)$ is simulated as Curve 2 shown in Fig. 6(b). The main pulse amplitude also is -1, and the first sub-pulse with the same polarity as the main pulse has the amplitude of -0.22. The theoretical calculation result of the first sub-pulse amplitude is -0.28 in Fig. 4(b) under the same conditions, which basically corresponds to the simulation results (-0.22).

Under the impedance conditions such as $Z_{in} = Z_{out} = 80\,\Omega$ and $R_L = 200\,\Omega > (Z_{in} + Z_{out})$, the pulse waveform of $U_{RL0}(t)$ is simulated as Curve 3 shown in Fig. 6(b). The main pulse amplitude is -1.12 and the amplitude of the first sub-pulse is 0, which basically correspond to theoretical results shown in Fig. 4(d). Under the impedance conditions such as $Z_{in} = Z_{out} = 80\,\Omega$ and $R_L = 120\,\Omega < (Z_{in} + Z_{out})$, the pulse waveform of $U_{RL0}(t)$ is simulated as Curve 4 shown in Fig. 6(b). The main pulse amplitude is -0.86 and the amplitude of the first sub-pulse is 0, which also demonstrates that the first sub-pulse can be eliminated by the condition $Z_{in} = Z_{out}$.

In conclusion, the fact that simulation results basically correspond to the theoretical calculation results demonstrates the correctness of the proposed theoretical method of variable wave reflection and transmission at the inductive port of transmission line.

4.2. Experiments

Experimental set-up was established as shown in Fig. 7(a) to demonstrate the proposed theoretical method of variable reflection and transmission of waves at the inductive port of BTL. The experimental set-up consisted of a 175 nF/36 kV charging capacitor C_1, a 1 : 9 SPT, a BTL and a load resistor R_L. The schematic of the experimental set-up was the same as Fig. 1(a) or Fig. 1(b), and the ground inductance L_{gnd} was 77 µH.

Firstly, the transmitting voltage pulse $U_{CB}(t)$ and the voltage wave transmission coefficient $\alpha_{Bu}(t)$ at Port B of the BTL were tested under the full impedance matching conditions ($Z_{in} = Z_{out} = 80\,\Omega$, $R_L = Z_{in} + Z_{out} = 160\,\Omega$). The electric lengths of the inner line and outer line of the BTL were as $\tau_{out} = \tau_{in} = 65$ ns. The primary charging capacitor C_1 with initial voltage of 11 kV charged the BTL,

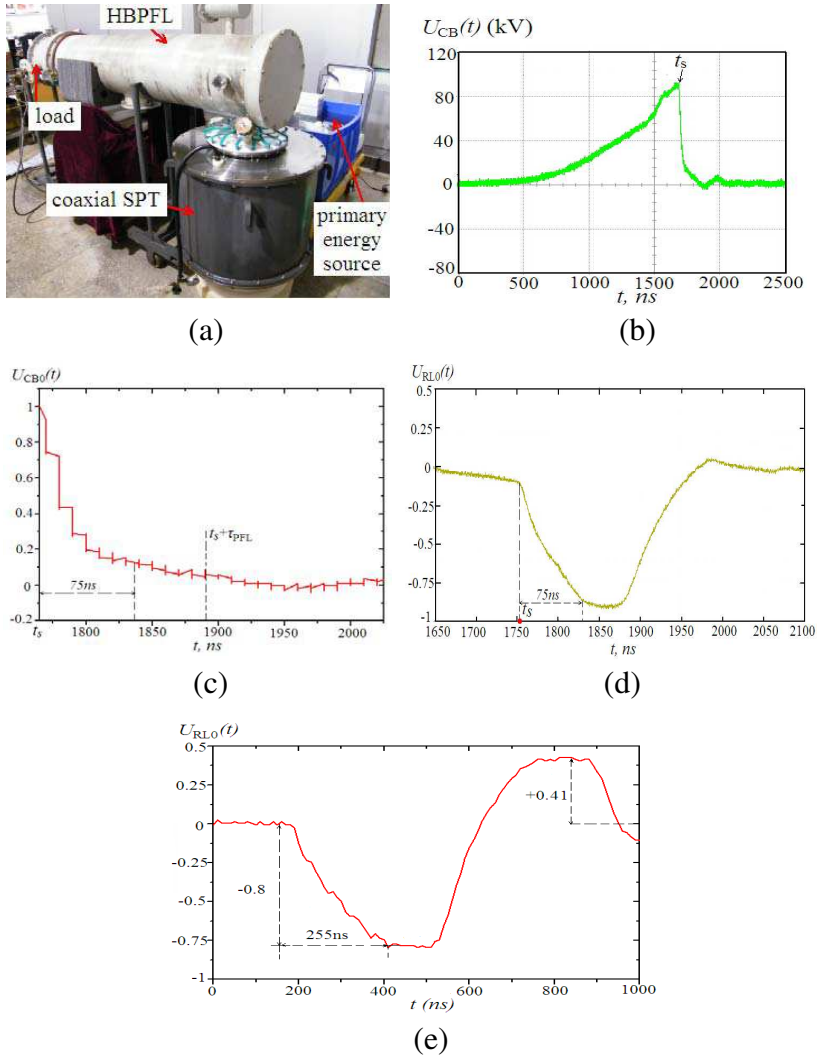

Figure 7. Experimental setup and tested results of $U_{CB}(t)$, $U_{CB0}(t)$ and $U_{RL0}(t)$; (a) The experimental setup; (b) The obtained $U_{CB}(t)$ from the charge stage of the BTL to the load pulse forming stage while the impedances were fully matched; (c) The obtained $U_{CB0}(t)$ at the inductive Port B during the stage $t_s \leq t \leq (t_s + 2\tau_{PFL})$; (d) Waveform of $U_{RL0}(t)$ in experiment when the impedances of the BTLwere completely matched; (e) Typical waveform of $U_{RL0}(t)$ in experiment when $Z_{in} = 50\,\Omega$, $Z_{out} = 25\,\Omega$, $R_L = 35\,\Omega$.

and $U_{CB}(t)$ at Port B was tested as shown in Fig. 7(b). Since $t = 500\,\text{ns}$, the BTL started to be charged; the charging course was over until $t = t_s = 1760\,\text{ns}$, and the maximum charging voltage $U_{CB}(t_s) = 92\,\text{kV}$. During the charging course of the BTL ($t < t_s$), the saturated inductance $L_{ss}(t)$ of the secondary windings of SPT was large enough and Port B equated to an open port. However, when $t > t_s$, the SPT also playing as a magnetic switch in Fig. 1 saturated and $L_{ss}(t)$ quickly decreased to a low level. The generated traveling waves were variably transmitted and reflected at Port B, and the amplitude of $U_{CB}(t)$ decreased from $U_{CB}(t_s)$ to 0.

The normalized transmitting voltage pulse $U_{CB0}(t)$ is shown in Fig. 7(c) form t_s, according to the tested $U_{CB}(t)$ in Fig. 7(b). The fall time of $U_{CB0}(t)$ was tested as 75 ns, and $L_{ss}(t)$ was extrapolated as about $1\,\mu\text{H}$, according to (9). The voltage wave transmitting coefficient at Port B was obtained as $\alpha_{Bu}(t) = 2U_{CB0}(t)$, from the experimental results shown in Fig. 7(c). The experimental waveform of $U_{CB0}(t)$ basically corresponded with the theoretical calculation waveform shown in Fig. 5(a) ($L_{ss}(t) \approx 1\,\mu\text{H}$) during the stage that $t_s \le t \le (t_s + \tau_{PFL})$, which demonstrated that the proposed theoretical method on variable traveling wave reflection was correct and reliable.

The obtained $U_{RL0}(t)$ on load in experiment is shown in Fig. 7(d). Since $t_s = 1760\,\text{ns}$, the main pulse of $U_{RL0}(t)$ began to form and the pulse rise time $t_r = 75\,\text{ns}$ which was the same as the fall time of $U_{CB0}(t)$ shown in Fig. 7(c). The back edge time of the main pulse of $U_{RL0}(t)$ was about 50 ns. The amplitudes of the main pulse and the first sub-pulse of $U_{RL0}(t)$ were -0.9 and 0, respectively. The tested $U_{RL0}(t)$ pulse basically corresponded with the $U_{RL0}(t)$ curve ($L_{ss}(t) \approx$ μH) shown in Fig. 4(a).

Through changing the filling dielectric of the BTL in experiment, the characteristic impedances and electric lengths of the BTL were regulated as $Z_{in} = 50\,\Omega$, $Z_{out} = 25\,\Omega$, $Z_{in} + Z_{out} > R_L = 35\,\Omega$ and $\tau_{out} = \tau_{in} = 193\,\text{ns}$. The normalized voltage pulse $U_{RL0}(t)$ on load was tested as shown in Fig. 7(e). The rise time t_r of $U_{RL0}(t)$ was about 255 ns which corresponded to the result $L_{ss}(t) \approx 1.27\,\mu\text{H}$ extrapolated from (9). The amplitude of the main pulse of $U_{RL0}(t)$ was less than -1, and the first sub-pulse had the reverse polarity in contrast to the main pulse (similar to Fig. 4(c)). In experiment, the tested amplitudes ratio k defined in (12) was $k = -0.41/0.8 = -51.3\%$. Through theoretical calculation from (12), $k = -45.6\%$. The theoretical calculation and experimental results of k basically corresponded to each other, which demonstrated that the proposed new theoretical method for variable reflection and transmission of electromagnetic waves at the inductive port of transmission line was correct.

5. CONCLUSIONS

In this paper, a new theoretical method for variable reflection and transmission of electromagnetic waves at the inductive port of transmission line is put forward, in order to analyze the wave reflection characteristics of the BTL at the inductive port of a saturated magnetic switch. At the inductive port, the variable reflection and transmission mechanisms of the voltage waves traveling through the BTL are analyzed in detail, and the effects of the inductive port on the rise time, flat top and tail oscillations of the load voltage pulse formed by the BTL are studied. It revealed that the inductance outside the BTL port delayed the port transition course from the open state to the short-circuit state, and the variable reflection and transmission of the traveling waves were caused at the BTL port during the transition course. The port transition course from the open state to the short-circuit state can be shortened and the variable reflection and transmission effects of waves can be suppressed by decreasing the inductance outside the BTL port, so that the rise time and fall time of the formed load voltage pulse are shortened. Simulation and experimental results demonstrated the proposed new theoretical method which shows great value for high-power microwave technology, high-power pulse forming, pulse shaping and modulation.

ACKNOWLEDGMENT

This work is supported by the National Natural Science Foundation of China under Grant No. 51177167. It's also supported by the Fund of Innovation, Graduate School of National University of Defense Technology under Grant No. B100702. Furthermore, the work is supported by Hunan Provincial Innovation Foundation for Postgraduate under Grant No. CX2010B034.

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